Analysis of Low Power High S-Carry Multi Adder

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***Abstract*:- Adder plays a major role in any part of the combinational system like subtractions, high speed multiplication, DSPs and ALUs. Any computational system requires fast process to be carried out. Carry select adder (CSLA) is one of the high speed adder used in many computations to perform fast arithmetic operations. The logic operation involved in conventional carry select adder and binary to excess -1 converter based CSLA are analyzed to study the data dependence to identify redundant logic operations. The modified CSLA has been developed using gate-level modification to significantly reduce the delay and power of CSLA. Based on this modification 8, 16, 32, 64, and 128-bit square root carry select adder (SQRT CSLA) architecture have been developed and compared with regular carry select adder architecture. The proposed design for higher adder has reduced power and delay is compared with the regular and modified SQRT CSLA. For 256-bit addition, it is proposed to simple gate level modification which significantly reduces the power by 19.4%. So this paper specially concentrates on speed and area constraints of CSLA.**

Keywords: SQRT CSLA, BEC with MUX, AOI

1. INTRODUCTION

In recent years, the increasing demand for high speed arithmetic units in microprocessors, image processing units and DSP chips has paved the path for development of high speed adders as addition is an indispensable operation in almost every arithmetic unit [1]. To increase portability of systems and battery life, area and power are the critical factors of concern. Furthermore for the applications such as the RISC processor design, where single cycle execution of instructions is the key measure of performance of the circuits, use of an efficient adder circuit becomes necessary, to realize efficient system performance [2]. However the regular CSLA is not area and power efficient because it uses multiple pairs of ripple carry in order to generate a partial sum with $C_{in} = 0$ and $C_{in} = 1$,then the final sum and carry are selected by multiplexers.

2. MATERIALS

The main idea of this work is to use BEC instead of the RCA with $C_{in} = 1$ in order to reduce the area and power consumption of the regular CSLA. To replace the *n*-bit RCA, an *n*+1-bit BEC is required [3]. The modified CSLA architecture has developed using Binary to Excess-1 converter (BEC). Fig. 1 illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the MUX. The XOR gate in BEC of Modified CSLA is replaced with the optimized XOR gate in AOI of Modified Area Efficient CSLA .With BEC there is reduction of gates by replacing n bit RCA with n+1 bit BEC [4]. When the

optimized XOR gate is used in Modified CSLA, it is verified that there is large reduction in number of gates.

$$X0 = {\sim}B0$$
$$X1 = B0 \wedge B1$$
$$X2 = B2 \wedge (B0\&B1)$$
$$X3 = B3 \wedge (B0\&B1\&B2)$$
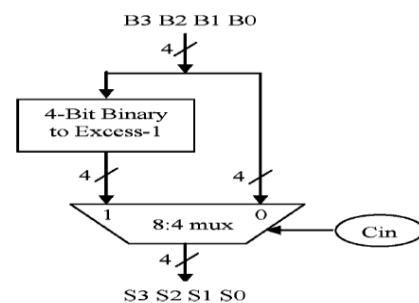
Fig.1 BEC with MUX

c6, sum[6:4]} = c3[t = 10] + mux
c10, sum[10:7]} = c6[t = 13] + mux
c15, sum[15:11]} = c10[t = 16] + mux
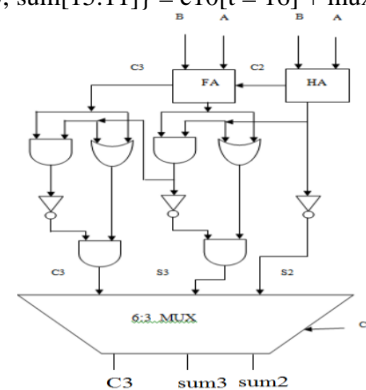
(a)
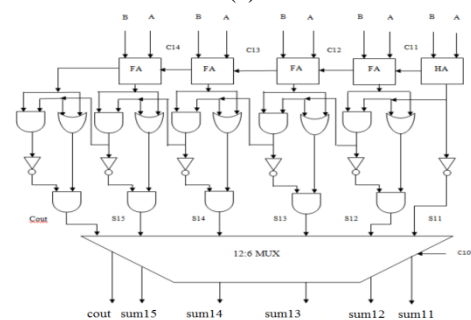
(b)

Fig. 2 (a) group 1, (b) group 5 (Modified CSLA)

3. METHODS

Delay Evaluation Methodology of Regular 16-b Sqrt CSLA: The structure of the 32-bit regular SQRT CSLA. It has groups of different sizes RCA.1). The group2 [see Fig. 2(a)] has two sets of 2-bit RCA. The sum3 is summation of S3 and MUX and sum 2 is summation of c1 and MUX, based on the delay values stated earlier and thereby their respective arrival time.2) Except for group2, the arrival time of MUX selection input is always greater than the arrival time [5]

Proposed Sqrt Carry Select Adder:

In this type of Adder, the block of Ripple Carry Adder with input carry as 1 has been replaced with a block of Binary to Excess-1 converter (BEC) [6]. This is done in order to reduce the area and power requirement of the previous conventional Carry Select Adder.

TABLE: I (Area count of CSLA)

GROUP NO.	REGULAR	MODIFIED
2	64	50
3	94	73
4	124	96
5	154	119
6	184	142
7	214	165

TABLE: II (% Reduction)

WORD SIZE(BIT)	AREA	AREA-DELAY	POWER	POWER-DELAY
8	17.3	5.5	12.10	0.46
16	19.02	10.3	13.81	4.34
32	20.2	13.2	16.87	8.41
64	20.69	18.1	17.84	15.05
128	20.8	19.5	18.78	17.4
256	21.58	22.28	19.4	21.1

Delay Evaluation methodology Of Modified:

32-b SQRT CSLA: The structure is given in Fig.2. The steps leading to the delay evaluation are given here Table I and Table II.

a. The second group has a 2-b RCA. Instead of another 2-bit RCA with C_{in} = 1 a 3-b BEC is used which adds 1 to the output from 2-bit RCA [7]. Based on the values of Table I, the arrival time of selection input c1 of 6:3 MUX is earlier than the s3 and c3 and later than the s2.

b. For the remaining groups the arrival time of MUX selection input is always greater than the arrival time of data inputs from the BECs.

Comparing the delay values of the earlier models and the proposed model, the reduction in area [11], power and delay values are given in table IV percentage.

4. RESULTS AND DISCUSSIONS

The design proposed in this paper has been developed using Verilog HDL and synthesized in Cadence RTL compiler using typical libraries of TMSC 180nm technology [10]. Designs of CSLA were developed using structural Verilog module and synthesized using Xilinx ISE simulator, version 10.1 and the implementation is done in cadence RTL compiler.
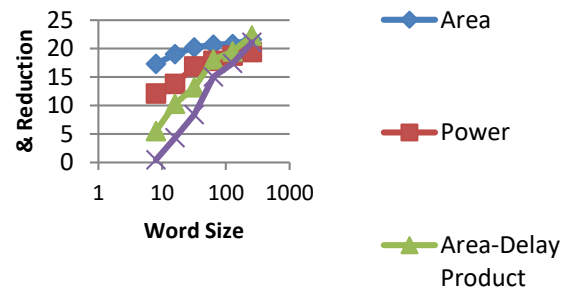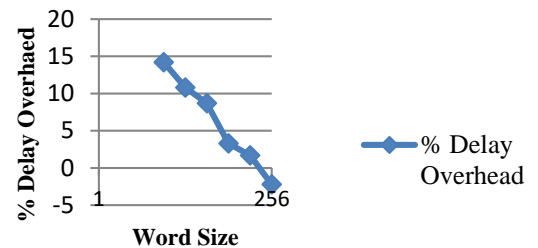

Fig.3 Percentage reduction in the cell area, total power, power delay product, and area–delay product

5. CONCLUSION

After comparing the different parameters of various adders with the proposed modified SQRT CSLA, it is evident that the power dissipation has been reduced to the desired extent with a slight increase in area. The proposed model provides a good tradeoff between the time and power consumption. Hence the modified 256-bit CSLA is more efficient for the VLSI hardware implementation. Further work is to be done in reducing the area and for higher order adders (512-bit), thus improving the overall system performance as such.

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