Analysis of Cuk Converters for Power Factor Correction Applications

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Abstract—**This paper presents the clear view of need for power factor correction. It also discussed the conventional types of power factor correction methods employed by the use of power electronic converters. The drawbacks of the conventional converter are overcome and new proposed converters with three different configurations are analyzed in this paper. The working of all the three types of converters is illustrated with the waveforms. The theoretical concepts are followed by the simulation results of all the three proposed converters. The simulation results are justified by the hardware implementation of the Cuk Converters.**

Keywords—*dicontinuous mode of operation; power factor correction; less ripple current; cuk converters.*

I. INTRODUCTION

Most of the equipments involved in the sophistication of the people are made to operate with power supplies of unity power factor. The machines operating with fixed power supplies along with active power factor are applied in many areas like communication, computer, automotive & biomedical industries. The fixed power supply can be achieved by means of power electronic components. Also to meet out the harmonic regulations & standards, Power Factor Correction (PFC) is needed. The active power factor correction is needed for the efficient working of the equipments. The active power factor correction using power electronics components found to be economical, efficient & reliable. So, this paper will present an idea about power factor correction using Cuk converters. The conventional power factor corrective methods and their drawbacks are discussed in the Section II. Section II discusses the proposed method for power factor correction. Its theoretical analysis along with the explanation of three types of proposed circuit. Section III presents the simulation results of the proposed method along with the output and input voltage waveforms and with tables tabulating the values of power factor for many loads. Section IV gives the hardware implementation of the proposed method with the relevant waveforms. Finally, Section V discussed the conclusion of the work presented in this paper.

II. CONVENTIONAL POWER FACTOR CORRECTION METHODS

Power factor correction using conventional converters are analyzed in this section. The PFC scheme has been configured in three different converters. The PFC schemes are analyzed in Boost, Buck and Cuk converters topology.

A. Drwabacks of using Boost converter for PFC applications

The boost converter when operated in discontinuous current mode (DCM) leads to the output current with high ripple content. This disadvantage has made it not suitable for the power factor applications.

B. Drawbacks of using Buck converter for PFC applications

In the operation of the buck converter in DCM, the input current does not follow the input line voltage. Moreover, the output voltage ratio is nearly reduced to half. The efficiency of the buck converter is also poor because of the high harmonic distortion at the output side and reduced power factor.

C. Analysis of Cuk converter for PFC applications

The cuk converter designed for power factor correction can be operated in both continuous and discontinuous current modes has many advantages like easy implementation of the transformer isolation, protection against high inrush current, low current ripple and also less Electromagnetic Interference (EMI). The conventional Cuk converter is illustrated in the Fig. 1.

The conventional Cuk converter has a diode bridge at the front end of the circuit. The diodes conduct in both positive and negative cycles and leads to large conduction loss and so efficiency is reduced. It acts as the major reason for the development of new PFC topology using bridgeless Cuk converter. The detailed working of these conventional converters is discussed in Thus, the Section II has briefly demonstrated the conventional methods of PFC and their
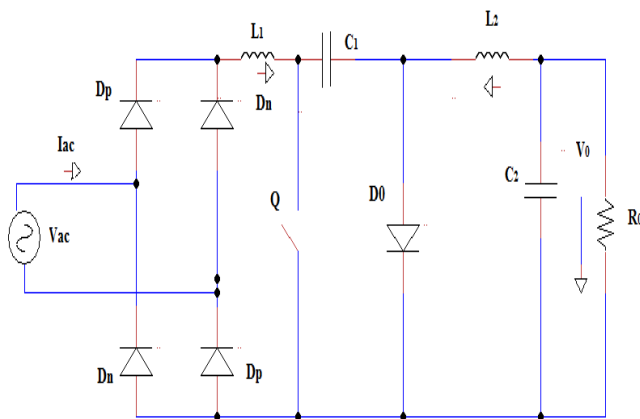
drawbacks.

Fig. 1. Conventional Cuk converter

III. PROPOSED CUK CONVERTER FOR POWER FACTOR CORRECTION APPLICATIONS

This chapter discusses about the need for new topology of PFC. New experiments were conducted to improve the efficiency by replacing the front end bridge by two switches alone. By doing so, the efficiency of converter increased also it is found to be economical.
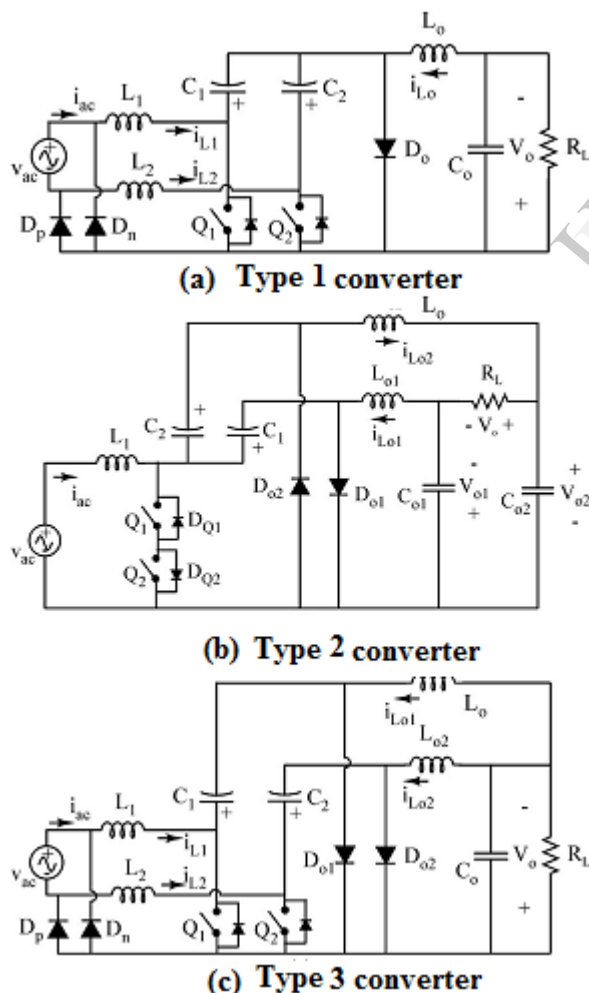

Fig. 2 Types of the Proposed Cuk Converter

The proposed Cuk converter is the combination of two dc-dc rectifiers, each one conducts for one half cycles. There is only one or two semiconductors in the process of connecting the input voltage to the output side which means that the conduction losses and the stress upon the switches are also greatly reduced thereby increasing the efficiency of the proposed scheme. The new topology has another advantage of low EMI when compared with the conventional one. The circuit consists of two semiconductor switches which can be operated depending upon the voltage ratio required by any load.

The circuit also has an additional inductor which improves the thermal performance of the circuit. The three inductors can be coupled on the same magnetic core for reducing the cost and size of the circuitry also. The working of type -1 converter is discussed in detail in [1]-[10]. The working of type-2 converter is not discussed in [19].

A. OPERATION OF TYPE 3 CUK CONVERTER

Before analyzing the converter, the following assumptions are made,

(i) The circuit is working in steady state with pure sine wave at its input side,

(ii) Lossless components,

(iii) The capacitors are large to maintain the voltage constant and to have zero ripple voltage.

During the positive half cycle, the first dc-dc cuk circuit, L_1 - Q_1 - C_1 – L_{01} –D_{01} are active through the diode D_p thereby connecting the input voltage to the output side load. During the negative half cycle, the second dc-dc cuk converter circuit, L_2 – Q_2 – C_2 – L_{02} –D_{02} are active through the diode D_n.

The proposed converter operates in DCM mode which has another advantage of near unity power factor. The switches are turned on at zero current and also the output diodes are turned off at zero current, thereby reducing the conduction losses.

Unfortunately the DCM operation has a disadvantage of limiting this topology to low power application alone. (<300W). The working of converter is very similar to the conventional cuk converter with three distinct stages in one switching period T_s.

The theoretical waveforms of cuk converter with DCM for positive half cycle alone are depicted in Fig. 3.

B. Stage 1 (t_0 to t_1)

In this stage, the switch Q_1 is in ON state. Diode D_p is forward biased by the inductor current I_{L1}. The diodes D_n, D_{01} and D_{02} are reverse biased. The current through the inductors L_1, L_{01} are linearly raised.

But, the current through L_{02} is zero due to the fixed capacitor voltage across C_2.

The peak current reached in this stage is given in (1).

$$I_{Q1,pk} = (V_m / L_e)* (D_1 T_s) \qquad (1)$$

Where, V_m is the maximum amplitude of the input voltage and D_1 is the duty cycle and L_e is the parallel combination of inductors L_1 and L_{01}.
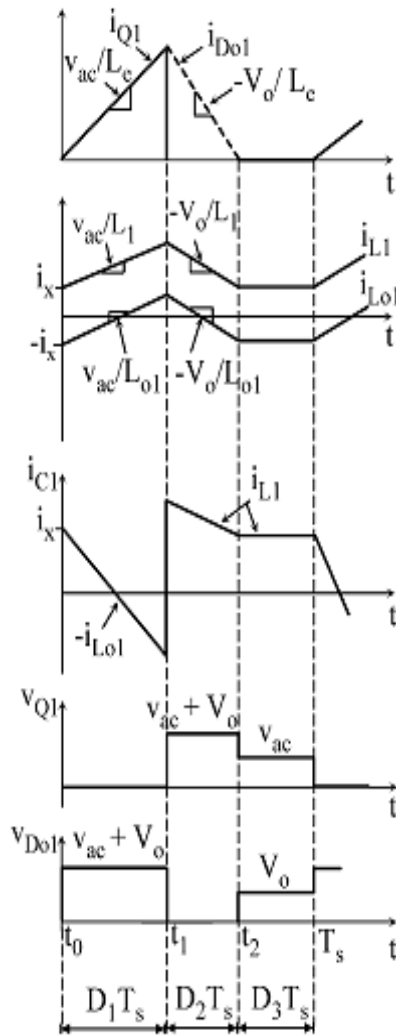
The second stage period can be derived and shown in (2) where, M is the voltage conversion ratio (V_0/V_m) ,

$$D_2 = (D_1/M) * \sin \omega t \qquad (2)$$

The working of the type 1 converter is very similar to the type 3 except for the stress across the output load side. Thus this Section III discussed about the working of Type 3 converter with necessary diagrams.

IV. SIMULATION RESULTS OF THE PROPOSED CUK CONVERTER

The new Cuk converter discussed in section III is validated by the simulation results. Type1, Type 2 & Type 3 converters are chosen for the simulation process and the simulation is done by using MATLAB software package. The simulation parameters of the converter are listed in Table I.

Table . I Simulation Parameters

Parameters	Values
Input Voltage , V_s	120*1.414
Inductors L_1, L_2	1mH
Capacitors C_1 , C_2	1μF
Output capacitor, C_0	12000μF
Output inductor, L_0	22μH
Input frequency, f_s	50 Hz
Switching frequency	50 KHz
Output resistor	50Ω

The waveforms obtained by the simulation of all the three types converters is shown in the Fig. 4. text edit has been completed, the paper is ready for the
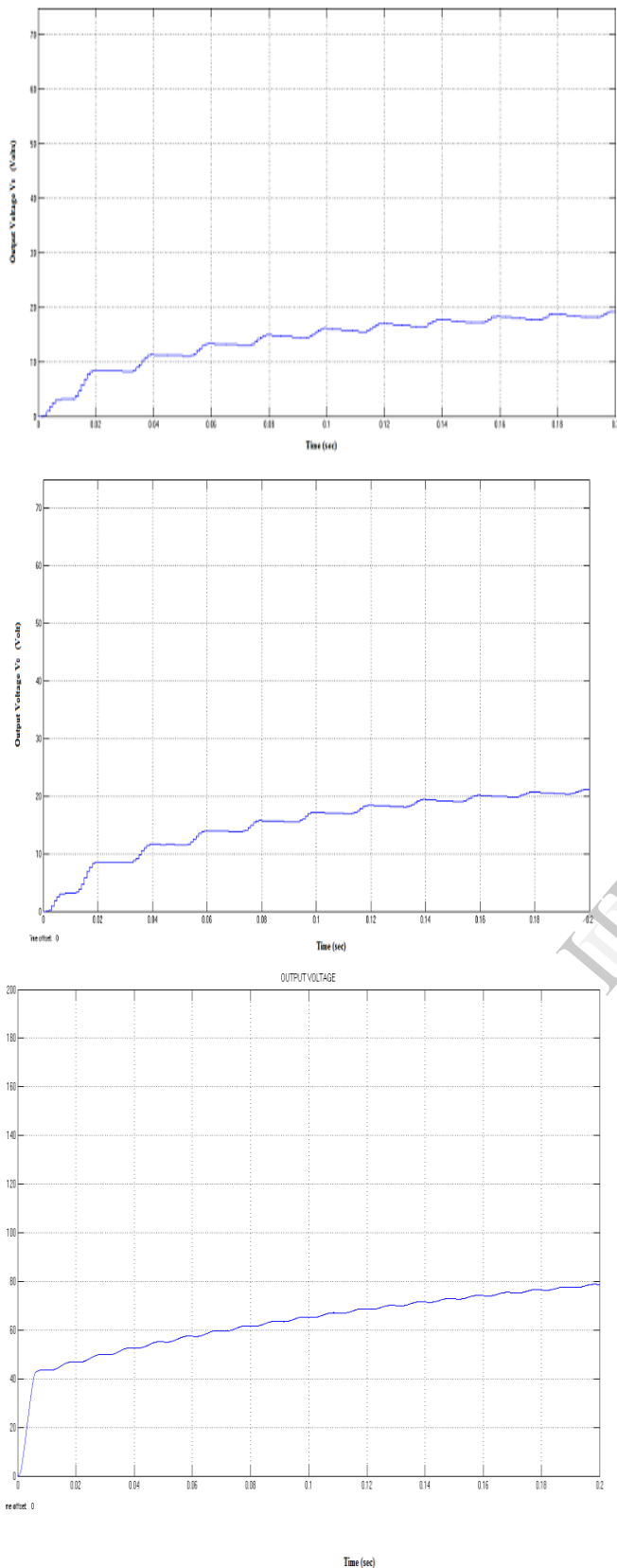

Fig. 3. Theoretical Waveforms of Type – 3 converter operating in DCM

C. Stage 2 (t_1 to t_2)

In this stage, the switch Q_1 is turned off but diode D_{01} is turned ON to provide a continuous current path for the inductors L_1, L_{01}. This stage ends when the current through D_{01} reaches zero and it become reverse biased. The current through the inductors are found be linearly decreasing. The magnitude of the decreasing current is shown in the waveform itself.

D. Stage 3 ($t_2,$ ts)

This stage operates with only one diode D_p in conduction to provide a current path for I_{L1}. The inductors will now behave as constant current sources and so no voltage across all the three inductors. Capacitor C_1 is charged by the inductor current I_{L1}. This stage ends when Q_1 getting turned ON.
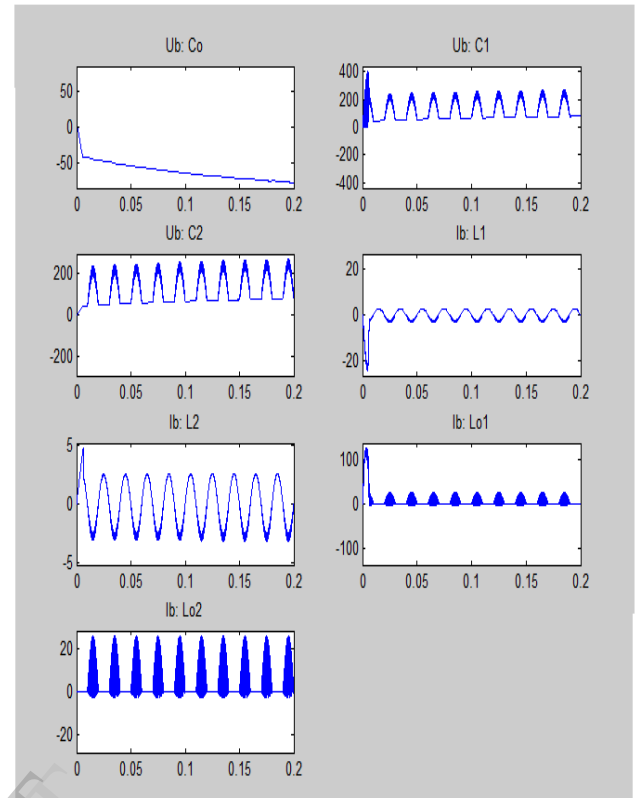
Fig. 5. Simulated Voltage and current waveforms across the inductors and capacitors

Thus, this section discussed about the simulation results of all the converters along with the waveforms.

V. HARWARE IMPLEMENTATION OF TYPE 3 CONVERTER

The type 3 converter discussed so far is now implemented in hardware. The output and the input voltage waveforms for this type of converter is shown in Fig. 6.

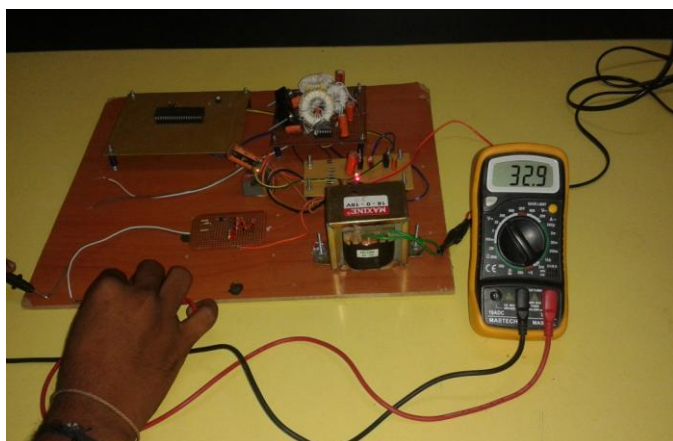Fig. 4. Simulated Output Voltage waveforms of Type 1, Type 2 and Type 3 Cuk converters

It is inferred from the waveforms that the type 3 converter is working efficiently. The waveforms across inductors and capacitors are illustrated in the Fig. 5.
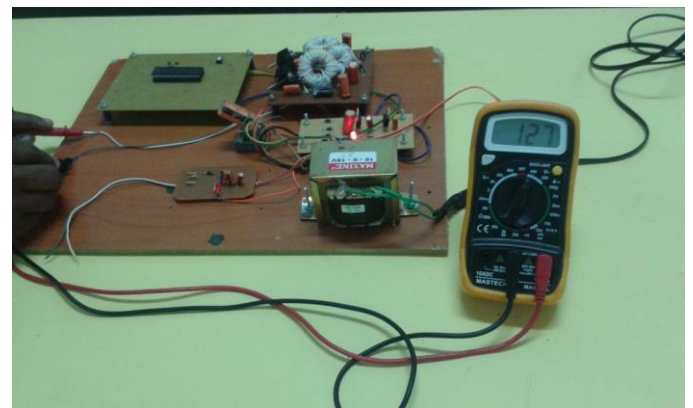
Fig. 6. Hardware implementation of type 3 converter with output load resistor of 15Ω**.**

VI. CONCLUSION

This paper discussed about the power factor correction converters using Cuk Topology. It also discussed about the conventional converters drawbacks and the proposed converters advantages. The proposed converter is simulated and the results are produced in this paper along with the hardware implementation. It is also concluded that among the three types, type 3 proves to be best and economical.

REFERENCES

1. Abbas A. Fardoun, Esam H. Ismail, Ahmad J. Sabzali and Mustafa A. Al-Saffar , " New efficient Bridgeless Cuk Converter for PFC application", IEEE Transactions on Power Electronics, Vol. 27, No. 7, July 2012.

2. W. Choi, J.Kwon, E.Kim, J. Lee, and B.Kwon, "Bridgeless boost rectifierwith lowconduction losses and reduced diode reverse-recovery problems,"IEEE Trans. Ind. Electron., vol. 54, no. 2, pp. 769–780, Apr. 2007.

3. G. Moschopoulos and P. Kain, "A novel single-phase soft-switched rectifier with unity power factor and minimal component count," IEEE Trans.Ind. Electron., vol. 51, no. 3, pp. 566–575, Jun. 2004.

4. R.-L. Lin andH.-M. Shih, "Piezoelectric transformer based current-sourcecharge-pump power-factor-correction electronic ballast," IEEE Trans.Power Electron., vol. 23, no. 3, pp. 1391–1400, May 2008.

5. S. Dwari and L. Parsa, "An efficient AC–DC step-up converter for low-voltage energy harvesting," IEEE Trans. Power Electron., vol. 25, no. 8,pp. 2188–2199, Aug. 2010.

6. Y. Jang and M. Jovanovic, "A bridgeless PFC boost rectifier with opti-mized magnetic utilization," IEEE Trans. Power Electron., vol. 24, no. 1,pp. 85–93, Jan. 2009.

7. L. Huber, Y. Jang, and M. Jovanovic, "Performance evaluation of bridgeless PFC boost rectifiers," IEEE Trans. Power Electron., vol. 23, no. 3,pp. 1381–1390, May 2008.

8. B. Su and Z. Lu, "An interleaved totem-pole boost bridgeless rectifier with reduced reverse-recovery problems for power factor correction," IEEE Trans. Power Electron., vol. 25, no. 6, pp. 1406–1415, Jun. 2010.

9. B. Su, J. Zhang, and Z. Lu, "Totem-pole boost bridgeless PFC rectifier with simple zero-current detection and full-range ZVS operating at the boundary of DCM/CCM," IEEE Trans. Power Electron., vol. 26, no. 2,. 427–435, Feb. 2011.

10. H.-Y. Tsai, T.-H. Hsia, and D. Chen, "A family of zero-voltage-transition bridgeless power-factor-correction circuits with a zero-current-switching auxiliary switch," IEEE Trans. Ind. Electron., vol. 58, no. 5, pp. 1848–1855, May 2011.

11. H. Ye, Z. Yang, J. Dai, C. Yan, X. Xin, and J. Ying, "Common modenoise modeling and analysis of dual boost PFCcircuit," in Proc. Int.Telecommun. Energy Conf., Sep. 2004, pp. 575–582.

12. B. Lu, R. Brown, andM. Soldano, "Bridgeless PFC implementation using one cycle control technique," in Proc. IEEE Appl. Power Electron. Conf., Mar. 2005, pp. 812–817.

13. P. Kong, S.Wang, and F. C. Lee, "Common mode EMI noise suppression for bridgeless PFC converters," IEEE Trans. Power Electron., vol. 23,no. 1, pp. 291–297, Jan, 2008.

14. W.-Y. Choi, J.-M. Kwon, E.-H. Kim, J.-J. Lee, and B.-H. Kwon, "Bridge-less boost rectifier with low conduction losses and reduced diode reverse-recovery problems," IEEE Trans. Ind. Electron., vol. 54, no. 2, pp. 769–780, Apr. 2007.

15. C.-M. Wang, "A novel single-stage high-power-factor electronic ballast with symmetrical half-bridge topology," IEEE Trans. Ind. Electron.,vol. 55, no. 2, pp. 969–972, Feb. 2008.

16. B. Su, J. Zhang, and Z. Lu, "Single inductor three-level boost bridgeless PFC rectifierwith nature voltage clamp," IEEE Int. Power Electron. Conf.,pp. 2092–2097, Jun. 2010.

17. M.Mahdavi and H. farzanehfard, "Zero-current-transition bridgeless PFC without extra voltage and current stress," IEEE Trans. Ind. Electron.,vol. 56, no. 7, pp. 2540–2547, Jul. 2009.

18. W.-Y. Choi and J.-S. Yoo, "A bridgeless single-stage half-bridge AC/DC converter," IEEE Trans. Power Electron., vol. 26, no. 12, pp. 3884–3895, Dec. 2011.

19. W. Wei, L. Hongpeng, J. Shigong, and X. Dianguo, "A novel bridgeless buck-boost PFC converter," in Proc. IEEE Power Electron. Spec. Conf.,2008, pp. 1304–1308.

20. E. H. Ismail, "Bridgeless SEPIC rectifier with unity power factor and reduced conduction losses," IEEE Trans. Ind. Electron., vol. 56, no. 4,pp. 1147–1157, Apr. 2009.

21. A. Sabzali, E. H. Ismail, M. Al-Saffar, and A. Fardoun, "New bridgelessDCM sepic and Cuk PFC rectifiers with low conduction and switchinglosses," IEEE Trans. Ind. Appl., vol. 47, no. 2, pp. 873–881, Mar./Apr.2011.

22. M. Mahdavi and H. Farzanehfard, "Bridgeless SEPIC PFC rectifier with reduced components and conduction losses," IEEE Trans. Ind. Electron., vol. 58, no. 9, pp. 4153–4160, Sep. 2011.

23. M. R. Sahid, A. H. M. Yatim, and T. Taufik, "A new AC-DC converter using bridgeless SEPIC," in Proc. IEEE Annu. Conf. Ind. Electron. Soc.,Nov. 2010, pp. 286–290.

24. L. Huber, L. Gang, and M. M. Jovanovic, "Design-oriented analysis and performance evaluation of buck PFC front-end," IEEE Trans. Power Electron., vol. 25, no. 1, pp. 85–94, Jan. 2010.

25. Y. Jang and M. M. Jovanovi´ c, "Bridgeless high-power-factor buck converter," IEEE Trans. Power Electron., vol. 26, no. 2, pp. 602–611, Feb.2011.

26. J. M. Alonso, M. A. Dalla Costa, and C. Ordizl, "Integrated buck-flyback converter as a high-power-factor off-line power supply," IEEE Trans. Electron., vol. 55, no. 3, pp. 1090–110, Mar. 2008.

27. M. Brkovic and S. Cuk, "Input current shaper using Cuk converter," in Proc. Int. Telecommun. Energy Conf., 1992, pp. 532–539.

28. D. S. L. Simonetti, J. Sebastian, and J. Uceda, "The discontinuous conduction mode Sepic and Cuk power factor preregulators: Analysis and design," IEEE Trans. Ind. Electron., vol. 44, no. 5, pp. 630–637, Oct.1997.

29. Y.-S. Roh, Y.-J. Moon, J.-C. Gong, and C. Yoo, "Active power factor correction (PFC) circuit with resistor-free zero-current detection," IEEE Trans. Power Electron., vol. 26, no. 2, pp. 630–637, Feb. 2011.

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