Analysis of Behaviour of Different SRAM Cell

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***Abstract*:- SRAM is a type of memory. In any electronic device memory is a very essential part. In this paper we compare the different cell of SRAM .Basic operation of SRAM cell needs 6 transistor. These 6 transistors can perform write, read and hold operation. But there is a many problems occur in real life operation like power dissipation, stability, delay, area and so on. So some new transistors are added to remove or decrease these problems. Although we have to compromise with some issues. This paper compares the parameters with different configurations of SRAM cell.**

Keywords: SRAM, leakage current, Power Dissipation, Stability

I. INTRODUCTION:

Without electronic devices we cannot survive in today's aspects. But a researcher knows that to prepare a device many obstacles are present. The main issue in electronic device is a memory. Without memory we can't think about an electronic device. SRAM memory is one of the major blocks of high speed systems, and this memory occupy maximum part of the chip area [1].It is today's world demand that we are more comfortable with small and portable devices. So we have to work on nanometre technology. For increasing the speed of circuit and reducing the area of chip, introduced sub-micron technology. And in sub-micron technology we should take care of dynamic power consumption. However due to result of this scaling, sub-threshold leakage increased. Thus, these parameters like speed, leakagecurrent, area should proper optimize. [2]

II.SRAM CELLS AND ITS PARAMETERS:

1. Conventional 6T SRAM cell:

This cell has two inverters which connected back to back. The two access transistors are connected with these inverters. The access transistors are used for read and write operation. Figure 1 shows the structure of conventional 6transistor SRAM cell. There are three operation of memory:

(i)Write operation: Write signal (word line) activates for passing the data or we can say for writing the data, we have to activate word line. The access transistor pass the data into inverters.

(ii)Hold operation: In this operation deactivate the word line. Inverters hold the data which we have written during write operation. These inverters reinforce the data.

(iii)Read Operation: Signals read in this operation when activates the word line. In this operation, the access transistors are used to read the data. Bit lines are recharged during this read operation. Stability is a main issue when read the data.

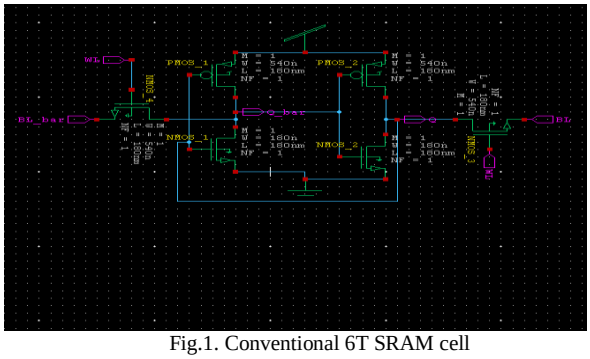

Fig.1. Conventional 6T SRAM cell

2. 7T SRAM cell:

One extra transistor are added for better performance.

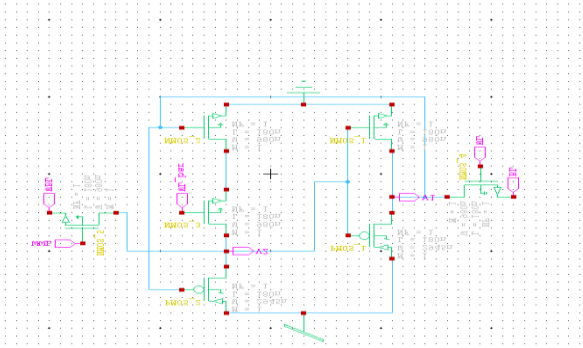

Fig.2. 7T SRAM cell

3.8T SRAM cell:

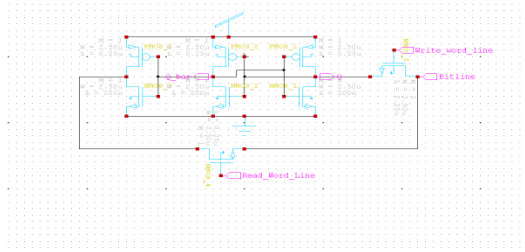

Fig.3. 8T SRAM cell

4.9T SRAM cell:

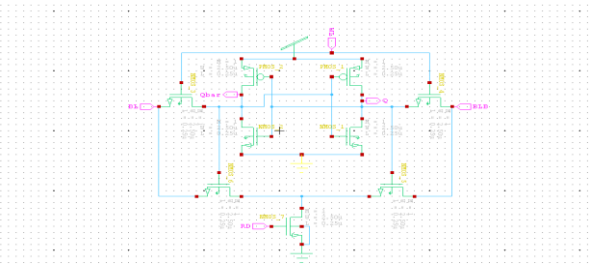

Fig.4. 9T SRAM cell

5.10T SRAM cell:

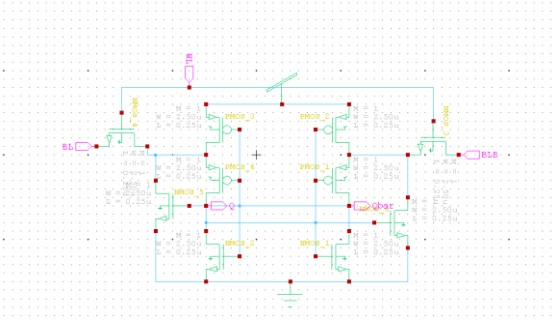

Fig.5. 10T SRAM cell

III. ANALYSIS OF DIFFERENT SRAM CELL:

Two parameters are analysed: Stability and leakage current.180nm technology are used for analysis.T SPICE of tanner tool is used for simulations.Two methods are used for SNM.SNM directly related to stability.One method is trial and error technique and another one is graphical technique.In trial and error technique two extra noise sources are connected between inverters and check the flip point of output.In graphical technique, butterfly curve is used for finding max SNM.

IV. CONCLUSION:

Different cell of SRAM are simulated using tanner tool. One thing should take care when inserting extra transistors is that operation cannot affected. We have designed structure upto 10 transistors. Two parameters are simulated stability and power dissipation using 180nm technology. We have to compromise with one parameter in every cell either area or power dissipation or stability or delay.

V. REFERENCES:

[1] Q. Chen, S. Mukhopadhyay, A. Bansal and K. Roy, "Circuit-aware Device Design Methodology for Nanometer Technologies: A Case Study for Low Power SRAM Design Design", Proceedings of Automation and Test in Europe, pp.1-6, 2006.

[2] Abhijit Sil, Soumik Ghosh, Neeharika Gogineni, Magdy Bayoumi, "A Novel High Write Speed, Low Power, Read-SNM-Free 6T SRAM Cell",

[3] H. Jiao, V. Kursun, Asymmetrical ground gating for low leakage and data robust sleep mode in memory banks, In: Proceeding soft he IEEE International Symposium on VLSI Design, AutomationandTest,pp.205–208, April2011.

[4] H. Jiao, V. Kursun, Low power and robust ground gated memory banks with combined write assist techniques, In: Proceeding soft he IEEE Faible Tension Faible Consommation, June2012

[5] H. Jiao, V. Kursun, Ground gated 8TSRAM cells with enhanced read and hold data stability, In: Proceeding soft he IEEE Computer Society Annual Symposium on VLSI, pp.52–57, August 2013.

[6] Predictive Technology Model (PTM).Available: ⟨http://www.eas.asu.edu/_ptm/⟩.