Analysis of 8T Sram using Energy Recovery Logic

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***Abstract*— High speed with low power requirement is a challenging task in the design of SRAM memory systems. As leakage power the major challenge of present chip designs. The modern technology is spreading fast, it is most important to design low power, high performance, and fast responding SRAM (Static Random Access Memory). The 6T SRAM cell is very much prone to noise during read operation. Researchers have proposed different SRAM topologies such as 8T, 9T, and 10T etc. bitcell design to overcome the problems in 6T SRAM cell these designs can improve the cell stability, but suffer from bitline leakage noise. A new method is suggested for simulate of SRAM by using the energy recovery logic in HSIPCE.**

Keywords*— Noise margin, Static Noise Margin (SNM), Stability and Power Consumption, read word line (RWL), write word line (WWL).

I. INTRODUCTION

Growths of the electronics devices are very fast as compare to other devices. Now the sizes of the devices are on nano-meter. As taking the examples of devices on 19th or 20th century they are large on size and slow on processing, but today it is not like that. The transistors are on small sizes, they are placed on every small device also. Sizes are also on nanometre and implementation is also very fast and easy. Very Large Scale Integration (VLSI), which is an implementation technology for electronic circuitry either analogue or digital. It is concerned with forming a pattern of interconnected switches and gates on the surface of a crystal of semiconductor. In VLSI, SRAM *(*Static Random Access Memory) is considered it is a type of memory that is faster and more reliable.

A SRAM cell consist of a latch, therefore the cell data is kept as long as power is turned on and refresh operation is not required for the SRAM cell. SRAM is mainly used for the cache memory in microprocessors, mainframe computers, engineering workstations and memory in hand held devices due to high speed and low power consumption. Each bit in an SRAM is stored on four transistors that form two cross coupled inverters, with increased device variability in nanometer scale technologies; SRAM becomes increasingly vulnerable to noise sources. [1]

The low-power processors, computers and super computers are using fast SRAMs and will require large quantity memories with faster access time. High-density, low-power SRAMs are needed for various applications such as laptops, notebooks and IC memory cards, due to the fact that these systems frequently use battery as power source and hence it should consume power, as low power as possible. Low cooling is also necessary for maintaining and packing costs are also required for these systems.

The power dissipation reduction in SRAMs can be achieved not only by power supply voltage reduction, but also using low-power circuit techniques. An SRAM cell must be designed such that it provides a non-destructive read operation and a reliable write operation [3]. Most useful part of the memory is SRAM so it must used very carefully the mismatch leads to reduced SRAM reliability.

II. 6T SRAM CELL

The conventional 6T memory cell comprised of two CMOS invertors cross coupled with two pass transistors connected to a complimentary bit lines as shown in Figure 1. The gate of access transistors N3 and N4 are connected to the WL (word line) to have data written to the memory cell or read from the memory cell through the BL or BLB (bitline) during write and read operation. The bit lines act as I/O buses which carry the data from the memory cell to the sense amplifier [2] SRAM cell perform three different operations, read, writes and holds operation.

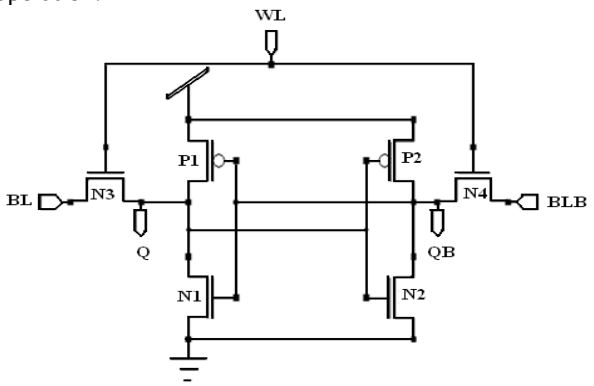


Figure1. 6T SRAM Cell

This 6T SRAM is used as a conventional way that means it is mostly considered for 6T SRAM. The read and write operation can be performed into this SRAM. This depends upon the "0"

and "1" value. Read and write operation can performed through this only.

There is another word called signal noise margin (SNM) is also calculated on SRAM, when the word line is set high and both bit line are still precharged high. At the start of read access, the bit lines are precharged to Vdd and then the wordlines are activated to access the cell. Increases in voltage severely degrade the SNM during the read operation.

III. PROBLEMS IN 6T SRAM CELL

The 6t-cell schematic is shown in figure 1.this most commonly used SRAM cell implementation; it is also called as conventional 6T SRAM. The advantage is that it is used less area. However, the potential stability problem of this design arises during read and writes operation, where the cell is most vulnerable towards noise and thus the stability of the cell is affected. if the cell structure is not designed properly, it may change its state during read and write operation[2].

IV. An 8T SRAM CELL

The problems have been encountered with the aggressive scaling in technology, when the conventional 6T (six transistors) SRAM cell configuration is utilized. An 8T cell can be found to solve the problem. The 6T SRAM shows poor stability at very small feature sizes, the hold and read static noise margins are small for robust operation and it is applicable for noise prone. 6T SRAM consists large number of noise problem. Therefore, an extensive way can be found on designing SRAM cells for low power operation. The common approach to meet the objective of low power design is to add more transistors to the original 6T cell. This cell employs two more transistors to access the read bitline. Operation can be performing by different additional transistors.

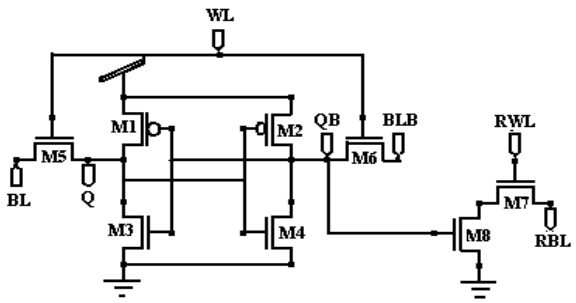


Figure2. Existing 8T SRAM Cell

To overcome the problem of data storage destruction during the read operation, an 8T-cell implementation was proposed, for which separate read/write bit and word signal lines are used as shown in Figure 2, to separate the data retention element and the data output element. In turn, the cell implementation provides a read-disturb-free operation.

V. Static Noise Margin

Although the extra two transistors have increased the size of the storage array by 20%, but instead of this should be able to see the benefits of the 8T unit: a read operation does not affect the contents in the cell [2].

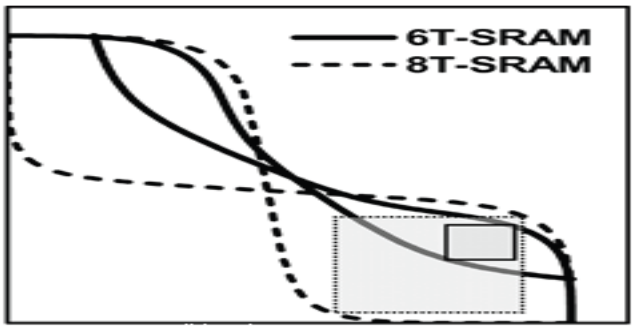


Figure3. Static noise margin

For a 6T cell, however, the worst-case static noise margin occurs in the read condition. In this case, the pass-gate disturbs the "0" storage node by pulling it up above ground, which significantly degrades the static noise margin. See Figure 3.

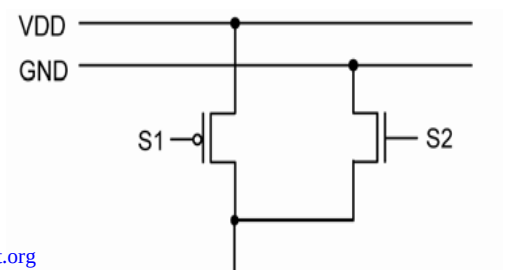
To overcome from large Power dissipation, using energy recovery circuit also known as adiabatic logic circuit. By using this type of circuit we can easily recover the energy and power which must be lost. Circuit are design in such a way that they useful for performing the functions [2].

VI. ENERGY RECOVERY LOGIC GATES

The recovery operation can be implemented if ideal charging and discharging paths are set up correctly. If every logic function primitive in the circuit is reversible, the controlling signal for the discharging path can be produced by an inverse logic gate [5].
To overcome from the problem of this power dissipation we used the techniques on the circuit called as energy recovery logic circuit, using this technique is become useful for power consumptions.

Many different ways the circuit can be plotted for example using NAND gate, transistors, inverters etc.

In this paper an energy recovery circuit is placed with 8T SRAM cell.



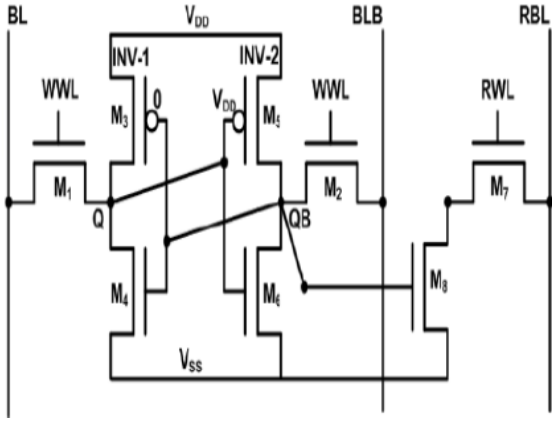


Fig.4. 8T SRAM USING ENERGY RECOVERY LOGIC

For low energy operation, a nanoscale SRAM circuit is approaching there are different technologies are adopted in this paper using 180 nm technology.

The proposed energy recovery SRAM circuit is shown in figure4. The proposed SRAM is structurally close to the conventional CMOS SRAM. The PMOS transistor connected between power line and Vdd and NMOS is connected to GND and Vdd. Operation is, first S1 and S2 are low so it connected to power line. Next S1 and S2 become high so that it connected to GND. Thus voltage decreases gradually to zero. Next S2 become low so that connection line is in a high-impedance state. In this both voltage level is different. After that energy recovery signal is input from bit line. While the input voltage increases, the other voltage depends on this circuit.

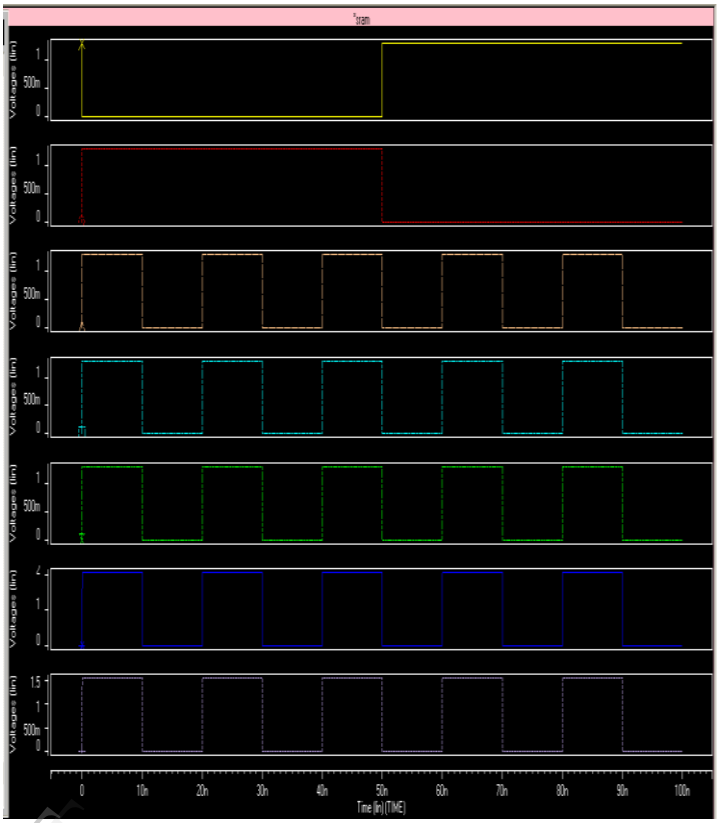


Figure5. Waveform of 8T SRAM using adiabatic logic

By this waveform read and write process can be done. PMOS is low then NMOS is high and bit line and word read line is high this shows that the read operation is performed. While using HSPICE, Waveform can be occurred through transient analysis. By using HSPICE Average power of the circuit, Delay etc can be find through cosmoscope. Considering about the technology there is different technology can be used . In this paper circuit are working on 180 nm technology.

VII. CONCLUSION

After the comparatively of 6T SRAM and 8T SRAM, although simulation shows that the write and read time is a little longer than 6T-SRAM, memory has significantly degrades the static noise margin than 6T-SRAM, and the read-operation does not need the pre-charge of the bit-line. In summary, 8T-SRAM can provide better stabilization, high speed and low power than 6T-SRAM. And while using energy recovery circuit power dissipation is less.

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REFERENCES

[1] Ajay Gadhe, Ujwal Shirode "Read stability and Write ability analysis of different SRAM cell structures" in International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 Vol. 3, Issue 1, January -February 2013, pp.1073-1078

[2] Nahid Rahman, B. P. Singh " Design of Low Power Sram Memory Using 8t Sram Cell" in International Journal of Recent Technology and Engineering (IJRTE) ISSN: 2277-3878, Volume-2, Issue-1, March 2013

[3] Narmada.S1, Pramod Kumar.T2, Obaleppa R Dasar1, Rajlaxmi Belavadi2, Prof.Rajani. in " Design and Physical Implementation of Asymmetric 8T-SRAM Memory Systems" The International Journal Of Engineering And Science (IJES) ||Volume||2 ||Issue|| 7 ||Pages|| 35-41||2013|| ISSN(e): 2319 – 1813 ISSN(p): 2319 – 1805 www.theijes.com The IJES Page 35

[4] Kai-ji Zhang*, Kun Chen,Wei-tao Pan, Pei-jun Ma "A research of Dual-Port SRAM cell using 8T" on 978-1-4244-5798-4/10/$26.00 ©2010 IEEE

[5] Yibin Ye and Kaushik Roy, Senior Member, IEEE "Energy Recovery Circuits Using Reversible and Partially Reversible Logic" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-I: FUNDAMENTAL THEORY AND APPLICATIONS, VOL. 43, NO. 9, SEPTEMBER 1996

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