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Analysis of 8-Bit Adder with CMOS & FS- GDI Techniques using Reversible Logic Gates

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Abstract - **The fast growth in modern electronics demands minimial power consumption in digital circuits. This led to the research of other logic techniques over traditional CMOS circuits. So, Reversible logic came in to existence as one of the solutions in which there is no information loss and no heat generation. Although, CMOS based reversible circuits reduce power but requires more transistors, increases switching power and not scalable. Among the other logic techniques like GDI(Gate Diffusion input), M-GDI(Modified - Gate Diffusion input) and FS-GDI (Full Swing-Gate Diffusion Input), The FS-GDI technique uses swing-restoration transistors to ensure full-voltage output levels while reducing transistor count. Cadence Virtuoso in 45nm technology is used to simulate and analyze each design. The results shows that the FS-GDI-based reversible adders consistently perform than CMOS based reversible designs for different bit widths. the proposed 8-bit reversible FS-GDI adder achieves approximately 21.0% improvement in power efficiency and 15.8% improvement in energy efficiency and a small increase in propagation delay is observed. Hence FS-GDI is a good approach for low-power reversible arithmetic circuits**.

Keywords: **Reversible Logic, CMOS, FS-GDI**

I. INTRODUCTION

As VLSI technology is continuously evolving, the need for designing digital circuits which can achieve high performance, consume low power and less area is increased. In the real world CMOS based circuits are used everywhere for its low static power, High integration density and high noise immunity but frequent switching leads to loss of energy in systems. These circuits converts many input patterns in to fewer output patterns destroying the data. So, the requirement for energy-efficient systems has become critical for arithmetic circuits, battery operated devices and large scale data centres. However, Reversible logic ensures that no information loss in system as it follows a one - one relationship between each input and output. this reduces the energy dissipation and can be adopted in future low power digital systems.

In irreversible logic based systems, the input cannot be recovered from the output. For example if there is a OR gate the output is '1' in all three cases for different combinations of 1 and 0 and It cannot be identified from which input the output is produced. But in reversible logic the number of inputs is equal to number of outputs. Each input corresponds to its output. And there is no feedback path from outputs. A reversible logic gate must be able to recover its original inputs from the outputs and the truth of a reversible logic gate must have unique input rows and output rows. Among the various reversible components, the reversible full adder plays an important role, as it performs addition which is widely used in arithmetic logic units, multipliers, and digital signal processing applications.

Eventhough reversible logic based CMOS circuits give clear theoretical benefits but it often results in inefficient designs with higher transistor count which increases over all power consumption of the circuit. To avoid these challenges, alternative transistor-level design techniques like GDI, M-GDI, FS-GDI techniques have been explored. The GDI technique works on a principle of applying inputs to source of PMOS, Source of NMOS and gate OF PMOS and NMOS. By changing these input signals, various Boolean functions can be implemented. though the power and area is reduced but fails to get full swing voltage levels. Similarly, M-GDI technique is the improved version of GDI method. In this method there is a small change that the body of PMOS is connected to VDD and the body of NMOS is connected to ground. It improves the voltage levels but cannot produce full voltage levels in all configurations. To address this issue, FS-GDI technique uses swing restoration transistors to improve the voltage swing of the circuit These transistors are placed as complementary transistors opposite to the circuit accordingly and this structure maintains reduced transistor count and low power dissipation

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while preserving full voltage levels across cascaded stages also. Hence, combining reversible logic with FS-GDI rather than CMOS provides an effective way for designing energy-efficient adders, making it well suited for multi stage and low power arithmetic circuits.

II. EXISTING WORK

The concept of low-power computing is based on Landauer's principle which states that "The amount of energy dissipated for every information bit loss is atleast kTln2 joules, where k is Boltzmann constant and T is temperature at which system operation is performed" It means each irreversible logic results in heat generation [1]. To overcome the limitations of irreversible computation, Parhami [2] explored reversible logic circuits which can be fault-tolerant, parity-preserving and can detect a error, Without extra hardware. This research is the foundation for the reversible arithmetic circuits with built-in fault tolerance.

Among all works, One such work is an optimal design of reversible parity-preserving full adder and full subtractor, presented by Kiran Kumar et al. in which gate count , quantum costs reduced and fault tolerance is improved. And the focus of this work is on gate- level optimization only [3]. On the transistor-level optimization side, other logic techniques like GDI is introduced by Morgenshtein [4]. This technique gives many Boolean functions reducing transistor count and power consumption. Another similar work by Morgenshtein, Shwartz, and Fish [5] confirms the implementation of GDI logic in nanoscale CMOS processes and can be used in modern fabrication technologies. The only limitation of GDI logic is degradation of voltage levels in outputs.

To address voltage swing degradation in GDI logic, Morgenshtein et al. [6] proposed the Full-Swing GDI (FS-GDI) technique. The carry look-ahead adder shows improved results compared to GDI and CMOS designs. This highlights FS-GDI as a scalable low-power logic style. Further Badry and Abdelghany [7], who designed a low-power adder using FS-GDI technique. Their results show decrease in power consumption and delay while maintaining strong voltage levels, On the other side, Islam et al. [8] synthesized fault-tolerant reversible logic circuits and observed reduce in delay for advanced adders such as carry look-ahead and carry skip adders. Another work, provides a comparative analysis of adder implementations using CMOS, GDI, Modified GDI, and FS-GDI was presented by Kumre [9]. It shows that FS-GDI is more consistent, achieve low power consumption and power-delay product. However, this study does not focus on reversible logic implementations.

From the reviewed literature and other works, it is understandable that reversible logic reduces energy dissipation, while GDI and FS-GDI reduce transistor count and power at the circuit level. However, most existing works treat these approaches independently. Reversible circuits are largely implemented using CMOS, are primarily applied to irreversible designs. This highlights a clear research gap in combining reversible logic with FS-GDI at the transistor level, particularly for scalable reversible arithmetic circuits.

III. METHODOLOGY

The methodology focuses on the design and implementation of a power-efficient full adder using two different approaches. In the first approach, the full adder is designed using reversible logic gates implemented with CMOS technology. In the second approach, the same reversible logic-based full adder is implemented using the FS-GDI technique. The 8-bit reversible Full Adder was designed and implemented using the FS-GDI technique in Cadence Virtuoso with 45nm CMOS technology and a 1.8V supply to each component. It was built by combining 1-bit full adder blocks to form 4-bit full adders, which were then cascaded to construct the full 8-bit unit. The design performs addition with improved power efficiency. Both designs are then compared and analyzed in terms of power consumption, delay, and overall performance to identify the most energy-efficient solution.

A full adder is a fundamental building block in digital systems, widely used in arithmetic logic units, multipliers, accumulators, and digital signal processing applications. Since addition is one of the most frequently executed operations, the efficiency of the full adder has a direct impact on overall system power consumption and performance. In reversible computing, the design of a power-efficient full adder is challenging due to constraints such as limited fan-out and the need to minimize garbage outputs. Conventional CMOS-based reversible full adders suffer from high transistor count and increased power dissipation, motivating the use of Full-Swing Gate Diffusion Input (FS-GDI) logic to achieve compact, low-power, and energy-efficient reversible full adder designs.

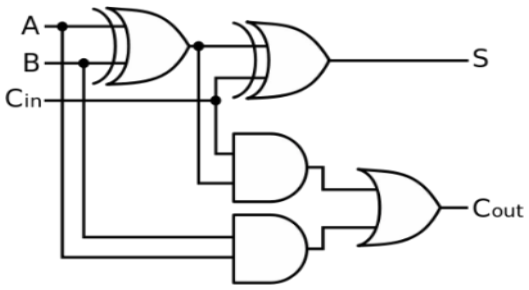

Fig 1: Circuit Diagram of Full Adder

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TABLE III
TRUTH TABLE OF FULL ADDER

Inputs			Outputs	
A	B	C	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

A. Design of Full adder using CMOS based reversible logic gates

A full adder is designed using two peres gates. The peres gate is a reversible logic gate implemented using CMOS buffer, AND gate and two XOR gates. For the first peres gate the inputs are B and A and one constant input '0'. By using this first peres gate first output generated is 'B' and it is a garbage output. The second output A⊕B is generated and is acts as primary input to second peres gate. The 'C' output generated as AB and is given to third input to second peres gate.

G1= B ------ (3.1)

For second peres gate, the secondary input is 'C'. The second Peres gate (P-2) generates an output A⊕B acts like primary input and it is a garbage output. and the other outputs are

Sum= A⊕B⊕C ---------- (3.2)

Carry=(A⊕B) C⊕AB ------- (3.3)

G2= A⊕B------(3.4)

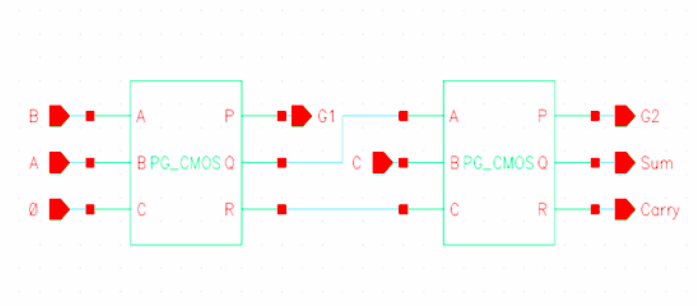

Fig 2: Schematic of Reversible Full Adder using CMOS Logic

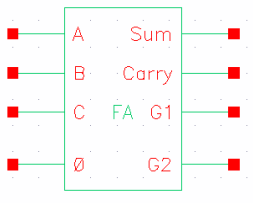

Fig 3: Symbol of Reversible Full Adder using CMOS Logic

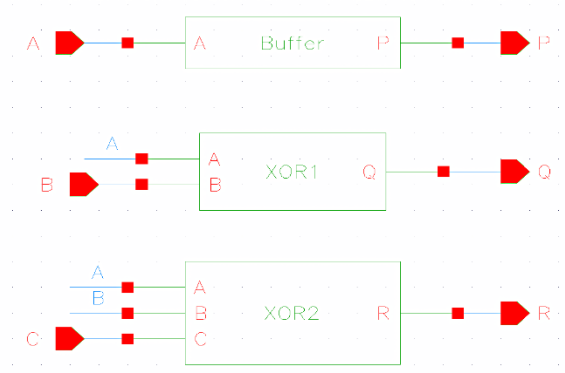

Fig 4: Schematic of PERES gate using CMOS logic gates

B. Design of Full adder using FS-GDI based reversible logic gates

A full adder is designed using two peres gates implemented using FS-GDI technique. The peres gate is a reversible logic gate implemented using FS-GDI buffer, AND gate and two XOR gates. For the first peres gate the inputs are B and A and one constant input '0'. By using this first peres gate first output generated is 'B' and it is a garbage output. The second output A⊕B is generated and is acts as primary input to second peres gate. The 'C' output generated as AB and is given to third input to second peres gate.

G1= B ------ (3.1)

For second peres gate, the secondary input is 'C'. The second Peres gate (P-2) generates an output A⊕B acts like primary input and it is a garbage output. and the other outputs are

Sum= A⊕B⊕C ---------- (3.2)

Carry=(A⊕B) C⊕AB ------- (3.3)

G2=A⊕B ------ (3.4)

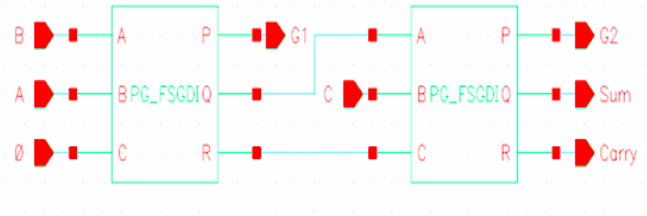

Fig 5: Schematic of Reversible Full Adder using FS-GDI Logic gates

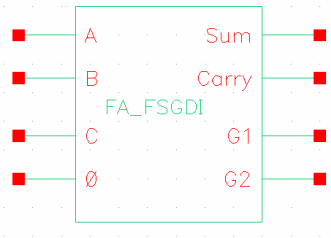

Fig 6: Symbol of Reversible Full Adder using FS-GDI Logic

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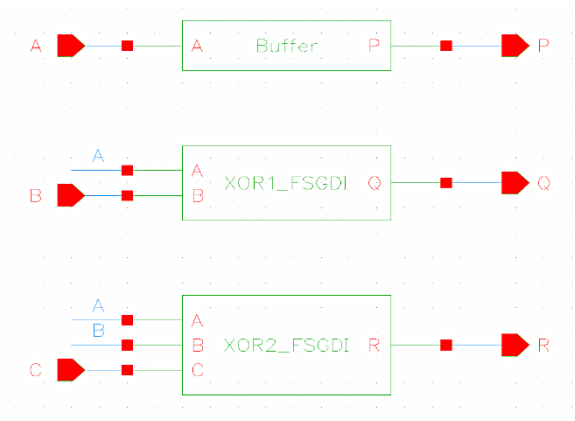

Fig 7: Schematic of PERES gate using FS-GDI logic gates

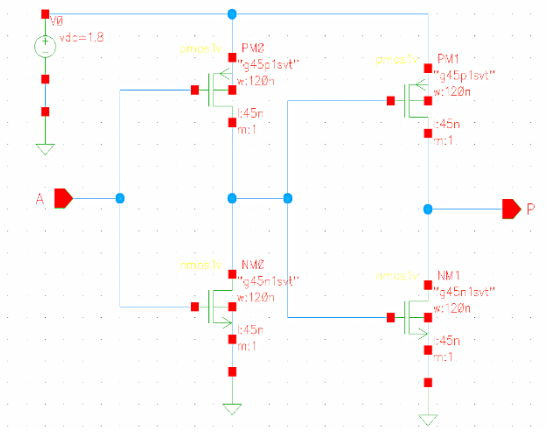

Fig 8: Schematic of Buffer Block

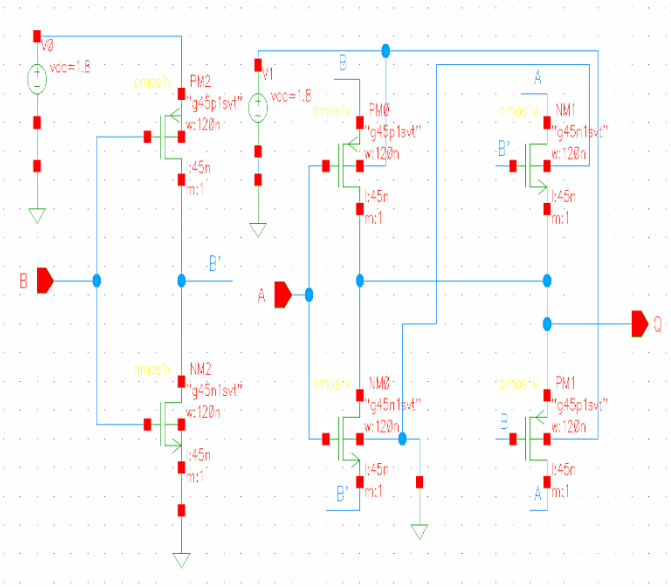

Fig 9: Schematic of XOR1 Block using FS-GDI Logic gates

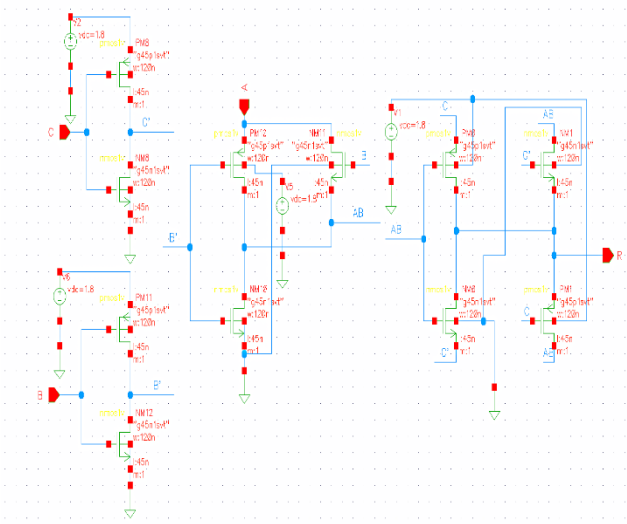

Fig 10: Schematic of XOR2 Block using FS-GDI Logic gates

C. Design of 4-Bit Adder using CMOS based reversible logic gates

The 4-bit reversible adder is designed using CMOS-based adder blocks connected in a cascaded manner as shown in Fig 11. The architecture consists of four identical FA units, each responsible for processing one bit of the input operands A and B along with a carry input. The first FA block receives inputs A0, B0, and an external carry-in (Cin), and generates the sum output S0 and a carry that is propagated to the next stage. Subsequent blocks compute sum outputs S1, S2, and S3 by adding the respective input bits with the propagated carry. This carry propagation follows a ripple-carry structure adapted to reversible logic. Constant inputs set to logic '0' are applied to each block to satisfy reversibility constraints and maintain a uniform design. Each FA block also produces garbage outputs to preserve the one to one mapping required for reversibility. The carry output shows the final carry of the 4-bit addition . This design represents efficient 4-bit addition while maintaining logical reversibility with conventional CMOS technology.

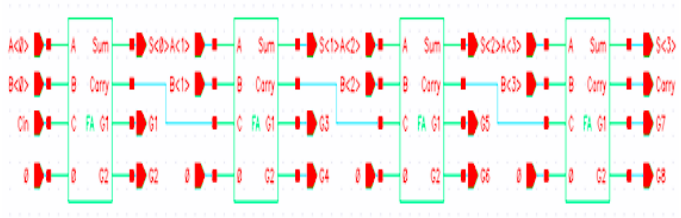

Fig 11: Implementation of 4- bit Reversible Adder using CMOS Logic

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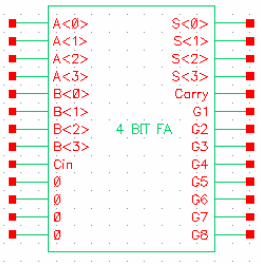

Fig 12: Symbol of 4- bit Reversible Adder using CMOS Logic

D. Design of 4-Bit Adder using FS-GDI based reversible logic gates

The 4-bit reversible adder is implemented by placing four identical FS-GDI based 1-bit reversible full adder blocks next to each other in a series as in Fig 14. Each FA block processes one bit from the input operands A and B along with Cin which is carry input, The first stage has inputs A0, B0, and Cin which generates the sum output S0 and a carry that is input to the second stage. Similarly, all other blocks give sum outputs S1, S2, and S3 by adding the respective input bits with the carry. This incoming carry in to each stage follows a ripple-carry structure . Constant inputs for each block are set to logic '0' and applied to each block to satisfy reversibility structure. Garbage outputs (G1-G8) are generated at every stage to preserve one-to-one mapping The carry output of last block represents the overall carry of the 4-bit addition. This design shows how FS-GDI-based reversible logic can be effective for low-power multi-bit arithmetic circuits.

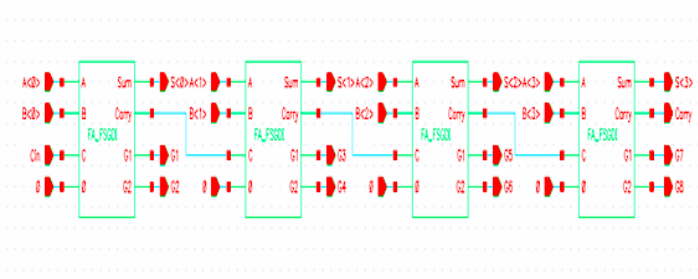

Fig 13: Implementation of 4- bit Reversible Adder using FS-GDI Logic

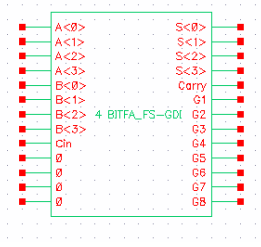

Fig 14: Symbol of 4- bit Reversible Adder using FS-GDI Logic

E. Design of 8-Bit Adder using CMOS based reversible logic gates

The 8-bit adder is developed using two identical 4-bit adder modules as shown in Fig 15. Each 4-bit module is implemented using CMOS based reversible logic gates, allows easy extension from smaller to larger adders. The circuit takes two 8-bit inputs. They are A0–A7 and B0–B7 which represents the operands A and B, along with an input carry-in (Cin) given to the least bit . The lower four bits computes the sum of A0–A3 and B0–B3 and produces outputs S0–S3 along with an internal carry. This carry is passed to the higher 4-four bits, which processes A4–A7 and B4–B7 and gives the sum outputs S4-S7 and the final carry output. Constant inputs set to logic '0' are used to support reversible gate operation . Garbage outputs are generated to preserve one-to-one input–output mapping, ensuring reversibility. The final outputs S0–S7 and the carry represent the complete 8-bit sum, indicating a low-power, modular, and arithmetic design.

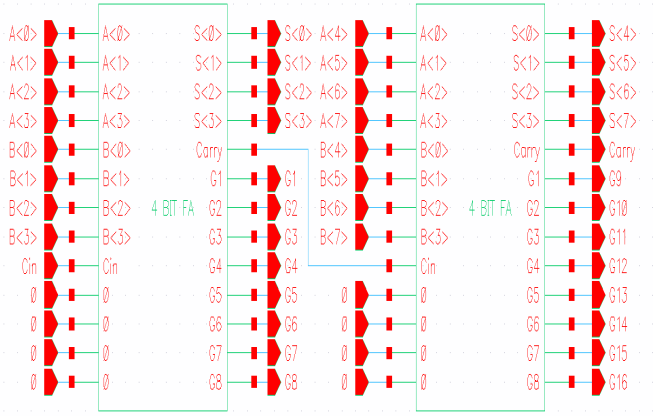

Fig 15: Implementation of 8- bit Reversible Adder using CMOS Logic

F. Design of 8-Bit Adder using FS-GDI based reversible logic gates

The below fig 16 represents the 8-bit adder which is designed using FS-GDI based two identical 4-bit adder blocks. Each 4-bit FA block accepts two 8-bit input operands A and B. each bit of input operand A is given as A0–A7 and the input operand B is given as B0–B7, along with an external carry-in (Cin). The lower 4-bit adder performs addition on bits A0–A3 and B0–B3 and generates outputs S0–S3 along with an internal carry. This carry is propagated to the higher 4-bit adder, which processes the sum of A4–A7 and B4–B7. Constant inputs in each block set to logic '0' are used to simplify the structure. Garbage outputs are produced to preserve one-to-one input–output mapping. The final outputs S0–S7 and carry out represent the 8-bit sum, demonstrating efficient and scalable arithmetic design.

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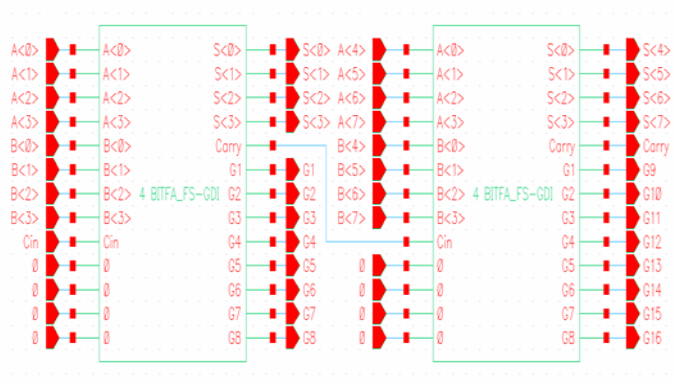

Fig 16: Implementation of 8- bit Reversible Adder using FS-GDI Logic

IV. RESULTS AND DISCUSSIONS

The evaluation of any logic design, especially one targeting reversible and low- power domains, must be based on several critical performance parameters. These include the number of gates used, power consumption, transistor count , the count of garbage outputs and constant inputs. these metrics are to be carefully simulated. All designs are simulated in Cadence Virtuoso using 45-nm technology and the full adder circuit outperforms previous designs[3] in all primary metrics.

Here is a comparative evaluation of transistor count between conventional CMOS and the FS-GDI designs. Transistor count is an important parameter that directly influences circuit complexity, silicon area and overall implementation cost. A reduction in transistor count generally leads to lower switching activity and improved power efficiency. The CMOS and FS-GDI architectures are analyzed for different bit configurations to understand their structural differences.

Table 2: Comparison of transistor count of CMOS designs and FS-GDI designs

CIRCUIT	CMOS	FS-GDI
INVERTER	2	2
BUFFER	4	4
AND	6	5
NAND	4	7
OR	6	5
NOR	4	7
XOR	14	6
XNOR	12	8
XOR1	14	6
XOR2	20	11
1 BIT FA	38	21
4 BIT ADDER	152	84
8 BIT ADDER	304	168

From the Table 2, It is observed that the FS-GDI technique requires fewer transistors than the conventional CMOS design. This reduction contributes to a more compact and area-efficient implementation. The minimized transistor usage also supports low power consumption and improved energy performance.

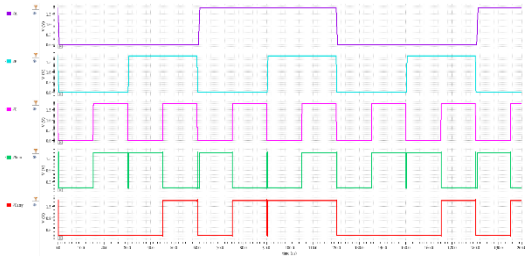

Fig 17: Results of Full Adder using CMOS reversible logic gates

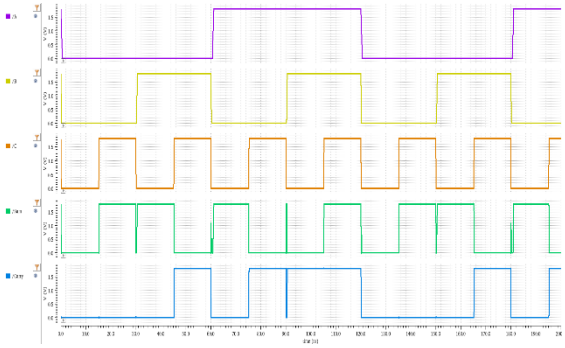

Fig 18: Results of Full Adder using FS-GDI reversible logic gates

From the Fig 17 and Fig 18, It is clear that The CMOS-based reversible full adder achieves correct reversible operation with an average power consumption of 1.4 µW and a propagation delay of 202ps, confirming stable signal flow and reliable logical behavior and The FS-GDI-based reversible full adder further improves power efficiency, consuming only 954.9 nW due to reduced transistor count and minimized switching activity. Although the FS-GDI design exhibits a slightly higher delay of 221ps, Comparative analysis shows a significant reduction in power consumption with FS-GDI compared to CMOS, with only a minor trade-off in speed.

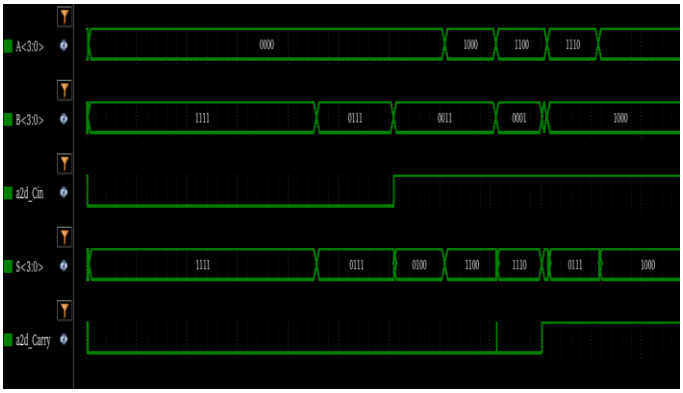

Fig 19: Results of 4-Bit Adder using CMOS Reversible Logic gates

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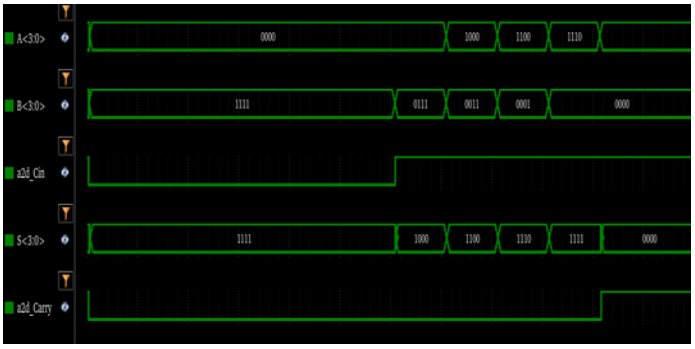

Fig 20: Results of 4-Bit Adder using FS-GDI Reversible Logic gates

From the Fig 19 and Fig 20, it is observed that The CMOS-based 4-bit reversible adder achieves correct reversible operation with an average power consumption of 3.768 µW and a propagation delay of 252.5ps, confirming stable signal flow and reliable logical behavior. The FS-GDI-based reversible adder further improves power efficiency, consuming only 3.214µW due to reduced transistor count and minimized switching activity. Although the FS-GDI design exhibits a slightly higher delay of 284.2ps, Comparative analysis shows a significant reduction in power consumption with FS-GDI compared to CMOS, with only a minor trade-off in speed.

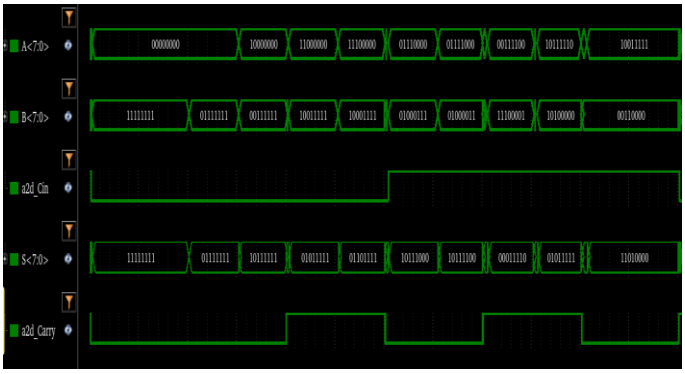

Fig 21: Results of 8-Bit adder using CMOS reversible logic gates

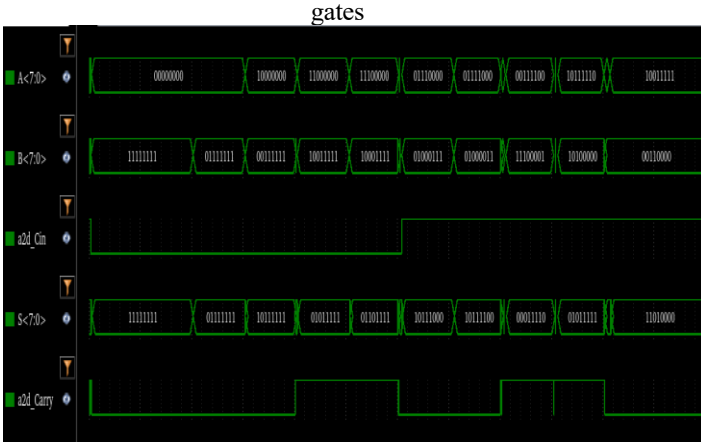

Fig 22: Results of 8-Bit adder using FS-GDI reversible logic gates

The CMOS-based 8-bit reversible adder achieves correct operation as shown in Fig 21 with an average power consumption of 8.762µW and a propagation delay of 362ps, confirming stable signal flow and reliable logical behavior. The FS-GDI-based reversible adder also achieves correct operation as shown in Fig 22 and further improves power efficiency, consuming only 6.922µW due to reduced transistor count and minimized switching activity. Although the FS-GDI design exhibits a slightly higher delay of 387ps, Comparative analysis shows a significant reduction in power consumption with FS-GDI compared to CMOS, with only a minor trade-off in speed.

Table 3: Comparison table of 1-bit reversible full adders using CMOS design and FS-GDI design

Property	CMOS design	FS-GDI design
Technology	45nm	45nm
Garbage Outputs	2	2
Power consumption	1.4µ	954.9n
Delay	202.1ps	221.3ps
Power Delay Product	2.83×10^{-16}	2.11×10^{-16}

Table 4: Comparison table of 4-bit reversible adders using CMOS design and FS-GDI design

Property	CMOS design	FS-GDI design
Technology	45nm	45nm
Garbage Outputs	8	8
Power consumption	3.768µ	3.214µ
Delay	252.5ps	284.2ps
Power Delay Product	9.51×10^{-16}	9.12×10^{-16}

Table 5: Comparison of 8-bit reversible adders using CMOS design and FS-GDI design

Property	CMOS design	FS-GDI design
Technology	45nm	45nm
Garbage Outputs	16	16
Power consumption	8.762µ	6.922µ
Delay	362ps	387ps
Power Delay Product	3.17×10^{-15}	2.67×10^{-15}

As shown in Table 3, the 1-bit FS-GDI reversible full adder provides a 31.8% reduction in power consumption and a 25.4% decrease in PDP, despite a slight increase in delay. Similarly, Table 4 indicates that the 4-bit FS-GDI adder improves power efficiency by 14.7% and reduces the power-delay product by 4.1%. In Table 5, the 8-bit FS-GDI design achieves a 21% reduction in power consumption along with a 15.8% improvement in PDP compared to the CMOS design. These

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improvements mainly result from the lower transistor count and reduced switching activity in the FS-GDI architecture, with only a minor delay trade-off.

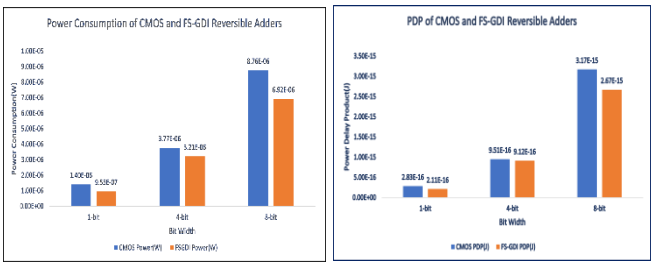

Fig 23: Power Consumption and PDP of CMOS and FS-GDI Based Reversible Adders

The above Fig 23 shows that FS-GDI reversible adders use less average power than CMOS designs for 1-bit, 4-bit, and 8-bit circuits, with the power savings increasing as the bit size grows. This indicates that FS-GDI logic is more effective in minimizing switching activity and overall power consumption and highlights that FS-GDI designs achieve lower Power–Delay Product (PDP) than CMOS, offering better energy efficiency even with a slight delay increase.

V. CONCLUSION

This paper presents the design and performance analysis of 1-bit, 4-bit, and 8-bit reversible adders using two methods which are CMOS-based reversible logic and the Full-Swing Gate Diffusion Input (FS-GDI) technique. The comparative analysis of all designs focuses on power consumption, propagation delay, and power–delay product (PDP). While CMOS based circuits give correct functionality, their higher transistor count and full-swing switching lead to increased power usage. In contrast, the FS-GDI approach reduces transistor count and switching activity resulting in lower power with slight increase in delay . Overall, the results show that FS-GDI-based reversible logic offers an energy-efficient and scalable solution for low-power arithmetic circuit design.

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