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Analysis and Design of Single phase Single Stage Integrated Converter to Improve Power Factor with Zero Voltage Switching

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***Abstract*: Now a day it is necessary to incorporate power factor correction in AC/DC front end converter modules as there is increase in usage of electronic devices like laptops, cell phone chargers, electric vehicles, UPS, etc. In this paper, a single phase high power factor ac/dc converter with soft switching characteristic has been described. The circuit topology is derived by integrating a boost converter and a buck converter. Boost converter takes care of front end power factor correction to acquire high power factor and to obtain low current harmonics at input line. Buck converter will take care of the output voltage regulation i.e it directs the dc-link voltage to give a steady stable dc output voltage. Without utilizing any active clamp circuit or snubber circuit, the dynamic switches of the proposed converter can accomplish zero-voltage switching on (ZVS) transition which is made in the circuit naturally. MATLAB13 has been used for simulating the circuit. The steady state analysis has been observed with different simulation circuits to get the desired performance output.**

Key words- PFC, Boost converter, Buck Converter, ZVS transition

I.INTRODUCTION

The power supply unit is a vital circuit obstruct in all electronic hardware. It is the interface between the ac mains and whatever is left of the useful circuits of the hardware. These utilitarian circuits as a rule need power at one or more fixed dc voltage levels. Switch mode power supplies (SMPS) are most regularly utilized for controlling electronic hardware since they give a practical, effective and high power density solution compared to linear regulators. The devices generally used in industrial, commercial and residential applications need to undergo rectification for their appropriate working and operation. They are associated with the grid including non-linear loads and subsequently have non-linear input characteristics, which results in production of non-sinusoidal line current. Likewise, current including frequency components at multiples of line frequency are observed which lead to line harmonics. Due to the increasing demand of these devices, the line current harmonics pose a major problem by degrading the power factor of the system thus affecting the performance of the devices. Consequently there is a need to lessen the line current so as to improve the power factor of the system. This has prompted outlining of Power Factor Correction circuits. Inferable from the advantages of basic circuit topology and easy control, boost or boost-buck converters have been generally served as power factor correctors. Keeping in mind the end goal to accomplish unity power factor, it requires the output voltage of both converter be higher than the amplitude of the ac line voltage. Hence, high-power factor ac/dc converters ordinarily comprise of two stages. The first is ac to dc stage which performs the function of PFC and the second one is a dc-to-dc stage used to supply regulated and stable dc voltage across the load.

In quest for high efficiency and high power factor, researchers have introduced numerous single-stage ac/dc converters taking into account the integration of a PFC stage and a dc to dc. By sharing may be a couple or dynamic switches, the single-stage methodologies have advantages of less count of components used, which is cost effective. As compared with two-stage approaches, the circuit efficiency is enhanced since only power conversion process is required. Among them, some single-stage methodologies incorporate a PFC converter with a full-ridge or half-bridge resonant converters. These resonant converters can work with ZVS if the resonant circuits present are inductive, i.e. the switching frequency is above the resonant frequency. In spite of the fact that, these topologies can effectively eliminate switching losses by switching the active switches near the resonance frequency to achieve ZVS, working active switches close to the resonance frequency results in high resonant current and more conduction losses. The significant issue is that the active switches normally operate at hard switching. An active switch that works at hard switching produces high switching losses as well as presents high voltage and current stresses on circuit components, bringing about poor efficiency and low circuit stability.

With a specific end goal to take care of the issue of hard switching, some soft switching techniques which include active clamp circuit or snubber circuit have been proposed. These soft switching techniques have considerably eliminated switching losses. Be that as it may, these strategies need to utilize additional switch, diode and receptive components to make the active switches turn on at zero-voltage. It includes the circuit complexity and general expense. In addition, another conduction losses coming about because of the circulating current in the active clamp circuit would happen.

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So as to eliminate the double circuit topology which makes the circuit complex, soft switching technique without active clamp circuit or snubber circuit, also to have high power factor with regulation of voltage, a new circuit topology is derived by integrating a boost converter and a buck converter. The boost converter performs the function of power factor correction (PFC) to get high power factor and low current harmonic at the input line. The buck converter further regulates the dc-link voltage to give a steady dc output voltage which results in high power factor with reduced circuit complexity, increased efficiency with regulated output voltage.

II. LITERATURE SURVEY

Mainly boost converters or Buck-boost converters are widely used as power factor correction converter [1-4]. There are two stages in power factor correction converter they are AC-DC conversion and DC-DC regulation [5-7]. As there are two energy converter stages there are switching losses, conduction loss and magnetic core loss.

The combination and cuk and sepic converters are used for PF correction and regulation [8-11]. But the boost and buck-boost, cuk and sepic has problem of hard switching due to parasitic capacitor. This happens at critical conduction mode. So the synchronous rectification is needed in these converters [12-13]. But by using this technique extra switch and control circuits are needed. Researches also proposed some single-stage approaches which integrate a PFC converter with a full-bridge or half-bridge resonant converters. These resonant converters can operate with ZVS if the resonant circuits present inductive, i.e. the switching frequency is above the resonant frequency. Moreover, ZVS can be achieved within a wide load range by variable-frequency control or asymmetrical pulse-width modulation (APWM) and also by active switching. The major problem is that the active switches usually operate in hard switching. An active switch that operates at hard switching not only generates high switching losses but also introduces high voltage and current stresses on circuit components, resulting in poor efficiency and low circuit stability. In order to solve the problem of hard switching, some soft-switching techniques which adopt active-clamp circuit or snubber circuit have been proposed [13-19]. These soft-switching techniques have substantially eliminated the switching loss. However, these techniques need to use additional auxiliary switch, diode and reactive components to make the active switches turn on at zero-voltage. It adds the circuit complexity and overall cost. Besides, another conduction losses resulting from the circulating current in the active- clamp circuit would happen.

In this project, a new ac/dc converter featuring ZVS with simple control is presented and analyzed.

III. SINGLE STAGE ACTIVE POWER FACTOR CORRECTION

There is a distorted input current waveform with increased harmonic content in the traditional off line converters with diode capacitor rectifier front-end. They can't meet neither the European line-current harmonic regulations characterized in the IEC1000-3-2 record or the comparing Japanese data consonant current determinations. To meet the necessities of above standards it is standard to include a power factor corrector in front of the separated dc/dc converter segment of the switching power supply. Again another dc/dc converter is required to get the regulated output voltage. In this way two converter is required for single-phase active power factor correction for the prerequisite of high input power factor and output voltage regulation. So, for single phase active power factor correction, there are two methodological approaches

(1) Two-stage approach
(2) Single-stage approach

Two-stage methodology is ordinarily utilized methodology as a part of high power applications. There are two independent power stages in two stage approach. The front-end PFC stage is normally a boost or buck-boost (or flyback) converter. The dc/dc output stage is the isolated one that is executed with no less than one switch, which is controlled by an independent PWM controller to firmly regulate the output voltage. The two-stage methodology is a financially a saving approach in high power applications; its cost-adequacy is lessened in low-control applications because of the extra PFC power stage and control circuits. A single stage plan joins the PFC circuit and dc/dc power conversion circuit into one stage. Various single-stage circuits have been accounted for lately. Contrasted with the two-stage approach, the single methodology uses stand out switch and controller to shape the input current and to regulate the output voltage. Despite the fact that for a single stage PFC converter attenuation of input current harmonics is not comparable to for the two-stage approach. Yet, it meets the necessities of IEC1000-3-2 standards. Again it is financially cost effective and conservative when compared to two stage approach.

IV. METHODOLOGY OF THE PROPOSED CONVERTER

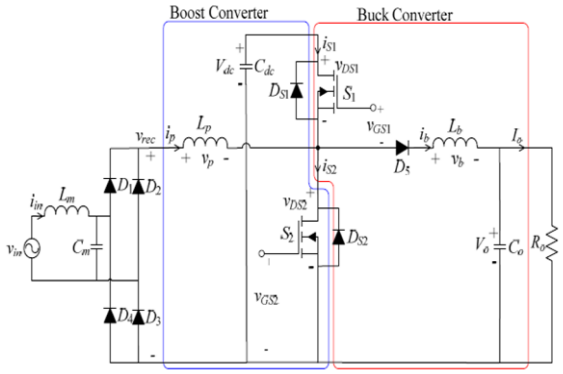

Fig.1 Circuit Diagram of Proposed converter

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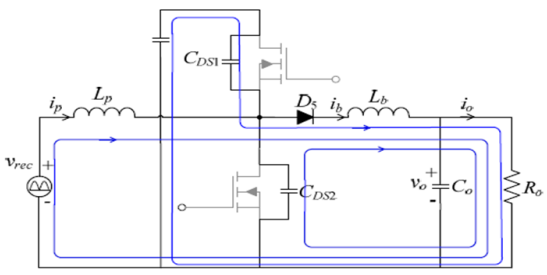
In order to solve the issue coming about because of hard switching, another ac/dc converter is proposed. The circuit topology is inferred by relocating the positions of the semiconductor switches. Here, MOSFETs S1 and S2 are the active switches and the antiparallel diodes DS1 and DS2 are their intrinsic body diodes, respectively. The proposed circuit mainly comprises of a low-pass filter (Lm and Cm), a diode-bridge rectifier (D1-D4), a boost converter and a buck converter. The boost converter is made out of Lp, DS1, S2 and Cdc and the buck converter is made out of Lb, D5, DS2, S1 and Co. Both converters work at a high-switching frequency, fs. The boost converter performs the function of PFC. When it works at discontinuous conduction mode (DCM), the average value of its inductor current in each high-switching cycle is approximately a sinusoidal function. The low pass filter is utilized to remove high frequency current of the inductor current. By this, the boost converter can wave shape the input line current to be sinusoidal and in phase with the input line voltage. In other word, high power factor and low current harmonic distortion (THDi) can be accomplished. The buck converter further directs the output voltage of the boost converter to supply stable dc voltage to the load. It is likewise designed to operate at DCM for achieving ZVS in light of the reason that will be discussed about it at the final this section.

vGS1 and vGS2 are the two gate voltages from a half-bridge driver integrated circuit (IC) are utilized to turn S1 and S2 on and off. These voltages are complementary rectangular-wave voltages. In order to keep both active switches not to cross conduct, there is a short non-overlap time characterized as "dead time". In the dead time, vGS1 and vGS2 are at a low level. The duty cycle of vGS1 and vGS2 is 0.5 by neglecting the short dead time.
For simplifying the circuit analysis, the following assumptions are made:
1) The semiconductor devices are ideal except for the parasitic output capacitance of the MOSFETs.
2) The capacitances of Cdc and Co are large enough that the dc-link voltage Vdc and the output voltage Vo can be regarded as constant.

Principle of Operation

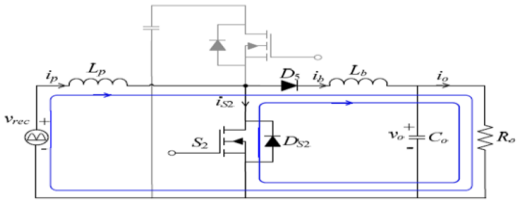
Mode I (t0-t1)



(a)

Preceding Mode I, S1 is at "ON" state. The boost inductor current ip is zero and the dc-link capacitor supplies the buck inductor current ib which moves through S1, D5, Lb and Co. This mode begins when S1 is turned off by the gate voltage, vGS1. The time interval of this mode is the turn-off transition. At the start of this mode, ib is redirected from S1 to flow through the output capacitors CDS1 and CDS2. CDS1 and CDS2 are charged and discharged, respectively. As the voltage across CDS2 (vDS2) reduces to be lower than the rectified input voltage vrec, the boost inductor current ip begins to increaes. At the point when vDS2 comes to - 0.7 V, DS2 turns on and Mode I ends.

Mode II (t1-t2)



(b)

At the beginning of Mode II, voltage vDS2 is maintained at about -0.7 V by the antiparallel diode DS2. After the short dead time, S2 is turned on by the gate voltage, vGS2. If the on-resistance of S2 is small enough, most of ib will flow through S2 in the direction from its source to drain.
Neglecting this small value of vDS2, the voltage across Lb and Lp are equal to

$$v_b(t) = -V_o \qquad (1)$$

$$v_p(t) = v_{rec}(t) = V_m \sin\{(2\Pi f_L t)\} \qquad (2)$$

where fL and Vm are the frequency and the amplitude of the input line voltage, respectively. Since the time interval of Mode I is very short, ib can be expressed as

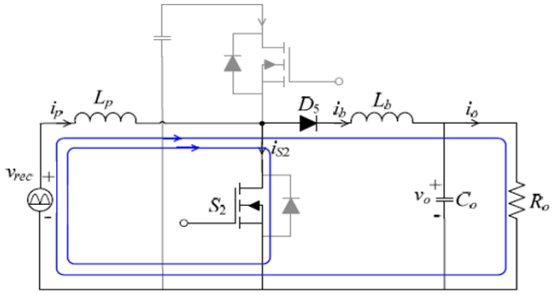
$$i_b(t) = i_b(t_0) - \frac{V_o}{L_b}(t - t_0) \qquad (3)$$

From (3), ib decreases from a peak value. The boost converter is designed to operate at DCM, therefore ip increases linearly from zero with a rising slope that is proportional to vrec.

$$i_p(t) = \frac{v_{rec}}{L_p}(t - t_0) = \frac{V_m \left|\sin(2\pi f_L t)\right|}{L_p}(t - t_0) \qquad (4)$$

In Mode II, ib is higher than ip. Current ib has two loops. Parts of ib flow through S2 and the rest are equal to ip and flow through the line-voltage source, diode rectifier and Lp. This mode ends when ip rises to become higher than ib.

Mode III (t2-t3)



(c)

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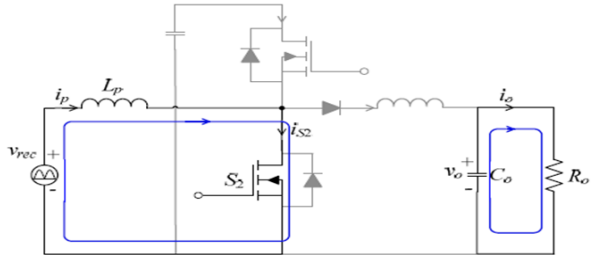
In Mode III, ip is higher than ib. Current ip has two loops. Parts of ip are equal to ib and flow into the buck converter, while the rest flow through S2. The current direction in S2 is naturally changed, i.e. from drain to source. The voltage and current equations for vb, vp, ib and ip are the same as (1) – (4). Current ib decreases continuously. On the contrary, ip keeps increasing. Since the buck converter is designed to operate at DCM, ib will decrease to zero at the end of this mode.

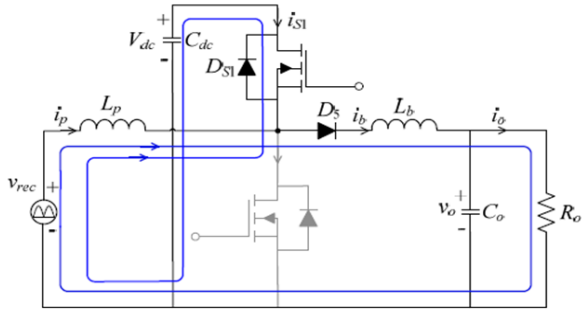
Mode IV (t3-t4)



(d)

In this mode, S2 remains on to carry ip. Beacuse ib is zero, the buck converter is at "OFF" state and the output capacitor Co supplies current to load. When S2 is turned off by the
gate voltage vGS2, Mode IV ends.

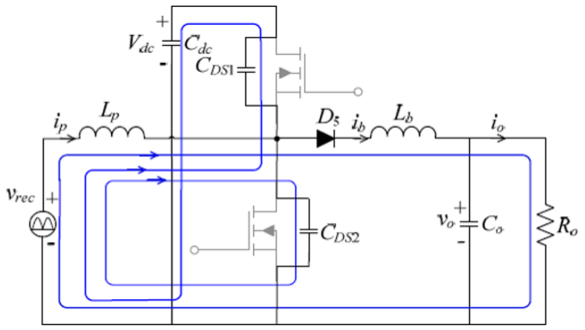
Mode V (t4-t5)



(e)

Current ip reaches a peak value at the time instant of turning off S2. For maintaining flux balance in Lp, ip will be diverted from S2 to flow through CDS1 and CDS2 when S2 is turned off. CDS1 and CDS2 are discharged and charged, respectively. Current ib is zero at the beginning of this mode, and will start to increase when the voltage across CDS1 (vDS1) decreases to be lower than Vdc-Vo, that is the voltage across Lb becomes positive. As vDS1 reaches -0.7 V, DS1 turns on and Mode V ends.

Mode VI (t5-t6)



(f)

At the beginning of Mode VI, vDS1 is maintained at about -0.7 V by the antiparallel diode DS1. After the short dead time, S1 is turned on by vGS1. If the on-resistance of S1 is small enough, most of ip will flow through S1 in the direction from its source to drain. Neglecting this small value of vDS1, the voltage imposed on Lp and Lb can be respectively expressed as

$$v_p(t) = v_{rec}(t) - V_{dc} = V_m\left|\sin(2\pi f_L t)\right| - V_{dc} \qquad (5)$$

$$v_b(t) = V_{dc} - V_o. \qquad (6)$$

For a boost converter, the dc-link voltage Vdc is higher than the rectified voltage vrec. Neglecting the short turning off transition of S2, ip can be expressed as:

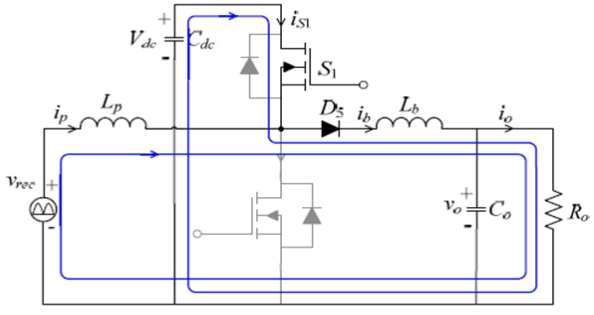
$$i_p(t) = i_p(t_4) - \frac{V_m\left|\sin(2\pi f_L t)\right| - V_{dc}}{L_p}(t - t_4) \qquad (7)$$

On the contrary, the voltage across Lb is positive to make ib rise from zero.

$$i_b(t) = \frac{V_{dc} - V_o}{L_b}(t - t_4) \qquad (8)$$

In Mode VI, ip is higher than ib. There are two loops for ip. Parts of ip flow through S1 to charge the dc-link capacitor Cdc and the rest are equal to ib and flow into the buck converter. This mode ends when ib rises to become higher than ip.

Mode VII (t6-t7)



(g)

In Mode VII, ib is higher than ip. There are two loops for ib. Parts of ib are equal to ip and flow into the boost converter, while the rest flow through S1. The current direction in S1 is naturally changed, i.e. from drain to source. The voltage and current equations for vp, vb, ip and ib are the same as (5) – (8). Current ib increases

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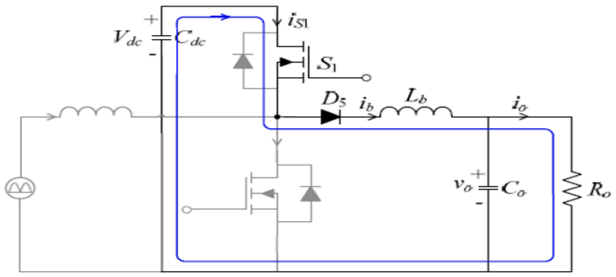
continuously while ip keeps decreasing. The circuit operation enters next mode as soon as ip decreases to zero.

Mode VIII (t7-t8)



(h)

S1 remains on and ib keeps increasing. This mode ends at the time when vGS1 becomes a low level to turn off S1 and, the circuit operation returns to Mode I of the next high frequency cycle.

Based on the circuit operation, prior to turning on one active switch, the output capacitance is discharged to about 0.7 V by the inductor current. Then the intrinsic body diode of the active switch turns on to clamp the active voltage at nearly zero voltage. By this way, each active switch achieves ZVS operation.

The reason for operating the buck converter at DCM is explained below. In operation Mode II, ip rises and ib decreases. It should be noted that ip rises in proportional to the input voltage and has a small peak in the vicinity of zero-cross point of the input voltage. If the buck converter is operated at continuous-conduction mode (CCM), ib could keep higher than ip. On this condition, the circuit operation would not enter into Mode III and Mode IV, and vDS1 is maintained at about Vdc. When S1 is turned on, ib is diverter from S2 to S1. CDS1 is discharged at a high voltage of Vdc, resulting a spike current and high switching losses.

V. SIMULATION RESULTS AND DISCUSSION

To verify the validity of the proposed single phase integrated high power factor, a well-known MATLAB 2013 has been used to carry out simulation process. Simulation has been done for open loop and closed loop simulation. Along with this, proposed circuit has been made to work with two loads in a single circuit which is advantageous.

The values calculated from the derived equations are listed in Table 1

Filter Inductor L_m	2.16 mH
Filter Capacitor C_m	0.47 µF
Boost Inductor L_p	0.76 mH
DC-Link Capacitors C_{dc}	100 µF
Buck Inductor L_b	2.14 mH
Buck Capacitor C_o	100 µF
Active Switches S_1, S_2	IRF840
Diodes D_5	MUR460

Table 1

1) (a) Simulation Circuit of proposed converter in open loop condition

In figure 2, the complete simulation diagram is being shown in open loop condition. The converter circuit operation have two functions where the rectified dc output voltage fed to the proposed converter and it functions for power factor correction when the circuit is operating in boost mode, a regulated stable dc output voltage can be observed across the output when the circuit is operating in buck mode.

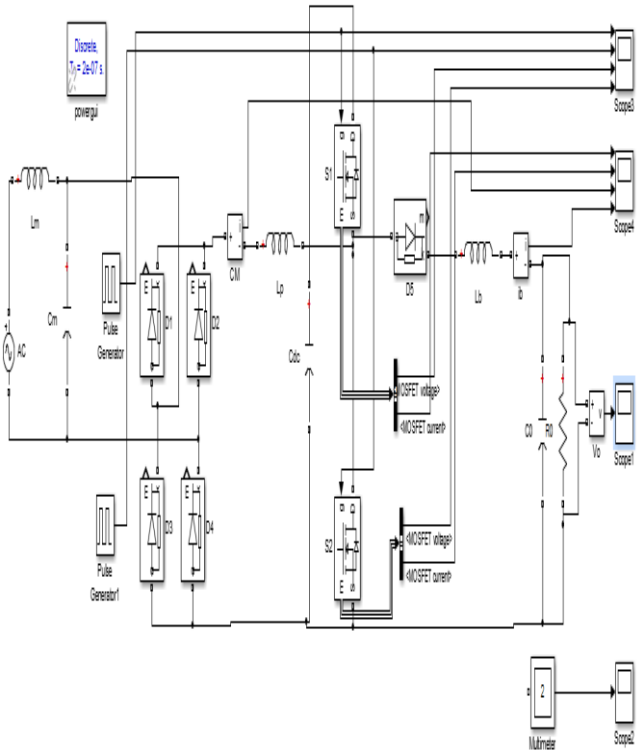


Figure 2.1 Simulation circuit of the proposed converter
In open loop condition

(b) Simulated output waveforms

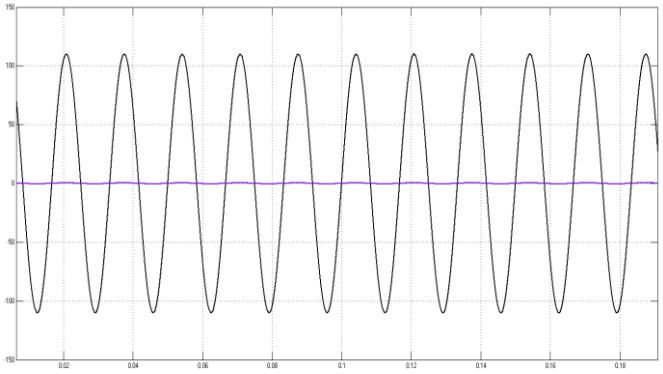


Figure 2.1(a) Input Phase voltage and current

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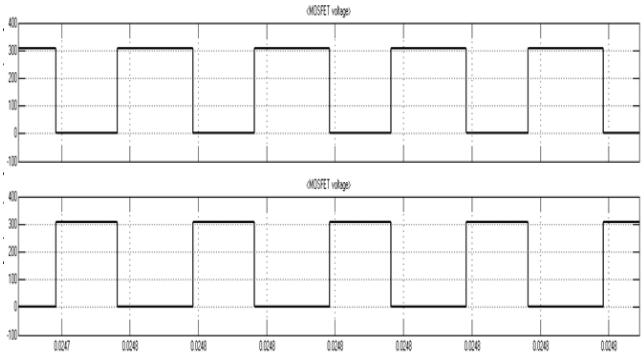

Figure 2.1(b) Voltage VDs1 and VDs2 of Diodes Ds1 and Ds2

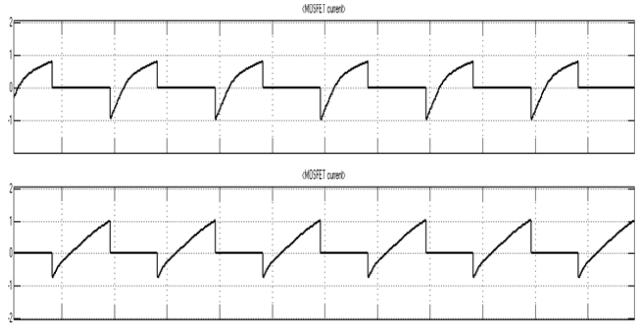

Figure 2.1(c) Current waveforms of Switches S1 and S2

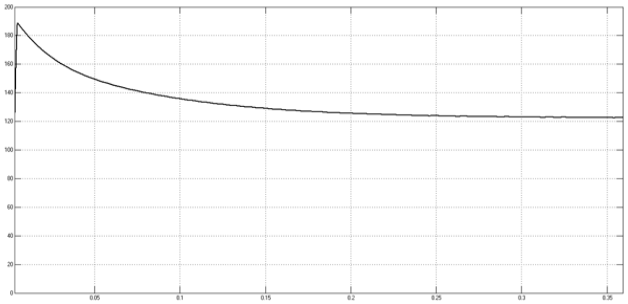

Figure 2.1(d) Regulated output voltage, Vo= 122V

2) Closed Loop Simulation circuit of Proposed Converter

Figure 2.2 shows the complete simulation circuit of proposed converter which can be divided into main circuit and the controller circuit which forms the closed loop simulation circuit.

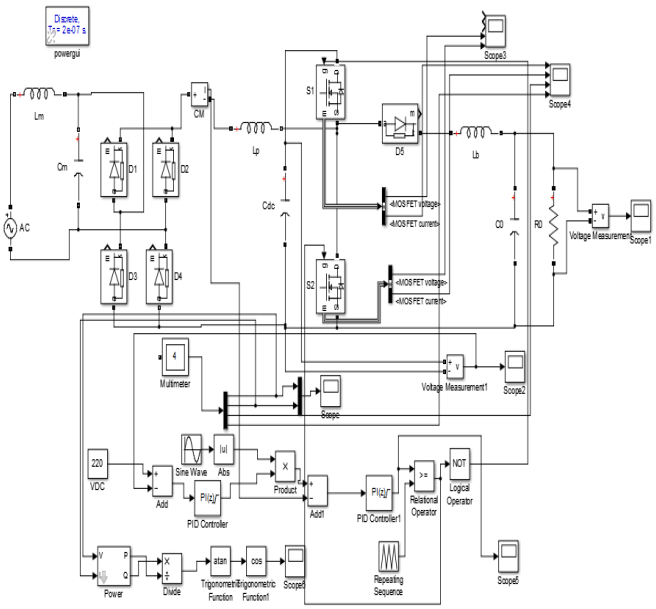

Figure 2.2: Closed loop simulation circuit

(b) Simulated waveforms for closed loop

The simulated waveforms for the closed loop have been shown in figures 2.2(a), 2.2(b), 2.2(c) and 2..2(d).

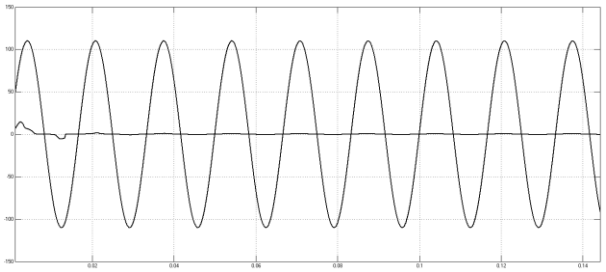

Figure 2.2(a): Input voltage and current waveforms in phase

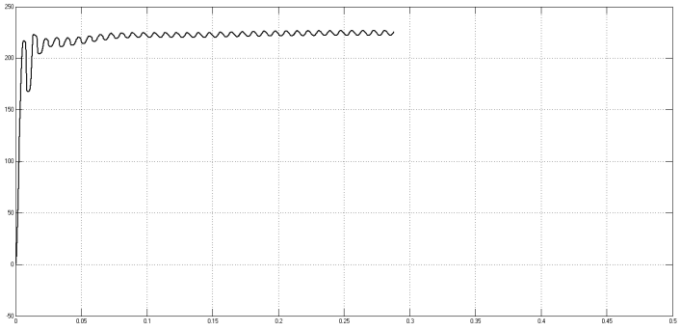

Figure 2.2(b) : Constant DC output performance of closed loop simulation

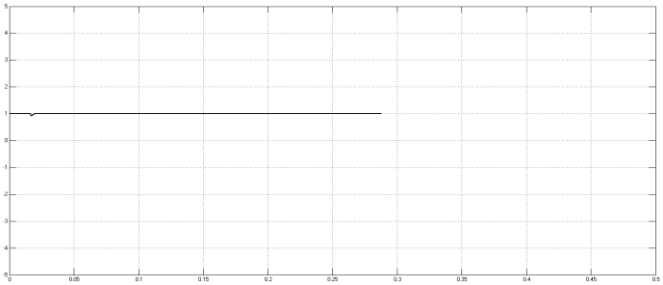

Figure 2.2(c): Graph showing Unity power factor

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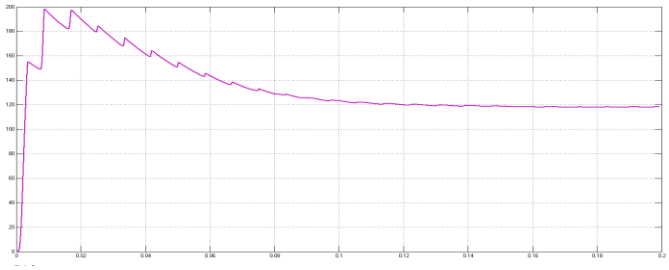

Figure 2.2(d) Regulated dc output voltage, Vo=120V

3) (a) Simulation of the proposed converter used for two different loads in this single stage approach

In this simulation circuit, for the proposed converter two different loads can be used across the boost mode and the buck mode in which a single stage approach circuit is capable to handle two different loads at a same time.

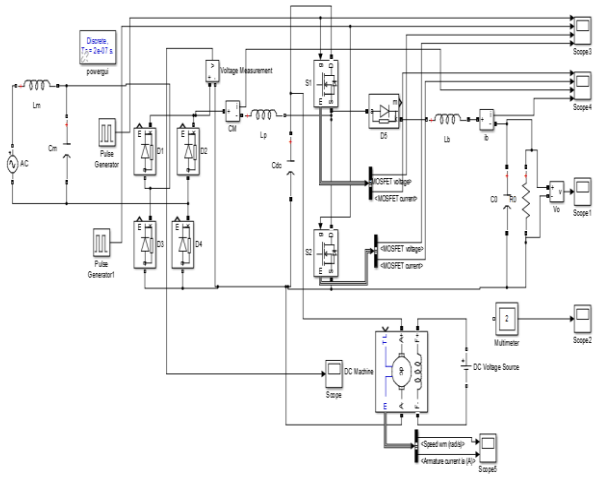

Figure 2.3 Simulation of the proposed converter used for two different loads in this single stage approach

(b) Simulated Waveforms for proposed converter with two different loads

Below figures show the simulated waveforms for the proposed circuit for the circuit works for two different loads

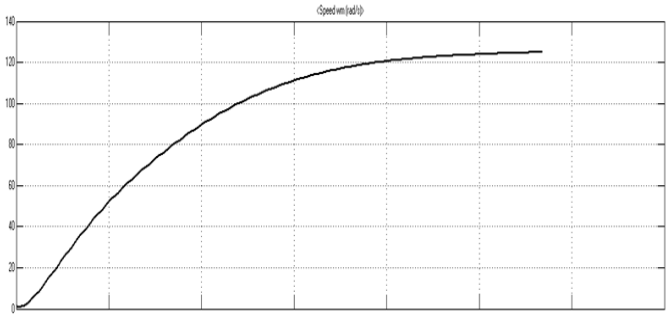

Figure 2.3(a) Graph of speed linearly increased w.r.t time

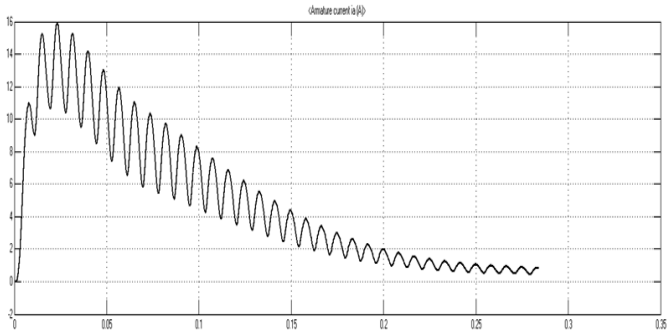

Figure 2.3(b) Graph of Armature current gradually decreased with increase in speed

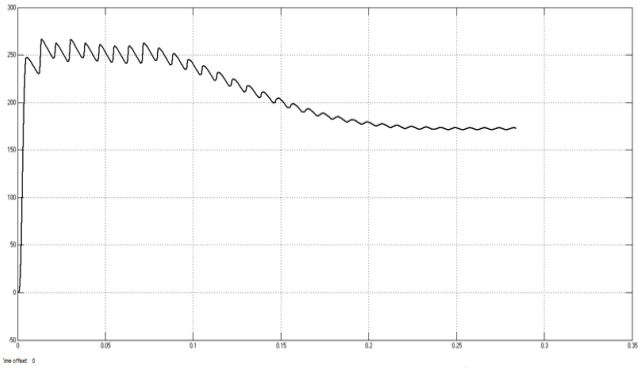

Figure 2.3(c) Regulated Dc output voltage of Vo= 180V

VI. CONCLUSION

From the simulation results of the open loop condition we observe that input current is in phase with the voltage so that the input line current harmonics has got reduced with high power factor. ZVS operation is achieved. Also the regulated output voltage has got settled after some time with a stable dc output voltage of 122V. From the simulation results of the closed loop condition we observe that input current is in phase with the voltage so that the input line current harmonics has got reduced with unity power factor. ZVS operation is achieved. Due to the controller, a constant voltage across Cdc i.e Vdc is achieved which is equal to 220V. Also the regulated output voltage has got settled after some time with a stable dc output voltage of 120V. For the proposed converter two different loads can be used across the boost mode and the buck mode in which a single stage approach circuit is capable to handle two different loads at a same time. Armature current and speed characteristics are shown in below figures 2.3(a) & 2.3(b). A regulated dc output voltage can also be observed across the resistive load as shown in figure 2.3(c).

From all the simulation results we can conclude that the proposed converter has achieved high power factor with less input harmonic current which is done by boost mode, the buck mode has given the dc regulated output voltage across the load. With this both circuits by operating in DCM mode have achieved ZVS transition there by eliminating the switching losses.

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