Analysis and Design of Quantum-Dot Cellular Automata

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Abstract— Quantum Dot Cellular Automata are proposed Models of Quantum Computation. Wire Crossing is an issue in Quantum Dot Cellular Automata (QCA) Design. Configurations of Such Wires can form a complete set of Logic Gates for Computation. We discuss about the QCA Basics and Logic design of QCA Majority Gate, QCA OR Gate, QCA AND Gate, QCA Inverter Gate, QCA NAND Gate. The circuit was simulated with QCA Designer and results were included in this paper. QCA an attractive technology for manufacturing memories in which the paradigm of memory-in-motion can be fully exploited. We can implement memory architecture for QCA implementation i.e. the RAM cell.

Index Terms— Quantum Dot cellular automata (QCA), QCA Architecture, QCA Design, QCA Simulation, QCA Majority Gate, QCA OR Gate, QCA AND Gate, QCA Inverter Gate, QCA NAND Gate.

I. INTRODUCTION

*Q*uantum-Dot cellular automata (QCA) is a new technology for nano electronic computers. It provides high density, high switching speed, and ultralow power dissipation. Quantum dot cellular automata are proposed models of quantum computation, which have been devised in analogy to conventional models cellular computation introduced by Von Neumann order to implement a system that encodes information in the form of electron position it becomes necessary to construct a vessel in which an electron can be trapped and counted as there or not there. A quantum dot does just this by establishing a region of low potential surrounded by a ring of high potential. Such rings are able to trap electrons of sufficiently low energies/temperature and are sometimes called potential wells. A cellular automata is a finite state machine consisting of a uniform (finite or infinite) grid of cells. Each cell can be in only one of a finite number of states at a discrete time. As time moves forward, the state of each cell in the grid is determined by a transformation rule that factors in its previous state and the states of the immediately adjacent cells. Grid arrangements of quantum-dot cells behave in ways that allow for computation. The simplest practical cell arrangement is given by placing quantum-dot cells in series, to the side of each other. Configurations of such wires can form a complete set of logic gates for computation. Uses electrons in cells to store and transmit data Electrons move between different positions via electron tunneling and logic functions performed by Coulombic interactions. Two extra electrons are introduced to the quantum cell. Electrons have the ability to tunnel from one quantum dot to the next. Repelling force of electrons moves the charge to opposite corners of the quantum cell, resulting in two possible arrangements, representing binary 0 and 1. Quantum dots will become the backbone of future microelectronic and photonic devices because of their unique properties due to quantum confinement of electrons in 3-dimensions this results in interesting electronic and optical properties. The application of quantum dots are Neuro-quantum structures, Single-electron devices, for instance transistor, Tunable lasers, Photo detectors, Sensors, Quantum Computing, Quantum Cellular Automata. QCA an attractive technology for manufacturing memories in which the paradigm of memory-in-motion can be fully exploited. We can implement memory architecture for QCA implementation i.e. the RAM cell. Quantum-Dot cellular automata (QCA) is a new technology for nanoelectronic computers. It provides high density, high switching speed, and ultralow power dissipation.

II. QCA ARCHITECTURE

A. QCA Design

QCA cell is a nanostructure device where electrons wells which confine electrons store the logic states and transmit information .A cell is composed of four quantum dots where each states contain one single electron per dot. Four dots are located at the corners of the cell. And two extra electrons are injected into the cell. The cell is charged with two extra electrons which tend to occupy diagonally opposite dots due to columbic repulsion. Unlike conventional logic where information transfers by electrical current, QCA connects the state of one cell to the state of its neighbors by columbic interaction. There are two possible arrangements denoted as cell polarization P=-1 which denotes logic "0" and P=+1 which denotes logic "1"(fig.1), binary information can be encoded. Clock in QCA based circuits is used to synchronize and to control the information flow as well as provides the power to run the circuits. There are propagation delays between the cell to cell reactions so that there should be a limit in count clock zone which ensure the proper propagation and also reliable transmission.
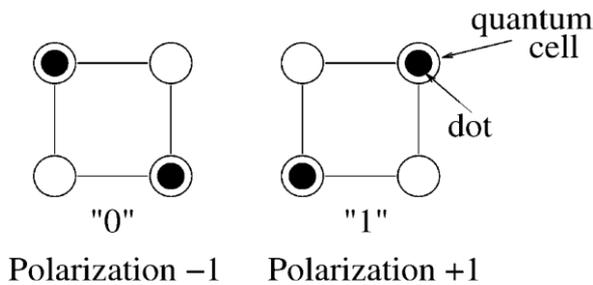
Fig.1

The numbering of the dots in a cell happens in a clockwise manner starting from the dot on the top right: top right dot i =1, bottom right dot i =2, bottom left dot i =3 and top left dot i =4. A polarization P in a cell is defined as where ρ_i denotes the electronic charge at dot i. The polarization measures the charge configuration that is, the extent to which the electronic charge is distributed among the four dots.

$$P = \frac{(p1 + p3) - (p2 + p4)}{(p1 + p2 + p3 + p4)}$$

III. QCA SIMULATION DESIGN TOOL

A. QCA Simulations

"Ab initio" simulations of QCA cells provide very accurate results for atmost about two interacting QCA cells. Because of the computational complexity involved, more cells cannot be added to the simulation without increasing the required simulation time beyond practical limits. For this reason, when simulating a larger number of cells, other simulation methods that employ approximations must be used to simplify the calculations. There are many different models that can be generally counted on to give reasonably accurate results for specific aspects of QCA operation. For instance, QCA designer which is a tool used to simulate clocked 4-dot QCAs, uses two different simulation engines, each having its own pros and cons. Both models can provide reasonably accurate simulations, however, due to certain approximations may not provide accurate results each time. One important approximation that both these models make is that the clocked 4-dot QCA are two-state systems. Generally this is true; however, this simplification can produce inaccurate results due to ambiguous cell configurations. Regardless of these possibilities, the QCA designer tool provides a good general tool to study logic designs of 4-dot QCA.

B. New QCA Simulation Tools

Since the QCA designer tool does not allow use of clocked QCA, a new design and simulation tool has been developed specifically to understand the unique logic of a QCA system. Fortunately, the simulation development for the QCA cells benefits from the relative simplicity of the design compared to the 4-dot QCA cells, as well as the past development of different simulation methods for the QCA cell. These factors preclude the immediate need for full ab initio simulation of properties, such as the cell-to-cell response for the QCA cells, and allow simulation to.

Focus on the logical output of groups of QCA cells. To choose which simulation techniques to use for the purposes of this study, key requirements were identified. First, the ground state of a system of QCAs must be known in order to provide the correct logic operation of a circuit and enable design of a logic library. This proved to be the most important requirement of the simulation engine. Another factor involved in determining requirements for the simulation design was that separation between the ground state of the system and the first excited states would be studied to determine robustness of the design. And lastly, but also a key requirement, is that, it is common for QCA configurations to produce circuits that have degenerate ground state configurations, and many times these different configurations produce opposite outputs. In an actual system, the circuit output in these cases would only be determined by noise, fabrication defect, or other random element, which are generally uncontrollable and, therefore, undesirable. Therefore, these degenerate cases were identified so they could be excluded from the library of 4-dot QCA logic constructs after several simulation techniques were studied, and based on these main requirements, the semi classical time-independent simulation techniques developed in were selected to drive the new simulation and design tool created for this study. This technique assumes the behavior of the electrons in the QCA to be classical except for the ability to tunnel between QDs. This becomes a reasonable approximation if the electron wave functions can be considered to be strongly localized (a reasonable assumption considering the desirable bistable behavior of QCA cells). The simulation operates by computing the energies of each combination of all of the QCA cell logic states (0 or 1) by computing the sum of the electrostatic contributions of point charges to the energy for each configuration such that

$$E = \sum_{(i \neq j)} \frac{q_i q_j}{4\pi \varepsilon_0 \varepsilon_r r_{ij}}$$

Where E is the total system energy, q are the charges, ε_0 ε_r is the permittivity, and r is the distance between point charges. The configuration with the lowest total energy produced the ground state of the system and resultant correct logic output of the circuit. When degenerate ground-state configurations were identified, they were examined to determine if different logical outputs were produced by the degenerate states. If the outputs were the same in each of the degenerate states, the circuit was maintained as an acceptable circuit; if not, then the circuit output was deemed to be random, from a logical sense, and thus unacceptable. The results of this process are the logical constructs that will be presented in the following section and that may be used in a qca-based design.

IV. LOGIC DESIGN USING QCA DESIGNER

A. Binary wire

The first of a group of simple logic constructs is the binary wire. The wire consists of a string of like-oriented QCA with the adjacent opposite oriented sites uninhabited by QCAs. During switching, each QCA passes the information to its

adjacent QCA cell, starting at the input QCA and continuing throughout the wire.

B. Inverter

The next simple logic construct to be introduced is the inverter. There are at least two ways to invert a signal in the QCA architecture. For the first way, one oppositely oriented QCA is placed in a position next to the binary wire between two like-oriented QCAs. This QCA, in turn, passes the information on to the next QCA except now the binary information is inverted. This inverter can be seen. The second way to invert a bit in the QCA architecture is by "turning a corner" in the correct direction. Of the four possible ways to turn a corner, two produce inverted signals, and two produce original signals

C. Planer Wire Crossing

Because of the unique structure of the QCA architecture, it is possible to cross wires without adding another level or dimension to the structure. This is accomplished by using QCA wires that are using different clocks. For example, two QCA wires that cross at a point do not affect. Each other unless they are using the same clock. This is true even if the QCA in one of the wires would normally drive the QCA in the other have the same polarization and effectively cancel each other's electric field at their midpoint, which is the point where the clock 0 wire crosses. This allows the clock 0 wire to pass unaffected by the clock 3 wire. In general, this effect holds true for any clocking scheme for a wire crossing, as long as the wires are not using the same clock. The ability to clock individual QCA or groups of QCA independent of other, possibly adjacent, QCA is assumed for this planer wire crossing scheme. Clocking with this precision may prove to be a challenge, especially for molecular scale implementations. The architecture is flexible enough to allow for other constructs based on other wire crossing schemes, such as multilayer crossing.

D. Majority Gate

The majority gate is an important structure in the 4-dot QCA architecture as it allows for universal computation to be performed. Likewise, the addition of a majority gate into the limited simple constructs already presented for the QCA architecture would make it a universal architecture as well. Before the majority gate is presented, however, it is required that sufficient explanation of the terms used to describe the majority gate must be given. First, "global inputs" to the QCA architecture are individual QCAs that are locked into their respective logic configurations. This type of QCA is common to all QCA architectures and could be implemented either by an external user Schematic for the simplest of QCA majority gates. QCA implementation of this majority gate. Input or by a specifically created QCA that is inherently fixed in regards to their electron configuration. "Local inputs" are QCA at the inputs to a specific logic construct or logic gate.

These QCA must have variable electron configurations that add to the total energy "calculations" of the system. "Outputs" must always have variable electron configurations and must also be assumed to dynamically contribute to total system Configurations. This is accomplished by the use of clocking, orientation, and global and local inputs. The simplest QCA majority gate can be created with only four QCA cells three of these QCA are held as global inputs (denoted by the blue

dashed outline). The single output QCA must be either clocked where it is driven by the inputs or, since the global inputs do not change, they may also be clocked using the same clock signal. The first clue that the QCA variety of the majority gate will be different than the QCA variety is that the bottom input to the majority gate is naturally inverted. This is due to properties that invert signals

As they turn corners in a specific direction [that is also used in the inverter. This simple majority gate can be used to create two input AND and OR gates by using the bottom input to "program" which gate is needed. For example, if a static logic 1 is applied to the bottom input and variable inputs "A" and "B" are applied to the top and left inputs, the operation of the gate is an AND (A,B) gate. If the same orientation has instead a logic 0 applied to the bottom input, the operation of the gate is an OR (A, B) gate. (Note that because the bottom input is inverted, the typical majority gate logic of adding a static "1" to one input To produce an OR gate and adding a static "0" to one input to produce an AND gate is itself inverted.) The simple QCA majority gate can also be used to create gates which perform the AND (A_, B) and OR (A_, B) operations by adding the static input to the top or left inputs instead of the bottom input. Additionally, this majority gate can also be used as an inverter if opposite static inputs are applied to the top and left inputs and the bottom input is reserved for a variable input. The fact that this majority gate can be both an AND gate, an OR gate, or an inverter allows

The QCA majority gate to be in itself a universal gate. The vast majority of complex circuitry will require that global inputs are not applied directly to individual majority gates. However, converting global inputs to local inputs can modify the logical function produced. This is due to the configuration of

The QCA map which places diagonally neighboring cells Majority gate with global inputs, which are removed from the local input sites: (a) schematic and (b) QCA implementation. Closer in spacing compared to collinear or parallel neighbor cells. An example of this can be found in the following majority gate configuration, in which, the local input sites are driven by collinear global inputs. The operation of this majority Gate does something interesting. It changes its function from the gate to a majority gate with the bottom—and also left—inputs inverted. This interesting feature is due to the majority gate "rejecting" local inputs of the gate. For this layout, the four local cells making up the majority gate (three local inputs and one local output) prefer only two different configurations. Because of the strength of the interaction of the local cells and relative weakness of the collinear wires driving them, they reject single inputs. This is the property that produces the modified majority gate function, which can be used to create a NAND gate, a NOR gate, an AND (A_, B) gate, an OR (A, B_) gate, or an inverter and is thus, in itself, a universal logic gate as well.

Clocking can also be used to change the action of the majority gate. Using the same QCA orientation, we can recover the operation of the majority gate. We do this by clocking the cells so that the inputs drive the output. Other clocking and orientation schemes produce similar logic gate operations to the gates. These different schemes for producing different types of

majority gates begin to show and unlock the complexity of the QCA architecture.

This complexity and richness will be used as the more complex constructs are formed.
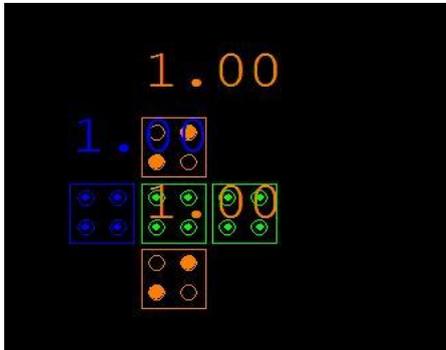
V. QCA Design
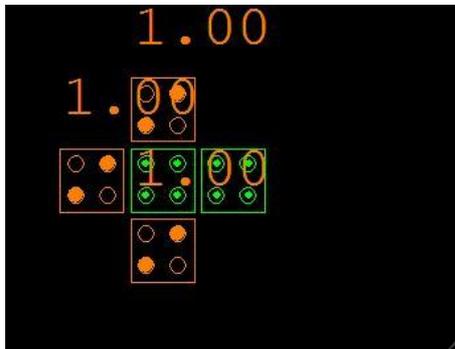

Figure 1.QCA circuit of Majority Gate
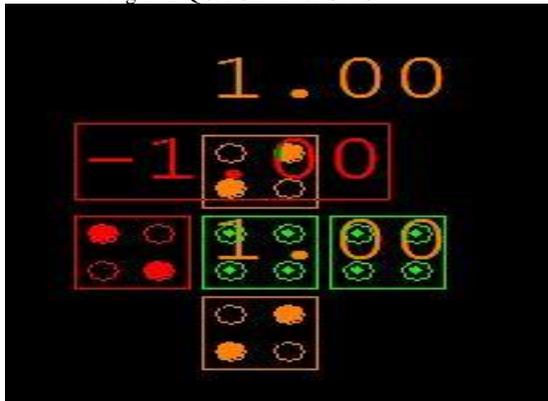

Figure 2.QCA Circuit of OR Gate
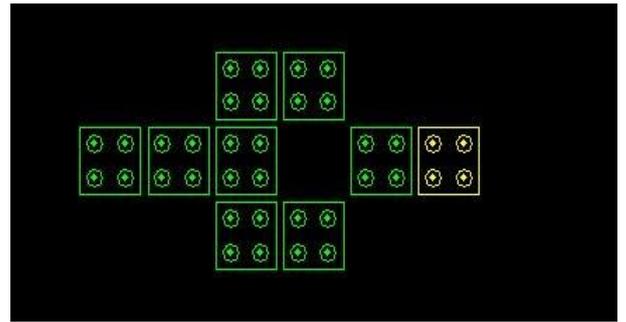

Figure 3.QCA Circuit of AND Gate
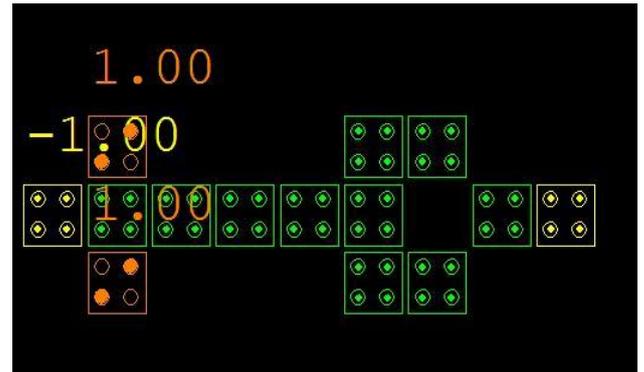

Figure 4.QCA Circuit of Inverter Gate

Figure 5.QCA Circuit of NAND Gate

VI. Simulations of QCA

A. Simulation of majority Gate

Figure 6. Simulation of majority Gate

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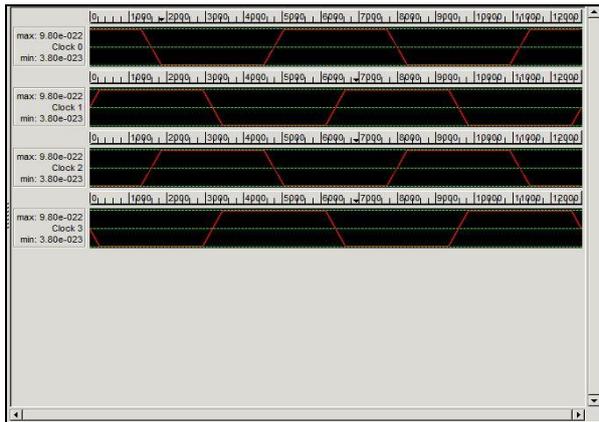B. *Simulation of Or gate*

Figure 7. Simulation of Or gate
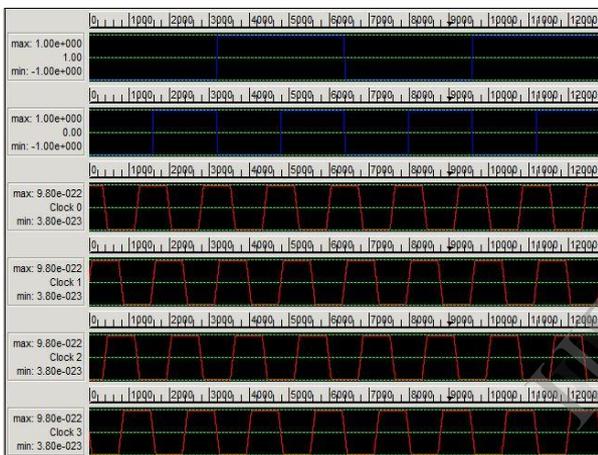
C. *Simulation of And Gate*

Figure 8. Simulation of And Gate

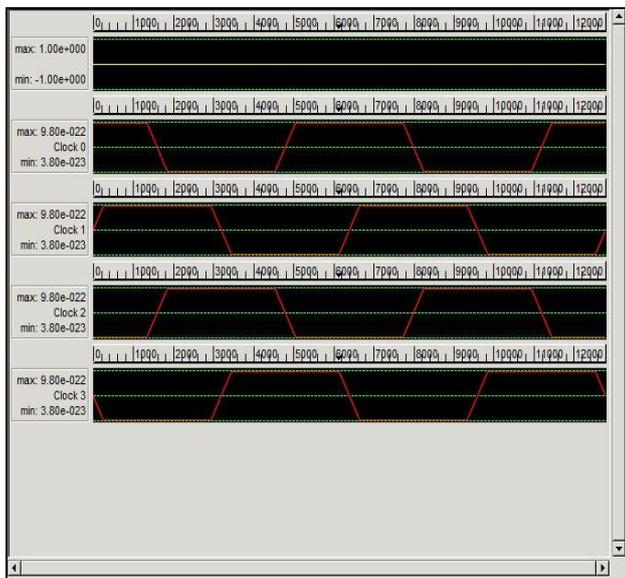D. *Simulation of Inverter gate*

Figure 9. Simulation of Inverter gate
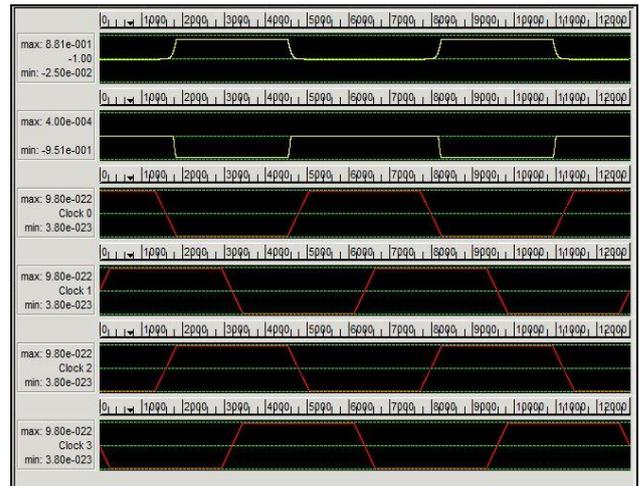
E. *Simulation of Nand gate*

Figure 10. Simulation of Nand gate

VII. CONCLUSION

This paper presents the QCA designs of logic gates majority gate, Or gate, And gate, Inverter, Nand gate. The described solution confirms a possibility of decimal nano computer design, which allows us to avoid both base-conversion errors and machine time losses due to these conversions as well as simplify programming languages and compilers.

Our future Scope is to perform QCA Design and simulation for higher configuration like 6-Dot QCA.

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