Analysis and Design of CMOS Cascode LNA for UWB Applications with Gain Enhancement and Out- Band Rejection Capability.

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Abstract

A 3.1 to 4.8 GHz Low Noise Amplifier (LNA) with gain enhanced and out-band rejection property for Ultra Wide Band (UWB) applications using 0.18 µm CMOS technology is designed and presented. The UWB transmitter and receiver systems signal powers suffers from close narrowband interferers such as the IEEE 802.11 a/b/g wireless local area network, and the 1.8-GHz digital cellular service/global system for mobile communications because of Federal Communications Commission's stringent power-emission limitations. Therefore, we proposed a wideband input network with out-band rejection capability UWB LNA using LC network. It uses a CMOS Cascode stage with 0.18 µm technology. An additional inductor inserted between the Cascode stages to enhance power gain. We have achieved A power gain of 13.2 dB, 3.9 dB of minimum noise figure with 1.9 mW power dissipation for the core LNA.

Index Terms—Complementary metal–oxide semiconductor (CMOS), low-noise amplifier (LNA), out-band rejection, ultra wideband (UWB).

1. Introduction

ULTRA-WIDEBAND (UWB) systems realize high data rate in the short-range wireless transmission, which are suitable for integration in various consumer electronics such as PCs, cellular phones, digital cameras, and PDAs. Federal Communications Commission (FCC). A February 14, 2002 FCC Report and Order authorized the unlicensed use of UWB in the frequency range from 3.1 to 10.6 GHz. The FCC power spectral density emission limit for UWB transmitters is -41.3 dBm/MHz But the minimum received power in the UWB channel is 47 and 67 dB, in the worst case, lower than those of the wireless local area network (WLAN) interferer powers at 5.2 and 2.4 GHz, respectively [1]. In addition, a tone is measured at 1.87 GHz in a smart phone currently on the market, and the power level is 35 dB higher than the UWB signal [2]. All of these interferers, as shown in Fig.1, have a harmful effect on the received UWB signal. A larger attenuation in the front-end can also relax the baseband filter achieving an implementation with the smaller group-delay variations and lower dc power consumption [5].Recently, a design of multiple-stop band filters is presented for the suppression of interfering signals such as global system for mobile communications (GSM), WLAN, and worldwide interoperability for microwave access (WIMAX) in UWB applications [3]. The coupled resonator stop band filter sections with bent resonators were adopted

in order to more effectively suppress harmonics and the maximum rejection is about 25 dB at 1.8 GHz .However, this prototype of the filter, which was fabricated on the basis of the standard printed circuit board (PCB) process, will increase the entire UWB system area. Moreover, the multiple receivers with equal-gain combining were employed to eliminate the narrowband interferers received in the two paths and combined out-of- phase to cancel each other by selecting the optimal local oscillator (LO) phase [4]. A maximum 28-dB attenuation of the interferers was measured, but it is unavoidable to increase the system's complexity.

On the other hand, the topologies utilized for wideband amplifiers generally include the distributed configuration [8], [9], resistive shunt-feedback structure [10]–[12], common-gate termination [13]–[15], and *LC* input network [16], [17]. The distributed amplifiers are attractive for their ultra-wide bandwidth. However, the major drawbacks are the large area and high dc power consumption, which make them unsuitable for many applications. The resistive shunt-feedback and common-gate amplifiers can provide good impedance matching and moderate gain while dissipating small amounts of dc power, but without the out-band rejection capability. Recently, a new topology of the broad band amplifier for out-bands rejection, which adopted a notch filter circuit with negative-resistance cell embedded, has been reported in [18] and [19]. Inevitably, the extra notch filter circuit made of inductors and cross-coupled transistors will occupy additional chip area and dc power simultaneously.

Fig 2(a) shows Direct Sequence (DS) UWB spectrum. In this paper, we have proposed a 3.1 to 4.8 GHz UWB low-noise amplifiers (LNA) for DS UWB lower band applications with out-of-band suppression by using the CMOS technology. In this UWB LNA, a new wideband input impedance-matching network, which is based on the *LC* structure with focus on the improvement of out-of-band rejection capability, is presented. By suitably introducing two additional capacitors in the traditional *LC* input network, two transmission zeros at 1.8 and 8.5 GHz are generated to achieve the out-band rejection property without suffering from deterioration of the in-band performance. A Cascode configuration with source degeneration input stage is used as a core LNA. An intermediate inductor inserted between Cascode stages to improve the power gain and to reduce power dissipation without effecting the other parameters .Sections II present the

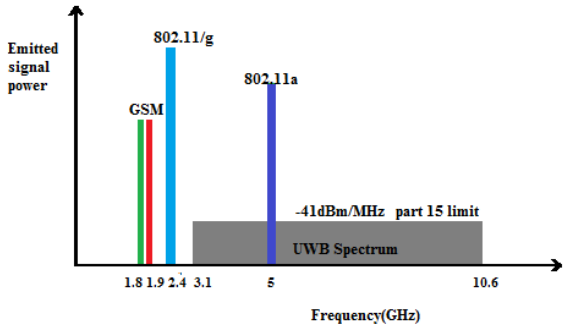

Fig. 1. UWB Spectrum and interferences

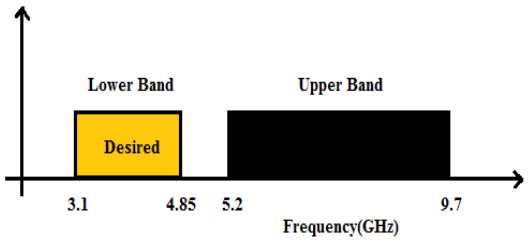

Fig. 2. Dual Band (DB) UWB Spectrum

UWBLNA design approach. The circuit implementation and simulated results are illustrated in Section III, followed by a conclusion in Section IV. In this study, the circuit simulation is performed via Agilent's Advanced Design System (ADS) software with BSIM3 CMOS model

II. LNA Design Approach

The 3.1 to 4.8 GHz CMOS UWB LNA proposed here adopts a source-degenerated Cascode configuration, as shown in Fig. 3. An *LC* input network for wideband operation is utilized with two new capacitors and for increasing the higher and lower out-band rejections, respectively. The load inductor in series with the resistor helps to enhance the gain flatness. The buffer transistor with a purely resistive load is employed for testing purposes. An additional inductor is inserted between the Cascode stages to enhance the overall gain.

A. Power Gain

The overall gain of the LNA without an additional inductor L_c is given by [22] (L_c considered to be shorted)

$$S_{21} = \frac{(1 + S_{11})v_{out}}{v_{in}}$$

$$= (1 + S_{11}) \frac{v'_{out}}{v_{in}} \, g_{m3(R_o || Z_o)} \quad (1)$$

Where

$$\frac{v'_{out}}{v_{in}} = \frac{g_{m1}(1 - \omega^2 L_g C_{RH})}{\square(\omega)} \left[(R_L + j\omega L_L) || \frac{1}{j\omega C_L} \right] \quad (2)$$

With

$$(\omega) = \omega^4 L_g L_S C_T C_{RH} - j\omega^3 L_g L_s g_{m1} C_{RH} - \omega^2 (L_g C_t + L_g C_{RH} + L_s C_t) + j\omega g_{m1} L_s + 1 \quad (3)$$

Z_o is the 50-Ω source resistance, $C_t = C_{gs1} + C_a$ and C_L is the total capacitance between the drain of the transistor M_2 and ground. S_{11} is the reflection coefficient at the input port. From (1), it is seen that extra transmission zeros (i.e.,$S_{21} = 0$) can be created when the following conditions are satisfied:

$$S_{11} = -1 \; or \; \frac{v'_{out}}{v_{in}} \quad (4)$$

In which means that the input impedance of the LNA is short circuit, and it occurs as the impedance Z_R, i.e., the impedance of the L_1C_1tank in series with the capacitor C_{RL} is equal to zero, where

$$Z_R(\omega) = \frac{[1 - \omega^2 L_1 (C_{RL} + C_1)]}{j\omega C_{RL}(1 - \omega^2 L_1 C_1)} \quad (5)$$

By using (2), (4), and (5), the locations of transmission zeros can be predicted as

$$\omega_{RH} = \frac{1}{\sqrt{L_g C_{RH}}} \quad \omega_{RL} = \frac{1}{\sqrt{L_1 (C_{RL} + C_1)}} \quad (6)$$

The overall gain of the circuit is increased by inserting an additional inductor in between the Cascode stages as shown in the fig 3. Complete schematic of proposed LNA.

With an additional inductor L_c between the Cascode stages, the increased value of the voltage gain is proportional to the inductance value of additional inductor L_c

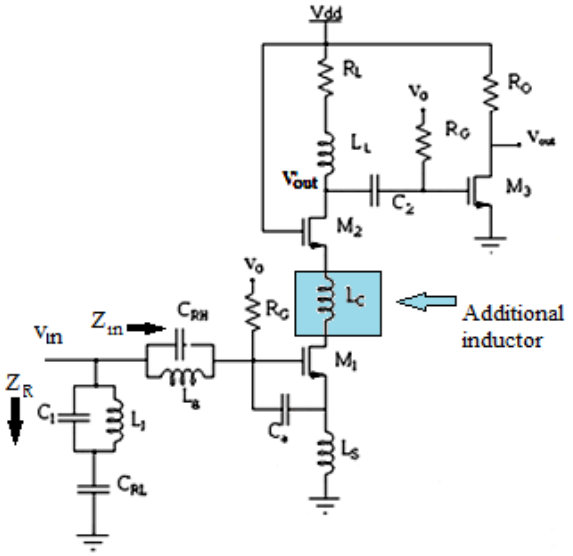

Fig. 3. Complete circuit diagram of proposed UWB LNA.

C. Out-Band Rejection capability.

The above ratiocination reveals that the additional capacitors and will bring about two transmission zeros to ameliorate the out-band performance. However, the out-band rejection characteristics are restricted by the series resistance of the on-chip inductor. As seen from (6), the higher and lower out-band transmission zeros are associated with the inductors and L_g and L_1 , respectively. These component values influence not only the zeros' frequencies, but also the out-band suppression levels,. The higher frequency out-band elimination efficiency is mainly determined by the impedance of the L_gC_{RH} tank at the resonant frequency (i.e., the larger impedance, the superior out-band suppression). Therefore, the first step is to assign a larger to arrive at larger resonant impedance [20, Ch. 14]. In addition, a preferable power gain in the target frequency range can be procured contemporaneously by using a larger value of L_g. The impedance of input LC circuit produces one series and one parallel resonance from which the lower transmission zero can be created. It is expectable that a smaller impedance at the series resonant frequency will accomplish the superior out-band elimination efficiency.

From the above discussion, it should be taken into account punctiliously by choosing appropriate values of and to achieve the tradeoff between the input match and out-band rejection performances. It is interesting to see the influence of the input network on the LNA's NF. After a

straightforward derivation following the procedure in [21],
The NF of the circuit shown in Fig. 3 can be obtained as

$$NF \propto \left[1-\left(\frac{\omega}{\omega_{RH}}\right)^2\right]^{-2}\left[1-\left(\frac{\omega}{\omega_{RL}}\right)^2\right]^{-2} \qquad (7)$$

Obviously, the proposed UWB LNA will produce double-peak maxima in noise factor at the two transmission zeros. Consequently, it must be cautious to prevent from worsening the noise property in the desired frequency range when designing the locations of the zeros. Fig. 5 shows the simulation result of the NF the total circuit. In this Cascode LNA the dominant noise contributor is the active gain stage. The out-band rejection input network has a minor influence on the total NF as long as the designed transmission zeros are not too close to the in-band. To reduce the noise contribution from the active gain stage, the width of the transistor will be chosen for optimum noise property. The additional inductor between the Cascode stages is chosen to optimize the total noise figure.

III. Implementation and simulation

The proposed out-band rejection UWB LNA is designed and simulated using Agilent Advanced Design System with 0.18 µm CMOS technology. The

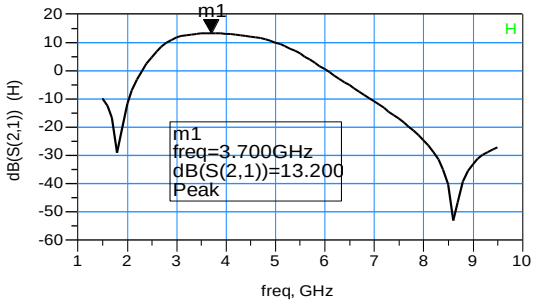

Fig.4. Power gain (S_{21}) of LNA

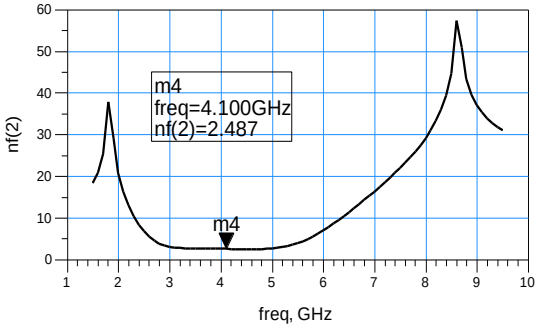

Fig. 5. Noise Figure of LNA

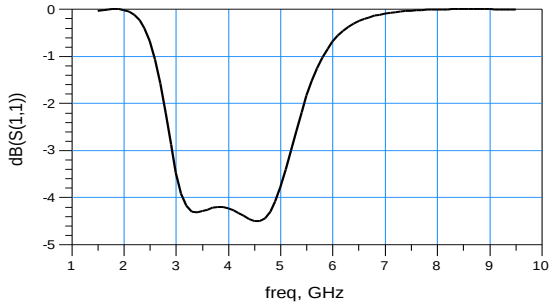

Fig. 6. Input Reflection Coefficient (S_{11}) of LNA

UWB LNA shown in Figure 3. The width of the transistor M_1 (145 µm)is optimized with the 1.9 mw power dissipation with good noise property. The comparisons are shown in the table.1.The size of the Cascode transistor M_2 (300 µm) is selected to be as large as possible to reduce its voltage headroom requirement, which is conductive to low voltage operations. In addition, the design of the input match and out band rejection characteristics are optimized with the proper selection of the input LC filter component values. In

Table.1
LNA performance comparisions

Reference	Technology	V_{dd} [V]	BW [GHz]	S_{11} [dB]	G_{max} [dB]	NF_{Min} [dB]	P_{diss} [mW]	Out band Rejection
[23]	0.18 µm CMOS	1.8	3 ~ 6	<-12	15.9	4.7	59.4	-
[24]	0.18 µm CMOS	1.3	0.04 ~ 7	<-16	8.6	4.2	9.0	-
[25]	0.18 µm CMOS	1.8	2.8 ~ 7.2	<-4	19.1	3	32.0	-
[26]	0.18 µm CMOS	1.8	3 ~ 4.8	<-10	13.9	4.7	14.6	-
[27]	0.18 µm CMOS	1.5	3 ~ 4.8	<-7	16	2.7	11.9	15 dB @ 2.4 GHz 19 dB @ 5.3 GHz
[18]	0.13 µm CMOS	1.5	3~5	<-10	19.4**	3.5	31.5	6 dB @ 2.4 GHz 44 dB @ 5.2 GHz
[19]	0.18 µm CMOS	1.8	3 ~ 4.8	<-10	19.7	4	24.0	13 dB @ 2.4 GHz 20 dB @ 5.8 GHz
[22]	0.18 µm CMOS	0.9	2.8 ~ 6.2	<-9	11.5	3.8	2.5*	25 dB @ 1.8 GHz 32 dB @ 8.5 GHz
This proposal	0.18 µm CMOS	0.9	2.9 ~ 4.9	<-4	**13.2**	3.9	**1.9* 6.2**	**42 dB @ 1.8 GHz 66 dB @ 8.5 GHz**

this study, the component values of the input network are L_1 = 1.8 nH, L_g =2.0 nH,C_1 = 0.91 pF, C_{RL} = 3.3pF,C_{RH} = 17 pF, C_a =0.025 pF and additional inductor L_c = 1.5 nH. The load consists of an inductor L_L in series with R_L to achieve flat gain over the whole band width. The value of Ro is set as 50 Ω to achieve output match for testing purposes.

The LNA drew a 2.1-mA dc core current from the 0.9-V supply voltage and complete LNA drew a 6.9-mA shown in table.2 .The simulated power gain of LNA shown in Fig. 4. The peak gain is 13.2 dB at 3.7 GHz with a 3-dB and width of 2GHz from 2.9 to 4.9 GHz and the minimum value of the noise figure is 3.9 dB .the input reflection coefficient (S_{11}) is less than -4dB in the operation Bandwidth shown in the figure. 6. The simulated out band rejection obtained 42 dB at 1.8 GHz and 66 dB at 8.5 GHz. From the peak power gain Shown in the Fig. 4.

IV. Conclusion

In this paper, we proposed a UWB LNA configuration with out-band rejection ability and demonstrated the simulated results using the 0.18 µm CMOS process. Extra transmission zeros are created by the use of an *LC* input network with additional capacitors and for improving the higher and lower out-band performances. Finally we have achieved gain enhancement and low power dissipation with an additional inductor between the Cascode stages.

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