Analog Circuits Testing Using Monte-Carlo Analysis and Neural Networks

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Abstract

Analog Circuits testing using Monte Carlo Analysis and Neural Networks is a new technique which is proposed for the diagnosis of fault in Analog Circuits. According to this method, the circuit which is to be tested is supplied with a ramp shape voltage. The output supply current is now analyzed with a new unsupervised neural network. If circuit has any fault then its supply current waveform will change. In this case the waveform of the supply current can be related to the type of the fault. In general to obtain this relationship will be a difficult task, but neural networks can provide a suitable solution for this problem. This network has been used in a hierarchical way. In the first step, a single layer is used to classifies the faults. If a single node represents a few faults then a sub layer is added to classify the other faults. This process will continues until a node represents each fault class according to analysis.

Keywords : Neural Networks , Ramp Supply voltage

Introduction

A new fault detection technique for analog circuits is developed. In this method, the circuit is supplied with a ramp shape voltage. The resulted supply current is analysed with a new unsupervised neural network. Simulating different faults and the Monte-Carlo analysis to account for parametric change and tolerances does the training of the proposed neural network.

In recent years, because of intensive capacity of integrated circuits, there has been a growing interest toward merging of analog and digital circuits. Testing of analog part of such circuits would be more difficult since analog circuits have greater range of input and output and their response are affected by tolerance and temperature. Several methods have been proposed

for testing of analog circuits. One group is based on simultaneous test of several points and is referred to the method of “bed of nails”. This method has the problem of accessing these points and is not feasible for integrated circuits because of unavailability of required points. The method of “built-in-self-test” in which the test circuit is built inside the integrated circuit increases the complexity, cost and decreases the speed. One of the methods that have recently been employed for test and fault detection in analog circuits is using a ramp voltage instead of DC voltage for the power supply of the circuit . In this case the power supply current contains information that pertains to the topology of the circuit. If circuit has a fault, its supply current waveform will change. The supply current waveform in this case can be related to the type of the fault. Obtaining this relationship in general could be a challenging task, but neural networks could offer a reasonable solution to this problem. The power supply current, resulted from ramp supply voltage, has been related to the respected fault by the Kohonen Self-Oganizing Feature Map (KSOFM) neural network . This network has been used in a hierarchical way. In the first step, a single layer KSOFM classifies the faults. If a single node represents a few faults, a sub layer is added to classify the misrepresented inputs. This continues until a node represents each fault class according to analysis.

Classification of faulty and fault free circuits

Classification is done using the frequency response. Variations in the component values affect the peak amplitude or central frequency of the filter. So the two parameters taken into consideration for the classification are the peak amplitude and the shift in the central frequency. The tolerance for the amplitude and central frequency shift is 10% of the nominal value. The correct circuits are those which have a tolerance within 110% and 90% of the nominal value for both the amplitude shift and the central frequency shift of the frequency response. The faulty circuits are those which have tolerances above 120% or below 80% of the nominal value for both amplitude shift and central frequency shift. Figure 2 shows the frequency response of a bi-quadratic filter. It also shows the tolerance bands for the peak amplitude and the central frequency. In case of bi-quadratic filter 100 samples were taken between .5MHz and 1.5MHz. Figure 3 shows the transient responses of the bi-quadratic filter (saturated ramp input). In the case of bi-quadratic filter 50 samples are taken from 0 to 4.9microseconds in case of continuous

pulse and 50 samples from 0 to 3 microseconds in case of saturated ramp input. The input in case of the bi-quadratic filter is 1V.

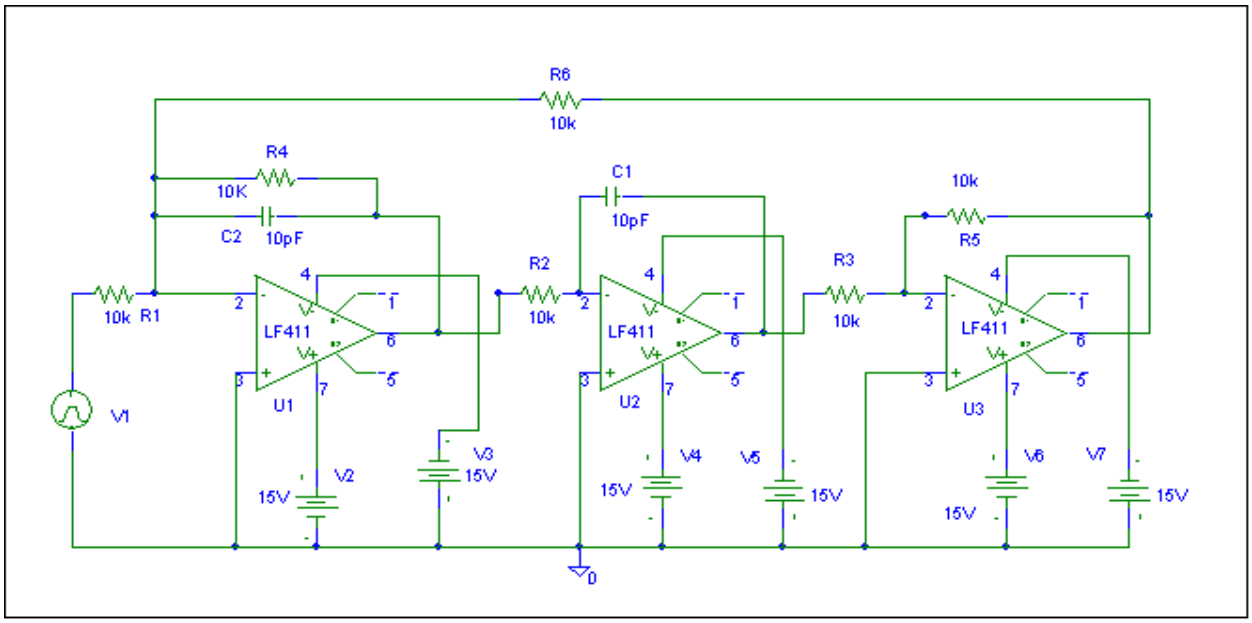


Figure 1. A Bi-quadratic Filter.

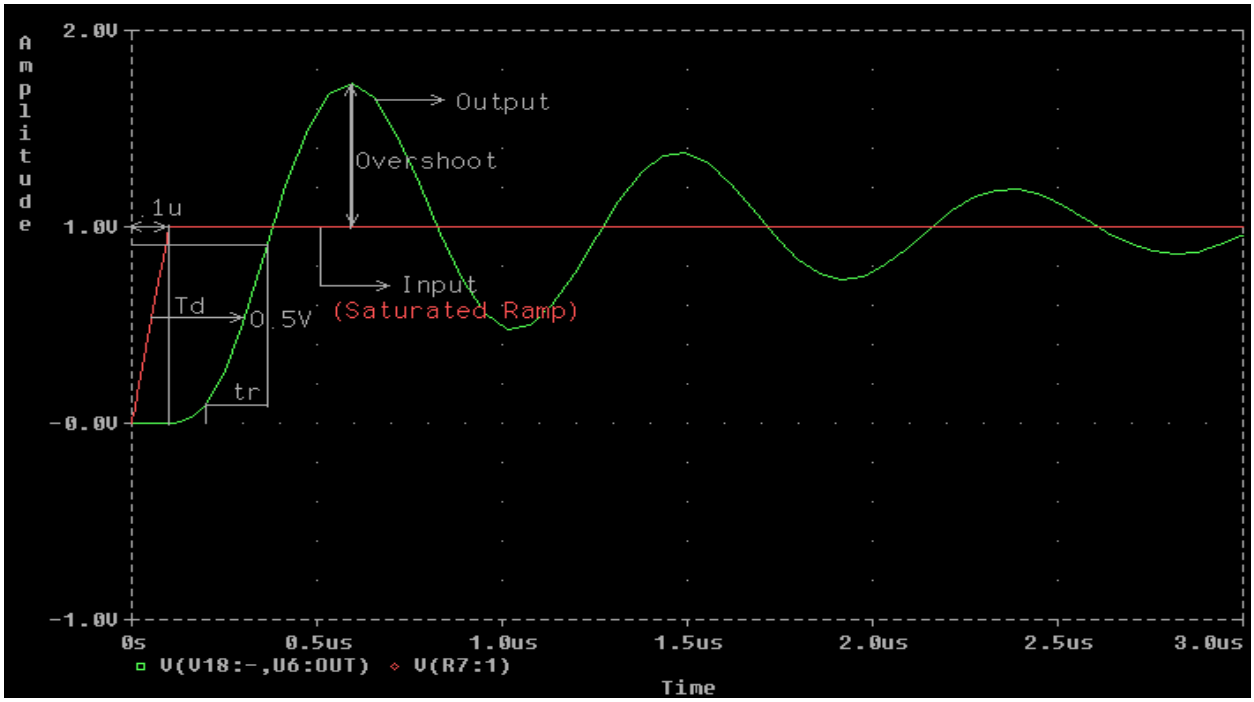


Figure 2. Transient Response of Bi-quadratic Filer for a Saturated Ramp input

Procedure of fault detection

The proposed method consists of three stages, namely, pattern generation, training and test. In the pattern generation stage, the circuit is simulated and its supply current

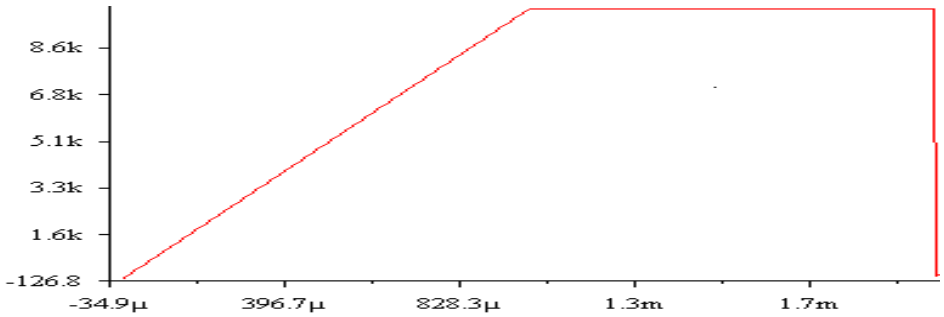


Figure 3. The waveform of supply voltage

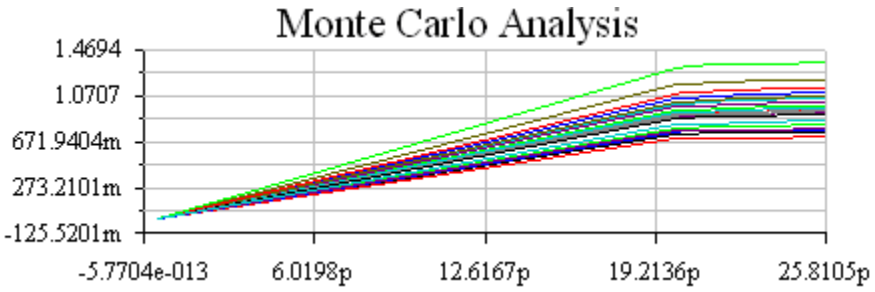


Figure 4. Supply current waveform patterns resulted from Monte-Carlo Analysis

resulted from applying ramp supply voltage is registered. The typical supply voltage waveform is shown in Figure 3.Waveform is sampled at m points and registered. For each state, with the help of Monte-Carlo analysis, more than one pattern is obtained. In each iteration, the Monte-Carlo analysis changes a parameter with respect to its nominal value and yields a pattern for that state. A sample of current waveforms for a specific state is shown in Figure 4. The patterns obtained from previous stage needed to be learned by a neural network .

The main techniques location and identification are:

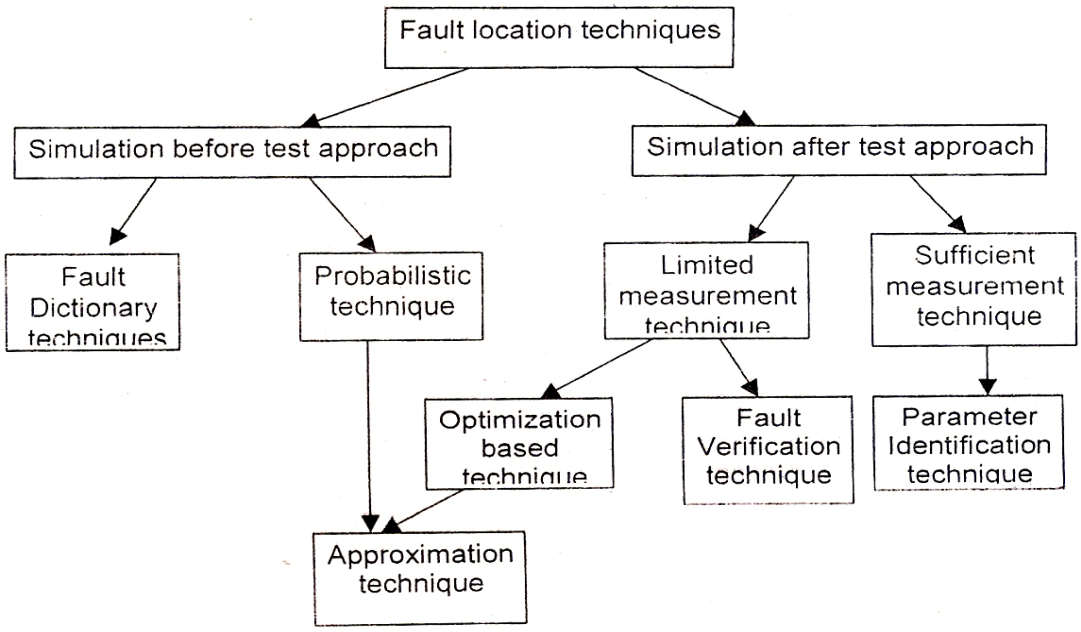


Figure 5 Fault location techniques

Monte-carlo analysis is a statical technique that we explore how changing component properties affects circuit performance

It will perform

- AC analysis
- DC analysis
- Transient analysis

Transient Analysis

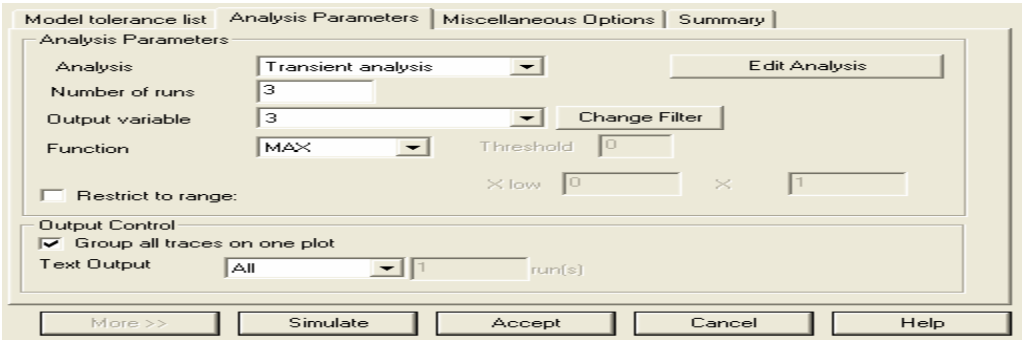


Figure 6 Transient analysis

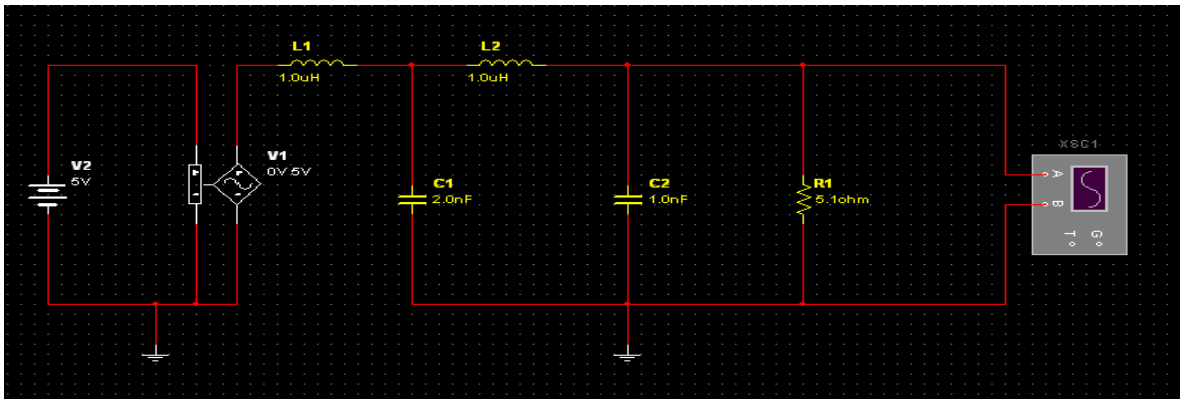
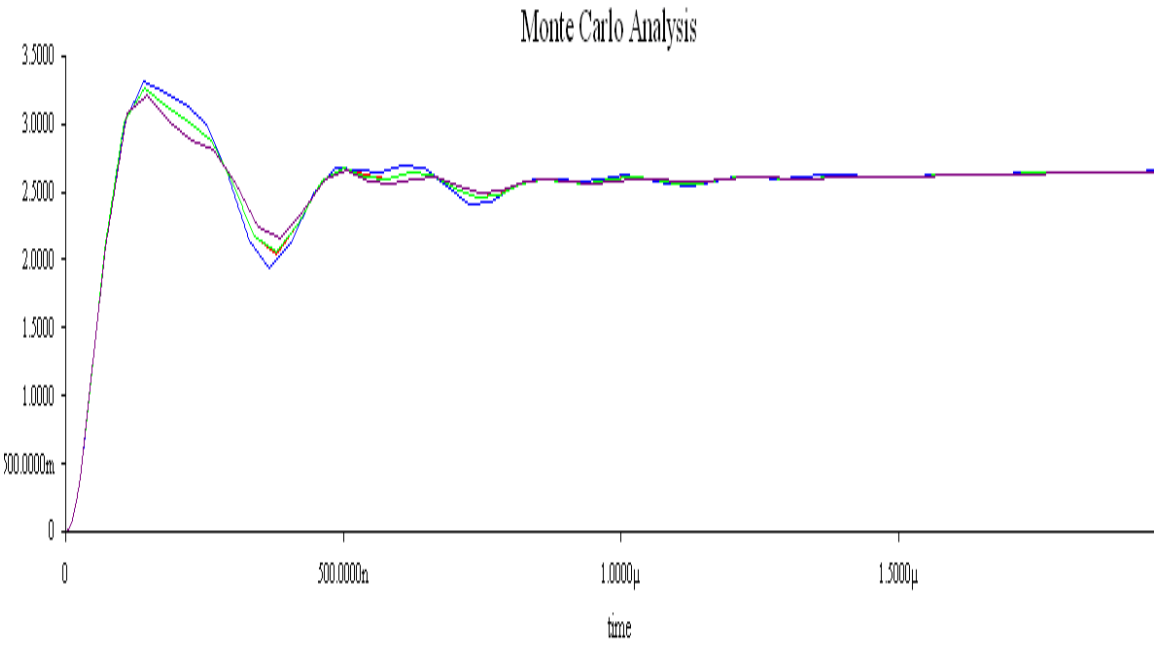


Figure 7 Example circuit for performance



Run Log Descriptions

# of run	time [sec]	worst value	sigma	parameters
Nominal Run...	1.42544e-007	3.26964 (same as nominal, higher than mean by 0.00250703)	0.0693036	rr1 resistance=51
Run #1		3.31676 (1.44107% higher than nominal, higher than mean by 0.0496247)	1.37181	rr1 resistance=57.845
Run #2		3.26759 (0.0627825% lower than nominal, higher than mean by 0.000454263)	0.0125575	rr1 resistance=50.7426
Run #3		3.21455 (1.68499% lower than nominal, lower than mean by -0.052586)	1.45367	rr1 resistance=45.0093

Figure 8 Monte Carlo Analysis

Analysis of CMOS operational amplifier circuit using monte carlo method and neural network analysis

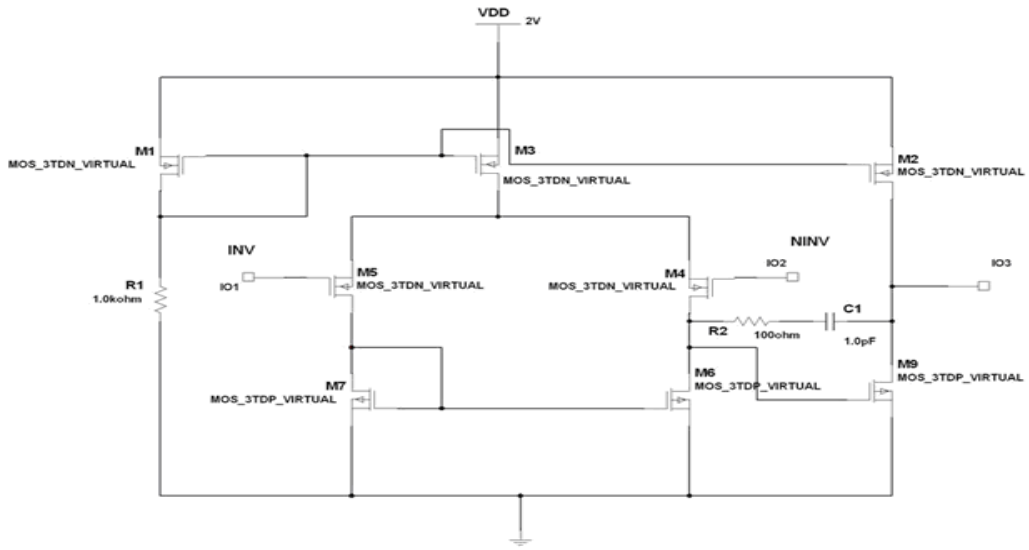


Figure 9 CMOS operational amplifier circuit

Conclusion

A new method based on application of ramp voltage as supply voltage and classification of supply current patterns has been described. This method takes advantage of Monte-Carlo analysis and modular neural network. The modular neural networks, developed in this research, is more sensitive to the transition regions of supply current waveforms. The simulation results show that the accuracy of the proposed system, compared to similar system, is almost doubled. Thus the outcome of using modular system is better accuracy and less training time. Further research is needed to improve the detection of such fault states.

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