Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 8 Issue 07, July-2019

An Optimal Design and Analysis of Low Power Phase Locked Loop using CMOS 32nm Technology

Miss. Monalisa M. Holkunde
Electronics and Telecommunication Department,
M.S. Bidve College of Engineering,
Latur- 413512- India

Prof. V. S. Bale
Electronics and Telecommunication Department
M.S. Bidve College of Engineering,
Latur- 413512- India

***Abstract*— Phase-locked loop (PLL) is widely applied for different purposes significantly for technology advancement in communication and instrumentation area. Many inventions have been listed in PLL design combined with novel integrated circuit technology have made PLL devices important system components. This increases the speed of operation of system but also the power consumption. In this paper a low power and high performance physical design of Phase Locked Loop is introduced. The proposed work is aimed to achieve the low power consumption and high stability. Based on the proposed idea, a physical design of PLL with feedback system is designed and simulated in Microwind 3.5 environment using 32nm CMOS technology with supply voltage of 1 V and IO Vdd as 1.8V. The complete design consumes 0.151mW of power. The designed PLL design is optimized to area of 18.5 µm2.**

Keywords – PLL, Physical design, PLL, Feedback System, VCO, Microwind 3.5.

I. INTRODUCTION

A phase-locked loop is a feedback control system that generates an output signal whose phase is related to the phase of an input signal. PLL is an integral design block of various system in communication and instrumentation area. With the continuous advancement of CMOS technology, the need for low complexity, low-power and high stability PLL has increased as more and more functions on the chip implemented. Along the same, with an increasing trend to a system-on-chip, in order to achieve low manufacturing cost, PLL has to be implemented in a low-voltage submicron CMOS technology. With aspect to this, we have proposed a low power and high stability PLL design.

A typical design of PLL consists of three basic blocks as phase detector, a low pass filter (LPF) and a Voltage Controlled Oscillator (VCO).

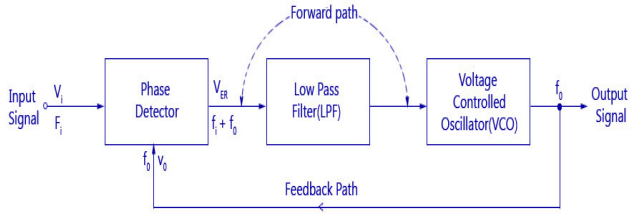

Fig. 1: Block diagram for PLL design system

The input signal 'Vi' with an input frequency 'fi' is passed through a phase detector. A phase detector is basically a comparator which compares the input frequency 'fi' with the feedback frequency 'fo' .The phase detector provides an output error voltage 'Ver' (=fi+fo), is nothing but a DC voltage. This DC voltage is then passed on to an LPF. The LPF removes the high frequency noise and produces a steady DC level, 'Vf' (=Fi-Fo).

The DC level is then passed on to a VCO. The output frequency of the VCO (fo) is directly proportional to the input signal. Both the input frequency and output frequency are compared and adjusted through feedback loops until the output frequency equals the input frequency. Thus the PLL works in these stages free-running, capture and phase lock.

As the name suggests, the free running stage refer to the stage when there is no input voltage applied. As soon as the input frequency is applied the VCO starts to change and begin producing an output frequency for comparison this stage is called the capture stage. The frequency comparison stops as soon as the output frequency is adjusted to become equal to the input frequency.

This stage is called the phase locked state. The paper is organized as follows. In section II, design overview of PLL is described. Section III and IV describes proposed physical part design of PLL system and performance analysis. Finally section V concludes the paper.

II. PROPOSED PLL DESIGN

Basic PLL is a feedback system composed of three elements: a phase detector, a loop filter and a voltage controlled oscillator (VCO).

1. Phase Detector

The phase detector output voltage proportional to the phase difference between the VCO's output signal and the reference. The phase detector output produces a regular square oscillation when the clock input and signal input have one quarter of period shift or 90º (π/2).

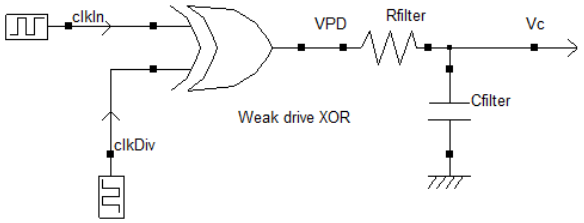

Fig. 2 : XOR gate Phase detector with filter

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 8 Issue 07, July-2019

The XOR gate output produces a regulator square oscillation VPD when the 'clk' and the signal 'divin' have one quarter of period shift (90º or Π/2).

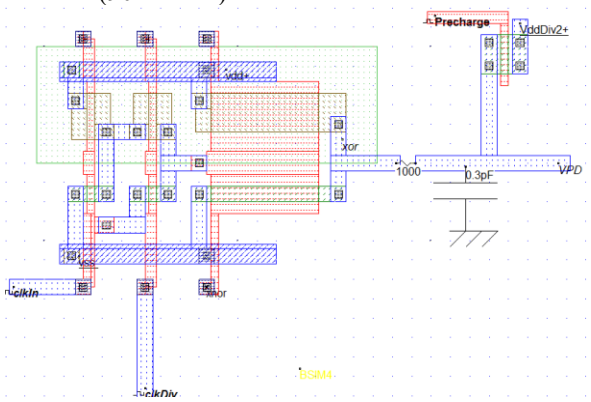

Fig. 3: Physical design of Phase Detector with filter

2. *Filter*

The filter is used to transform the instantaneous phase difference VPD into an analog voltage 'Vc' which is equivalent to the average voltage 'VPD'. The rapid variations of the phase detector output are converted into a slow varying signal 'Vc' which will later control the voltage controlled oscillator. Without filtering, the VCO control would have too rapid changes which would lead to instability. The filter may simply be a large capacitor C, charged and discharged through the Ron resistance of the switch. The 'RonC' delay creates a low-pass filter.

3. *Voltage Control Oscillator*

The VCO is the most important functional unit in the PLL. It is commonly used for clock generation in phase lock loop circuits. Its output frequency determines the effectiveness of PLL. In addition to operating at highest frequency, this unit consumes the most of the power in the system. Obviously, this unit is of particular focus to reduce power consumption. PLL with multiple outputs means to design VCO with multiple outputs.

The voltage controlled oscillator (VCO) generates a clock with a controllable frequency. The VCO is commonly used for clock generation in phase lock loop circuits. The clock may vary typically by +/-50% of its central frequency.

The current-started inverter chain uses a voltage control 'Vcontrol' to modify the current that flows in the N1, P1 branch. The current through N1 is mirrored by N2, N3, N4, N5 & N6. The some current flows in P1. The current Through P1 is mirrored by P2, P3 and P4. Consequent by the change in 'Vcontrol' induces a global change in the inverter currents and acts directly on the delay.

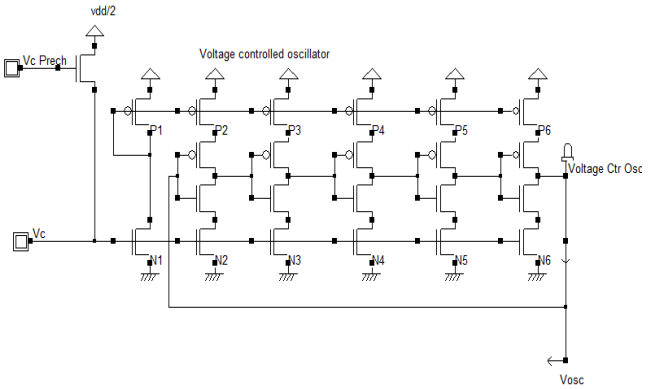

Fig. 4: Schematic design of VCO

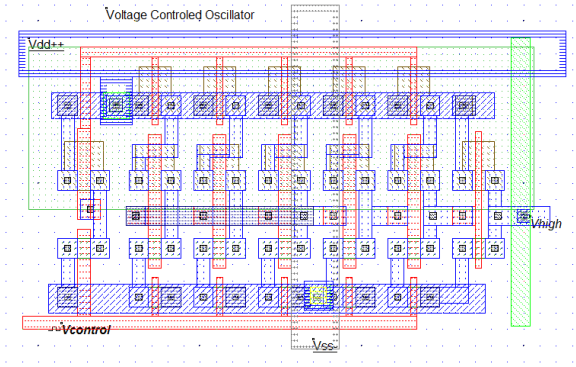

Fig. 5: Physical design of VCO

4. *Complete PLL system*

The PLL system design is done with combining all three parts as designed above.

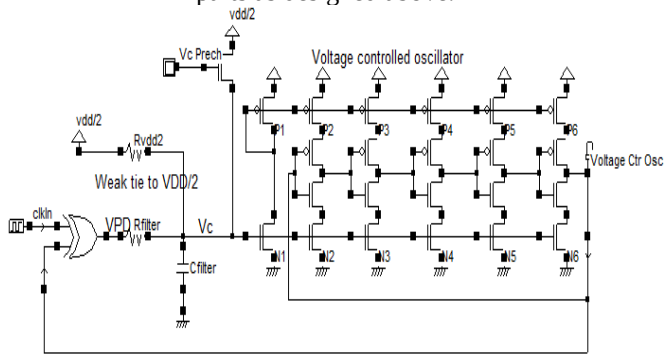

Fig. 6: PLL design combining with all three modules

III. PHYSICAL DESIGN IMPLEMENTATION

The proposed PLL is designed and analyzed using 32 nm CMOS technology with Microwind 3.5.

Microwind software is having module level design approach where one can create module of the discrete component use in the design and can be inserted on the same substrate.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 8 Issue 07, July-2019

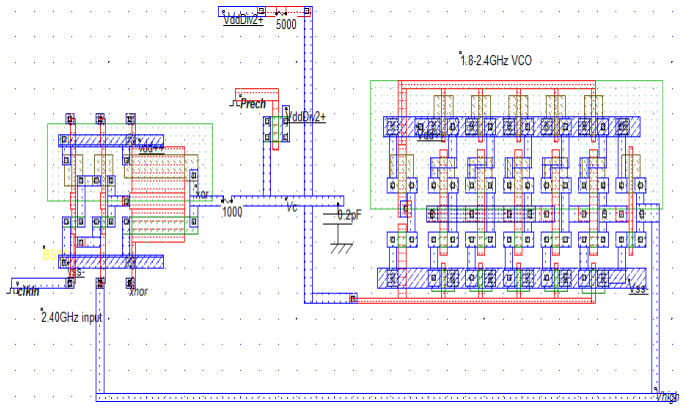

Fig. 7: Physical design for complete PLL system

Physical design parameters for PLL:

Width: 21.2µm (354 lambda)
Height: 9.7µm (161 lambda)
Surf: 205.2µm2
Electrical nodes: 31
NMOS devices: 29
PMOS devices: 28

IV. PERFORMANCE ANALYSIS

For simulation here are the details;
While dealing with phase detector, where both the input signals, CLKIn and CLCDIV are at the different levels. Here we are delaying the period of the second signal, CLCDIV with almost doubling the value of period.

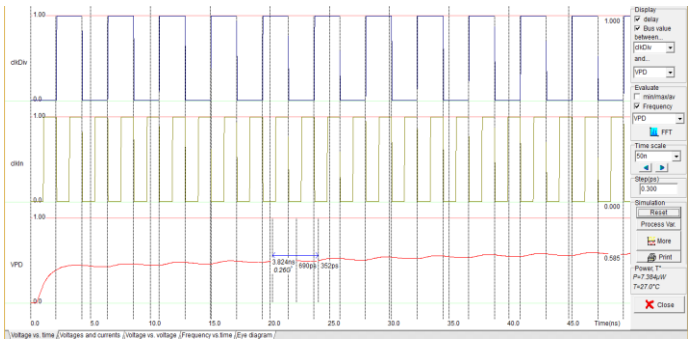

Fig. 8: Input vs output for two signals with periodic phase difference

In the simulation, it is cleared that, the output of phase detector, VPD is varrying with the change in period level change of signal.
For VCO, the inut signal V-Control, is varrying in such a manner that from lower level to upper so that we can find the oscillating frequency. In our case, VCO starts oscillating from 0.4V with output of maximum frequency as 2.80 GHz.

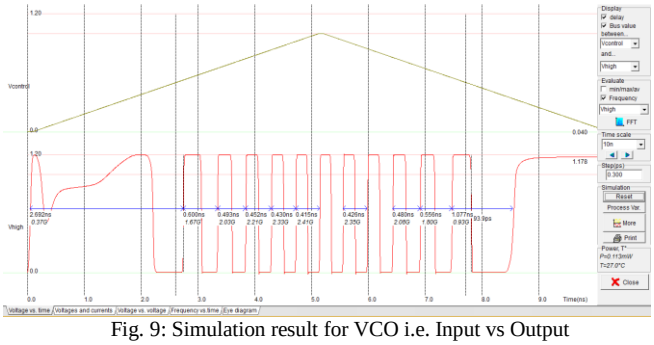

Fig. 9: Simulation result for VCO i.e. Input vs Output

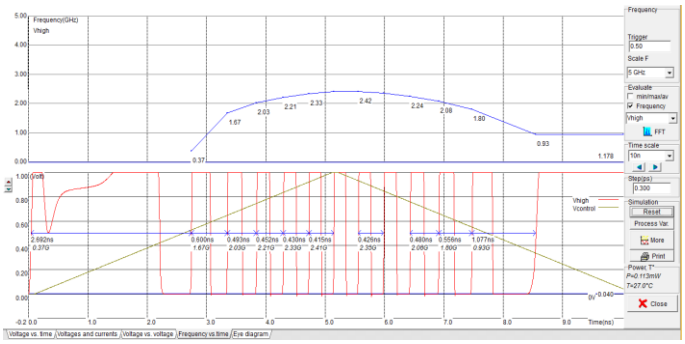

Fig. 10: AC Transient analysis for VCO

Combining all the physical modules of PLL system, below provided is the transient analysis for voltage of PLL. Her the input signal is varied so instantaneously.

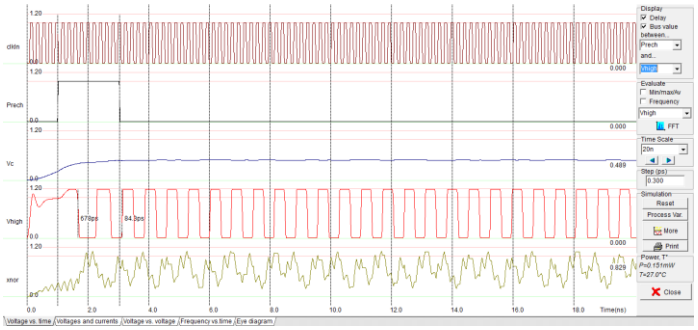

Fig. 11: Simulation result of complete PLL

This implementation includes a filter register Rfilters of 1000.0 nm (1000-Ω) and RVdd Div2 of 5000.0 Ohm (5000 Ω). The virtual capacitor Cfilter is fixed to 0.3pf. This resistance and capacitance are easy to integrate on-chip. The input frequency is fixed to 2.44 GHz. Simulation has seen on chip. During the initialization phase, the precharge is active & control voltage Vc rapidly change to VDD/2.

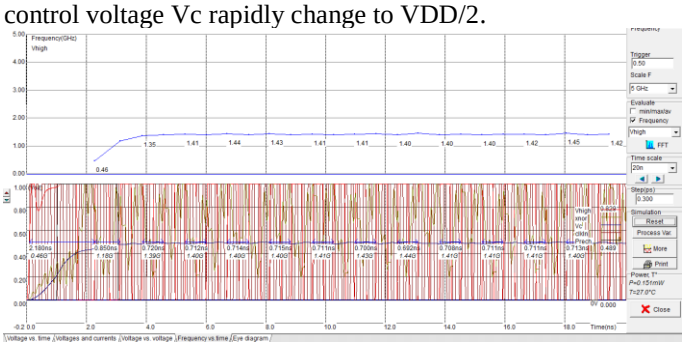

Fig. 12: Frequency vs time simulation

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 8 Issue 07, July-2019

We have seen that for the first 10 nanoseconds the phase difference is very important. The VCO outputs starts to converge to the reference clock. In terms of voltage control, Vc tends to oscillate and then converge to a stable state where the PLL is locked and stable. The output is equal to one fourth of the period according to phase detector principles.

V. CONCLUSION

This paper is presented a PLL with improved power designed in CMOS 32nm technology. This paper presents the physical design implementation and simulation of PLL design. The simulation results allow the circuit designer to fully explore the trade-offs like Glitch period and power consumption. The goal of this design is to achieve more than 1GHz and successfully achieved 1.23GHz frequency.

At last, we club up all the working modules of the PLL in 32nm CMOS technology. It consumes different power values for the various range of input frequency variations, as for triangular waveform as input, it consumes, 0.151mW of power for running simulation for 200nsec.

REFERENCES:

[1] Aastha Singhal, Charu Madhu, Vijay Kumar, “Designs of All Digital Phase Locked Loop”, IEEE transactions on Recent Advances in Engineering and Computational Sciences" IEEE" 2014 (RAECS).

[2] Dong Xie ; Dajin Zhang ; Peng Gao, “Research on phase-locked loop control and its application”, 2016 IEEE Information Technology, Networking, Electronic and Automation Control Conference.

[3] De Sousa and Huyart 2004] Fernando Rangel de Sousa, Student Member, IEEE, and Bernard Huyart, Member, IEEE, “A Reconfigurable High-Frequency Phase-Locked Loop”, ieee transactions on instrumentation and measurement, vol. 53, no. 4, august 2004 1035.

[4] Zainab Mohamad Ashari, Anis Nurashikin Nordin, Muhamad Ibn Ibrahimy, “Design of a 5GHz phase-locked loop”, 2011 IEEE Regional Symposium on Micro and Nano Electronics.

[5] V. Lagareste ; F. Badets ; D. Belot ; Y. Deval ; J.B. Begueret ; P. Melchior, “A new PLL architecture: the composite PLL”; IEEE 48th Midwest Symposium on Circuits and Systems, 2005.

[6] Sicard and Bendhia 2007] Etienne sicard, Sonia Delmas Bendia, Advanced CMOS Cell Design, TATA McGRAW HILL 2007.

[7] Ms. U. A. Belorkar, Dr. S. A. Ladhake, “Design of high performance VCO using 65nm VLSI technology.” International journal of Computer Networking & Communication system, vol.2.