An Innovative Approach of Single Phase Single Stage Inverter to Eliminate Common Mode Leakage Current

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Abstract—This paper proposes a single-phase, single-stage buck-boost inverter for photovoltaic (PV) systems. The presented topology has one common terminal in input and output ports which eliminates common mode leakage current problem in grid connected PV applications. Although it uses four switches, its operation is bi-modal and only two switches receive high frequency PWM signals in each mode. Its principle of operation is described in detail with the help of equivalent circuits. Its dynamic models presented, based on which a bi-modal controller is designed.

I.INTRODUCTION

Mainstreaming of renewable energy sources like solar photo voltaic (PV) and emphasis on storage systems like fuel cell (FC) in the current energy scenario are faced with the ubiquitous challenge of conditioning the dc output into grid quality ac power. Inverter circuits, which execute this function, boost and invert the variable output dc voltages from these PV or FC devices to ac voltages with tightly controlled magnitude and frequency for interfacing with utility grid. PV inverter topologies, without any galvanic isolation, are today de-rigueur due to their size and cost advantages. However, the senon-isolated inverters are associated with problems liked current injection to the grid and common mode leakage current (CMLC), the latter impairing PV panel life. Half or full bridge inverters are the most common topologies employed for grid connected PV systems, though these suffer from the problem of CMLC. This problem can be modified by using bipolar pulse width modulation (PWM) technique. But this brings problems like large grid current ripple, high harmonic content and poor efficiency of the inverter. This problem was proposed to be resolved by disconnecting positive and negative terminals of PV from free-wheeling path during zero output voltage level generation. Networks that perform this task are classified in two categories based on the method of decoupling, i.e. dc or ac. The dc-based decoupling configurations incorporate the decoupling network in the decide to provide the decoupled freewheeling path, examples being H5, H6. Solutions like HERIC, on the other hand, include the decoupling network in the ac side to provide the decoupled freewheeling path. However, due to the presence of junction capacitance of switches, a high frequency common mode voltage is generated. Moreover, there is a chance of high frequency resonance during freewheeling mode. A class of reported topologies share one common terminal between PV and grid, which ensures zero CMLC. In, one such topology is proposed with buck boost capability. But since it uses two input voltage sources for positive and negative halves of output voltage, this leads to underutilization of PV panel. In and differential connection of two buck-boost and boost converters were proposed. These converters shape simple configuration with four active switches suitable for renewable energy application. However, hard switching of all the devices at high frequency reduces the efficiency and increases its affinity towards EMI problems.

The inductors in are replaced by coupled inductor pairs. This provides high voltage gain capability but the problems of its parent topology persist. Some topologies which operate only in buck mode require high input voltage for grid connected applications. In previous paper solution propose a buck boost inverter where an ac-ac unit is used to perform the boost function. However, this unit comprises four active switches which increase the overall switch count, which greatly reduces power density and efficiency. In other lecture proposed doubly grounded buck boost inverters. However, active switch count of all these are greater than or equal to five, which makes them no better than traditional two stage configuration. Single stage inverter proposed in last lecture 21 uses a pair of coupled inductors which allows it to attain high voltage gain and reduces the size of power decoupling filter size. However, the use of seven semiconductor devices impairs system efficiency.

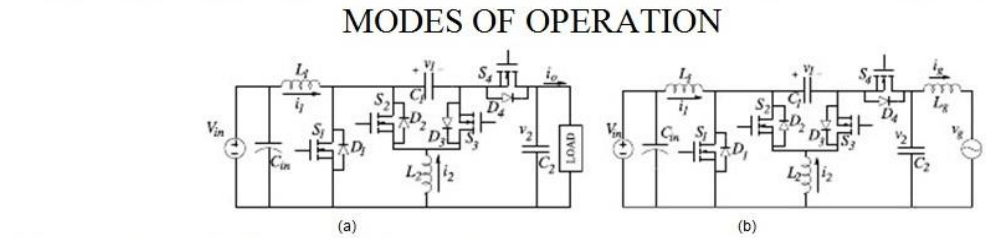

Fig. 1. Proposed Inverter (a) Stand-alone Mode (b) Grid-connected mode.

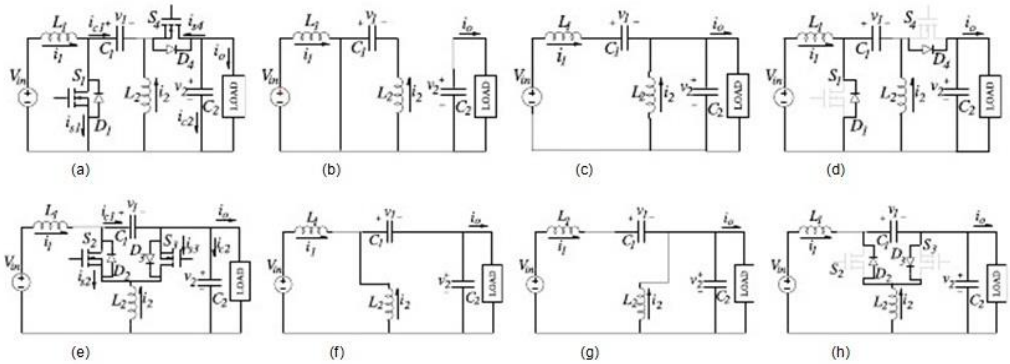

Fig. 2. Mode-1 circuits (a) Two switch equivalent (b) ON time (c) OFF time (d) Dead time; Mode-2 circuits (e) Two switch equivalent (f) ON time (g) OFF time (h) Dead time.

This paper proposes a buck-boost single-phase inverter with only four switches, two inductors and two capacitors. It also shares a common terminal between the input and output ports, which practically eliminates CMLC problems and reduces possibilities of consequent panel degradation. It is basically a combination of two dc-dc buck-boost converters operating sequentially to generate an ac voltage output. Principle of operation and AC voltage generation is explained with the assistance of modal equivalents for both polarities of the ac voltage. Current programmed mode (CPM) based controllers designed to achieve the desired control constraints. Finally, experimental results under different load conditions and in grid connected mode are showcased to validate the performance of the inverter.

II.OPERATION PRINCIPLE OF THE INVERTER

Fig.1a shows the circuit schematic of the proposed single-phase buck-boost inverter in stand-alone mode, which consists of two inductors (L1, L2), two capacitors (C1 , C2), four MOSFETs (S1 -S4) and a power decoupling capacitor (Cin)to alleviate the low frequency input current (2nd harmonic) of the inverter. The input is output dc stage of any renewable power source, for instance PV, whose voltage, Vin, varies over a wide range. Input dc and output ac stages have one common terminal which alleviates the CMLC problem in grid connected applications. Fig.1b shows the inverter in grid-connected mode where Lg is grid side filter inductor.

Operation of the proposed inverter is described in two modes, Mode-1 and Mode-2, respectively, for positive and negative polarity of the output ac voltage. In Mode-1, S1 is considered as the main switch while in Mode-2 it is S2. Their conduction period is designated as ON time and the remaining duration of the switching period is designated as OFF time.

TABLE I SWITCH STATUS

	Vgs1	Vgs2	Vgs3	Vgs4
MODE1	S(t)	ON	OFF	S(t)
MODE2	OFF	S(t)	S(t)	ON

Switch status in each mode is summarized in TableI

Where vgs1,. . ., vgs4 represent gate drive signals of switchesS1,…, S4 , respectively.

A.MODE-1 (v2>0)

In this mode of operation, switch S2 is not triggered at all while switch S3 is made always conducting. The two-switch equivalent circuit of inverter is shown in Fig.2a which is similar to SEPIC converter. Switch S1 is triggered by the binary switching function (S) while switch S4 is triggered byte Boolean complement (S). All reference current directions and voltage polarities are indicated in the figure. The ON-and OFF-time equivalent circuits are shown in Fig.2b and 2c,respectively.

B. MODE-2 (v2<0)

During this mode, switch S1 is not triggered at all while switch S4 is always kept in conduction. Switches S2 and S3are gated with complementary PWM switching signals. The two-switch equivalent circuit is shown in Fig.2e, which is similar to canonical switching cell (CSC) with input side inductor, and ON and OFF time equivalent circuits are shown in Figs. 2f and 2g, respectively. It can be noticed that voltage across L1 and current through C2 is constant. Hence i1 andv2 do not have switching frequency ripple.

III. RESULTS AND DISCUSSIONS

A 300 W, 110 V, 50 Hz laboratory prototype is developed, as shown in Fig.12a, following the design rules mentioned earlier. The inverter parameters are presented in Table I. Control law and PWM generation are realized on an FPGA (Altera Cyclone-I) based digital platform. The recorded waveforms are in accordance with the steady state expressions derived. It is observed that the rms value of *i*2 is 4.9 A, which is approximately equal to the rated input current, but has a crest factor 2.45, which somewhat affects the size of *L*2. Hence, although a small increase in inductor losses occurs, this does not severely affect total losses. With a given MoSFET switch, the conduction loss is decided by the rms current, which is lower than the rated value, while the switching loss is somewhat increased due to the non-unity crest factor.

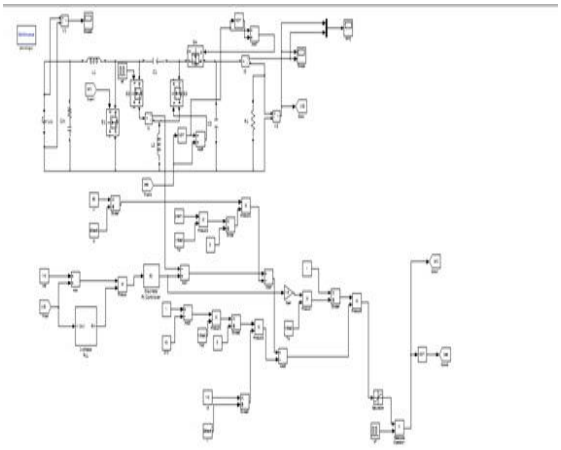

Fig 4. Circuit for PV mode

In this mode, *ig* is the outer loop control variable and controller (*Hg*) design follows the same rules as discussed in stand-alone mode. Thus to ensure a minimal specification set of PM=45◦ and BW=300 Hz, the required controller parameter set chosen for both stand-alone and grid-connected mode, are listed in Table.I. Fig.10a- 10d show the consequent variation in the outer loop-gain over the range of duty ratio [0, *Dmax*], at rated load. Slope of the phase plot, around BW, has an inverse relationship with PM, hence a robust design is ensured when the required PM is ensured for the steepest phase plot. Since this phase slope increase monotonically with *D*, controller design is based on the plant model at *D* = *Dmax*. Variation in BW and PM is observed to be monotonic, hence the values at the range limits, i.e. *D* = 0;*Dmax*, are listed in Table.I. Fig.11 shows the overall control schematic for stand-alone and grid-connected mode. In stand-alone mode, the output voltage error signal is multiplied with the reference voltage polarity before feeding to the controller block (*Hs*). In grid connected mode, the reference grid current, *igref* , is generated.

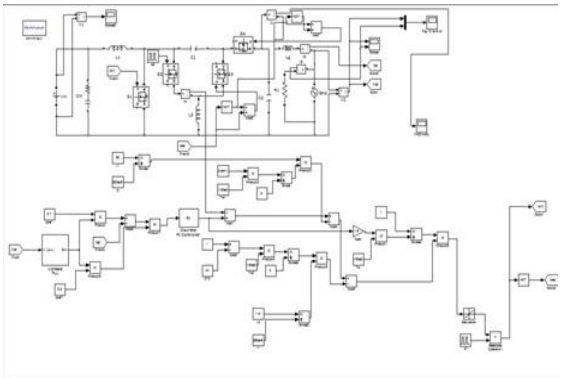

Fig 5. Voltage and Current equations in grid mode

With a given MoSFET switch, the conduction loss is decided by the rms current, which is lower than the rated value, while the switching loss is somewhat increased due to the non-unity crest factor. Fig 5 shows the experimental waveforms of the output voltage and current under four different conditions viz. 300 W resistive load (Fig. 13a), 200 W, 0.75 pf inductive load (Fig. 4), 200 W diode rectifier load with RL filter (Fig.4) and 250 W grid tied operation (Fig.5). Observed voltage THD values for resistive, inductive and non-linear loads are 2:7%, 3:6% and 4:1%, respectively. Fig.14a and 14b shows the output voltage frequency spectrum for resistive and non-linear loads, respectively. Fig 6 shows frequency spectrum of grid current in grid-connected mode which has THD of 4:3%. In all cases, the respective THD values are well within IEEE-519 limits.

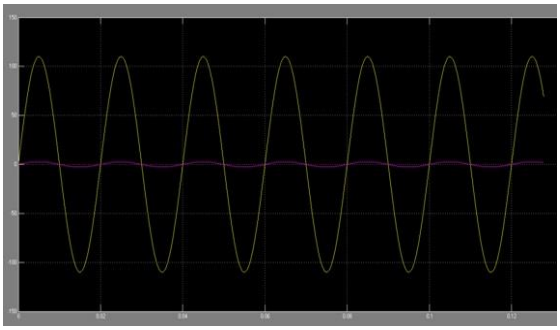

Fig 6. Waveform of Grid Current

Fig.6 illustrates transient performance under 50 W to 300 W step change at different points of output voltage i.e. positive half peak, zero-crossing and negative half peak. None of these load transitions show any distortion in output voltage, validating the PM specification used in control design. Fig.7 shows the efficiency curves, obtained by loss analysis calculations, for different input voltage and load conditions. Maximum efficiency of 95.70% is seen to be attained at rated load for 100 V dc input. It also shows the loss distribution among main components of inverter at rated load with 100 V input voltage. Among these losses, conduction loss of switches is the major contributor to total loss. Use of higher current rating switch like IRFP4868PBF (*rdson* = 22.5mΩ), instead of
FDA38N30 (*rdson* = 85mΩ), efficiency plots shown in Fig.1, increases maximum efficiency around 97%.

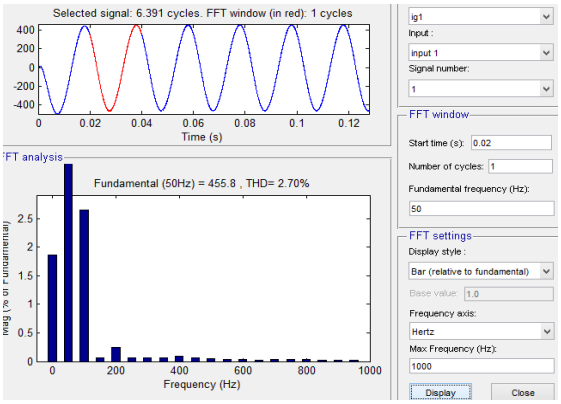

Fig 7. Harmonic order

Fig.7 shows the efficiency curves, obtained by loss analysis calculations, for different input voltage and load conditions. Maximum efficiency of 95.70% is seen to be attained at rated load for 100 V dc input. Among these losses, conduction loss of switches is the major contributor to total loss. Use of higher current rating switch like IRFP4868PBF (rdson = 22.5mΩ), instead of FDA38N30 (rdson = 85mΩ), efficiency plots shown in Fig.7, increases maximum efficiency around 97%. A comparison of the proposed inverter with recently reported single stage inverter topologies, of comparable rating, is presented in the design.

IV.CONCLUSION

This paper presents a new single-stage, single-phase, buck-boost inverter, with both input and output ports sharing a common terminal. This eliminates the problem of common mode voltage in grid connected PV applications, which helps to increase productive life of PV systems. It uses four switches and two inductors, which ensures minimum part count among reported topologies of comparable rating. Its bi-modal operation principle is explained in detail through steady-state and dynamic analyses. A two-loop controller structure is used, with the inner current loop realized by CPM. Outer loop design is based on a minimal constraint on phase-margin, applied to the set of small-signal plants derived from the large-signal inverter model. All controller design aspects are presented in detail. Power decoupling at low input voltage side requires a large Capacitor, which adds to the overall size and slightly increases cost. Design of the energy storage elements, loss and efficiency Calculations has been presented.

V.ACKNOWLEDGEMENTS

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