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An Improved 6-T SRAM For Better SNM And Minimum Average Power

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Abstract : **This improved approach has over came the Basic 6-T SRAM disadvantages and it has the improved butterfly curve and static noise margin nearer to the 8-T SRAM. This improved model is giving lower area utilization and lesser Average power consumption. This modern model is implemented in 180 nm technology and it had been implemented in cadence tool. In this paper I used 180 nm technology and supply voltage as 1.8 v and frequency 100 MHz to enable pass transistors and vcc. In this paper it explains the different mode of circuit and its operations with improved butterfly diagram.**

Keywords : Memory devices, SRAM, Average power, butterfly diagram, static noise margin, write circuit, read circuit, hold circuit frequency.

1.INTRODUCTION

The CMOS consists various technology of different methods to solve any type of problems we faced in the process of execution. These days the demand on chip capacity is increased to support demand I implemented new approach to the old method of 6-T SRAM. The new method is using two word lines instead of one word line which consists in Basic circuit.

In the Basic 6-T circuit cell unstable while performing read and write operations[1]. But, in this modern approach cell is stable by adjusting different operating points. The modern approach able to stand drawbacks of the Basic 6-T SRAM and it should perform read while read operation is executing similarly write while write operation performing. This modern approach able to give the better static noise margin than the Basic circuit. It gives the better butterfly diagram than the Basic circuit and similar to the 8-T SRAM circuit.

To achieve cell stability[2] for write operation we have to strengthen the pass transistors and weaken the storage inverters so that the write operation is performed. To achieve cell stability for read operation we have to weaken the pass transistors and strengthen the storage inverters so that the read operation is performed. To obtain the hold operation we should strengthen the both pass transistors and storage inverters so that hold operation can be performed.

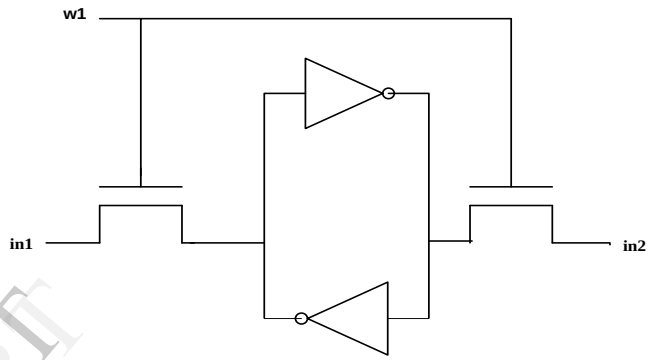

Figure - 1 Improved circuit

In a Basic 6-T SRAM variability tolerance had been compromised due to execution of read and write operation on the same pass transistors in the circuit[3]. Because, we were unable to perform the both read and write operation simultaneously at the pass transistor. The optimization of these both read and write circuits at a time is not possible in the Basic circuit so, I implemented the modern method to do better than the Basic circuit. In this method I developed read and write operations at different word lines. By enabling the two word lines and disabling them according to the requirement we can able to perform read, write and hold operation. Since, write and read operations are performed within the 6-T cell by manipulating different conditions of enabling word line according to the requirement[4].

This modern approach can be utilize like a Basic 6-T SRAM by enabling word lines on both sides. To obtain better results I adjusted the transistors w/l ratio such that better graph can obtain. For minimization of threshold voltage problems I fixed the supply voltage as 1.8 v. If we require less supply voltage we can able to adjust the supply voltage 1.8 to 0.8 any value we can put according to the requirement of the circuit and it has flexibility to adopt any voltage in this range[4]. In this work of improved model using two word line instead of one word line in the Basic circuit to obtain better results and achieving perfect butterfly diagram. The new method gives you low Average power, low voltage operation, better SNM to improve

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utilization of this circuit in wide variety of operations and applications. In this paper I explained about SRAM dc analysis with three different operations write circuit analysis, read circuit analysis, hold circuit analysis and mentioned about butterfly diagram.

2.MODERN 6-T CELL DESIGN

The standard 6-T cell design used for stability where it required. But, this modern 6-T cell design uses in the stability requirement and the application where it requires stability and improvement in terms of accurate and better butterfly diagram just similar to 8-T SRAM. The accurate butterfly diagram gives the less Average power means the signal is improved a lot.

The transient analysis gives us the circuit analysis of the analog signal in this we can able to see the function of the inverters and it`s waveform. Whether they are performing correctly or not if it needs some modifications we can make according to that. In this case we can able to see the circuit step by step performance. For the better results we can able to adjust the w/l ratio until we can get the better and desired results of the transient circuit. From this we can able to calculate the Average power and delay of this circuit. In the standard circuit the pass transistor is connected to the second input and other side of pass transistor is directly connected to the first inverter. But, practically it is not possible to connect directly while executing in the cadence warning is coming due to power over load so, I made the connection such that the line connected from the transistor to the inverter is divided and connected separately. Initially I got the problem of effecting the second voltage to the first inverter output and same as the first voltage is effecting the second inverter output but, it is nullified now.

2.1 Write Operation

In the write operation I enable the pass transistors to write the content in the inverters. To write that content we have to enable the pass transistor on one side to enter the data from one side, if we want other side we can follow the same procedure to enable the other side to write the data from other side. By this operation we can able to write the data in to the circuit.

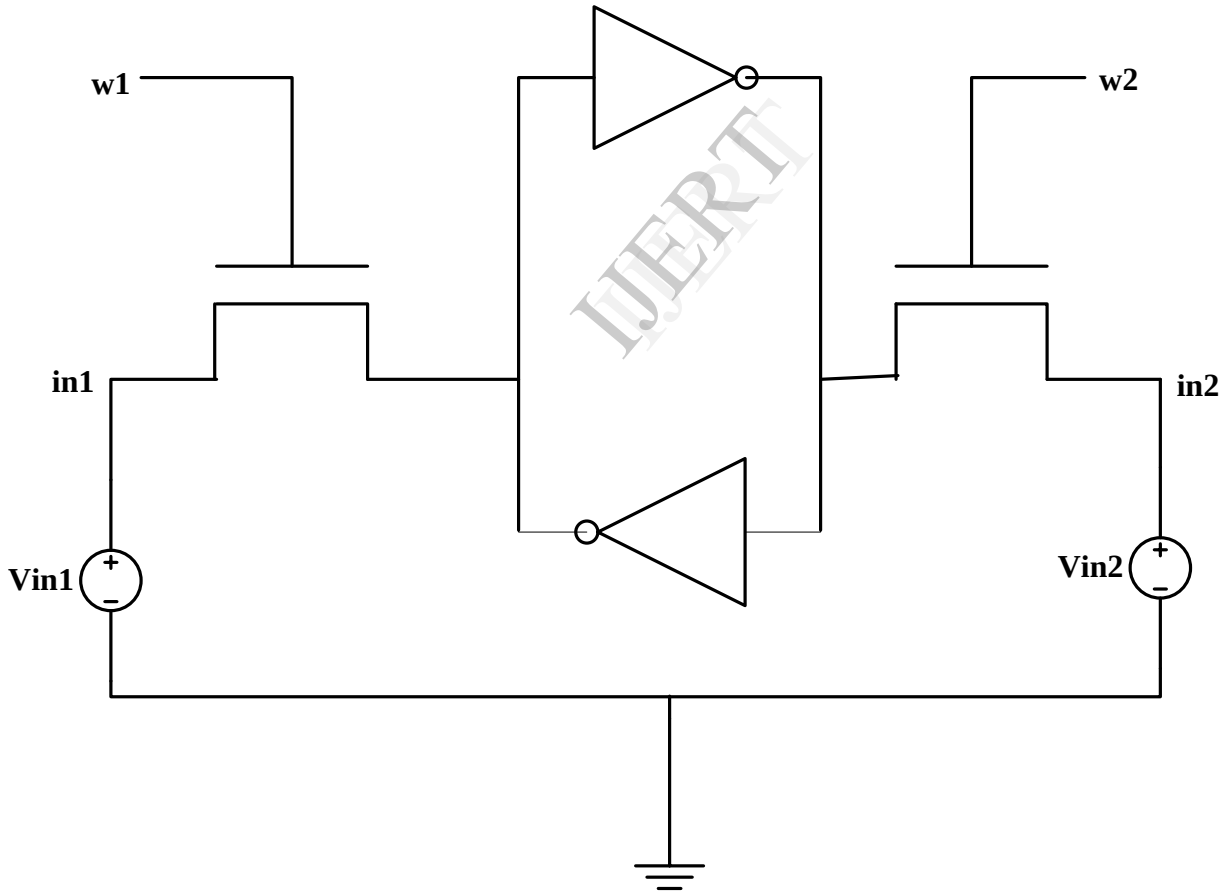

Figure - 2 Write circuit

In this Figure - 2 mention the supply of voltage 1 (Vin1) when the w1 active and similarly Vin2 is active when the w2 is active. In those only one condition is active at a time then we can get the better butterfly diagram.

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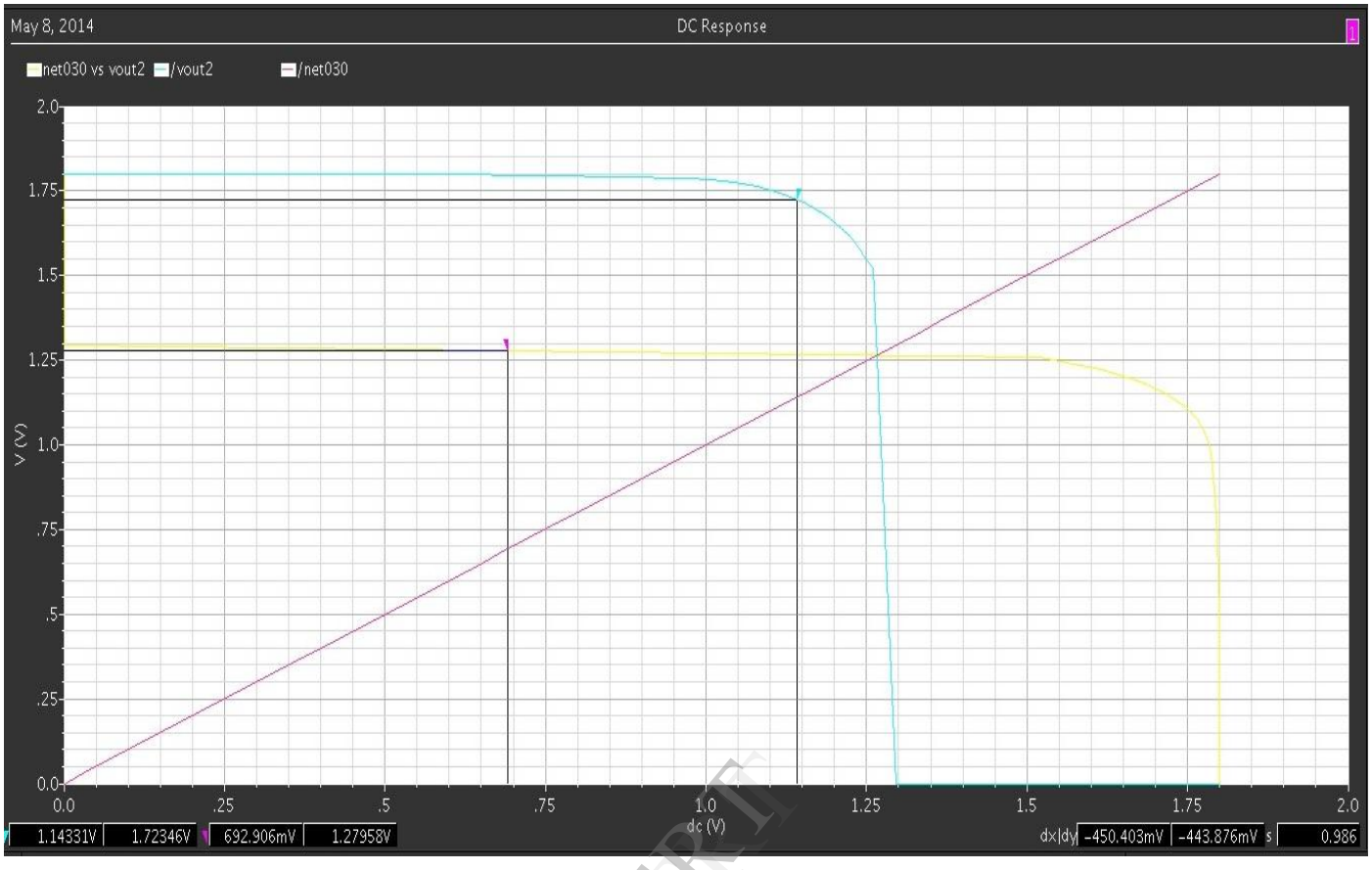

Figure - 3 Write waveform

SNM is calculated by maximum square of the butterfly diagram Figure - 3 indicates that concepts according to the procedure the calculation is required.

2.2 Read Operation

Read operation is the process of just opposite the write operation. In this process the content can be access in the pass transistor. The storage inverter is having the data from write operation what data we stored it we can able to access from read operation. Hear we can able to transfer data from storage inverter to either out1 side or out2 side we can able to access the data on any side of it. The operation performed in Figure - 4.

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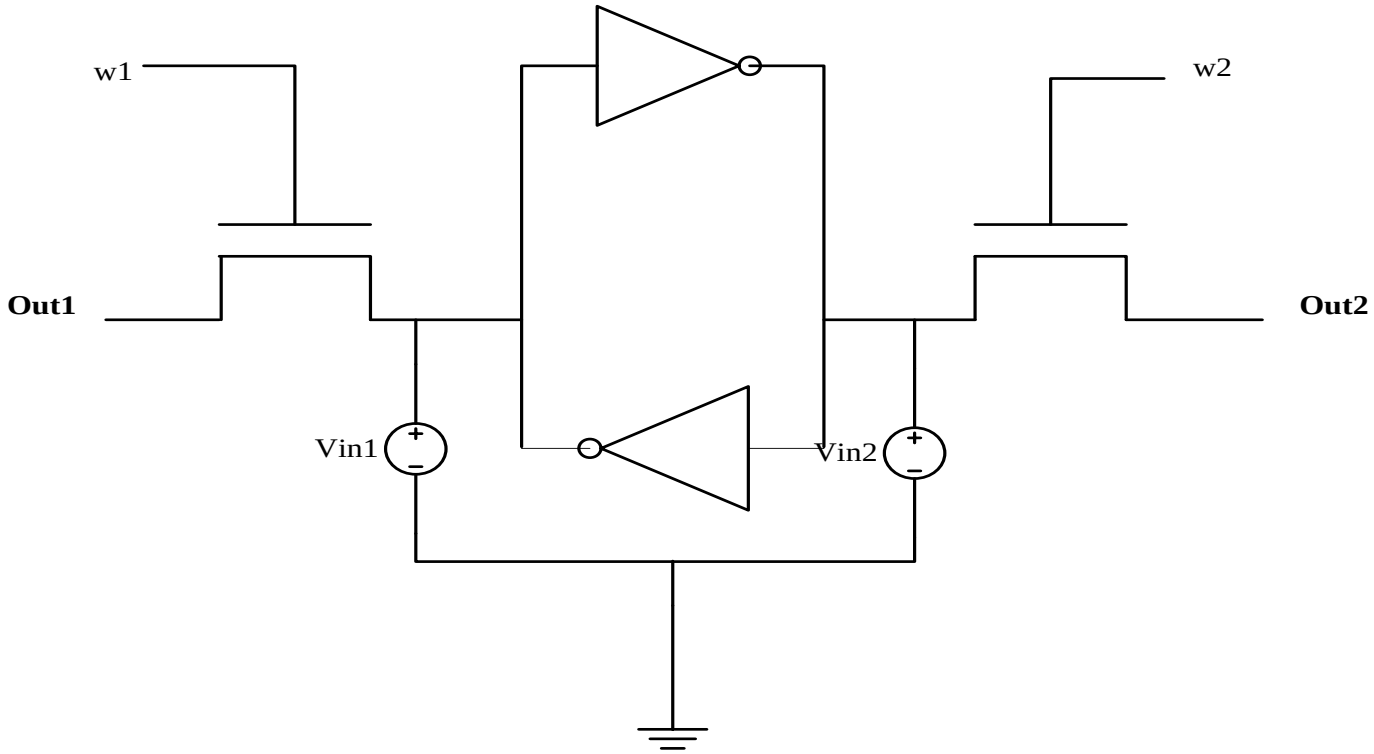

Figure - 4 Read circuit

2.3 Hold Operation

Hold operation is the one to keep the data on hold in this case the data not able to access it remains inaccessible to the user in this case the data is stored in the cell. This hold operation can preserve the data from cyber attacks and any unauthorised access.

In this Figure - 5 it describes the hold operation circuit in this we have to disable the pass transistor on both sides that means we have to disable the word lines. Then what ever the content inside the storage inverters it will remain hold.

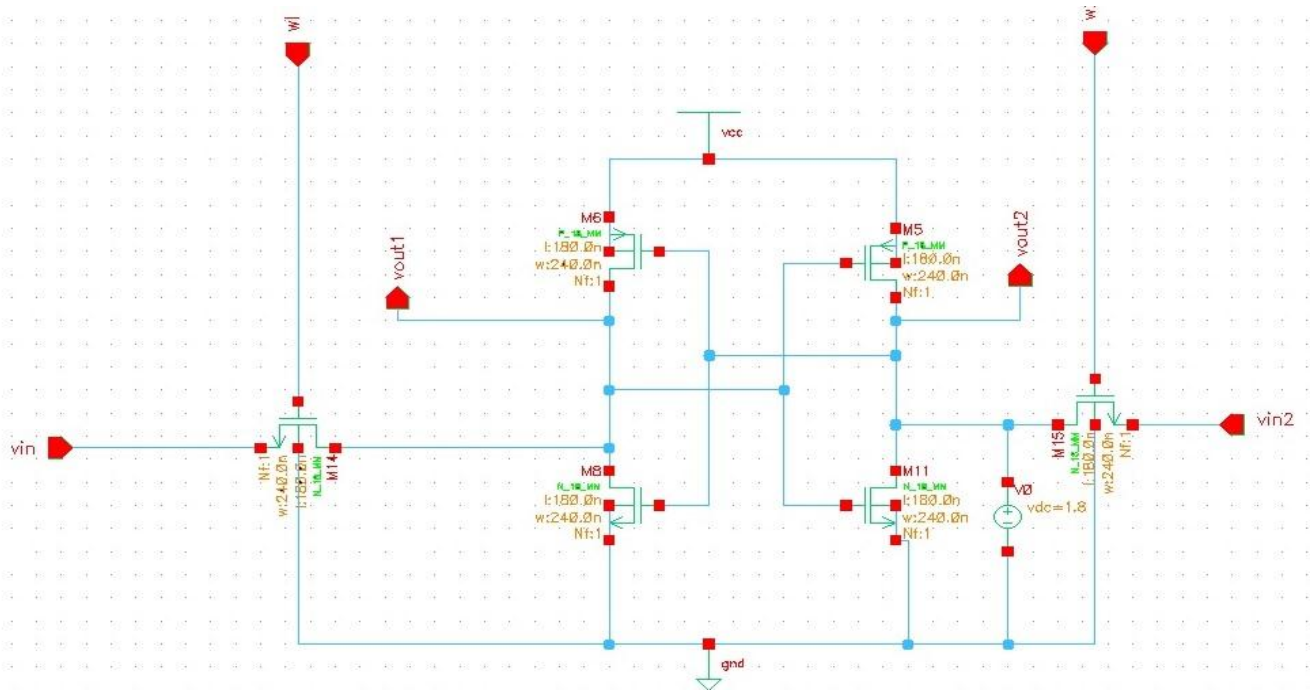

Figure - 5 Hold circuit

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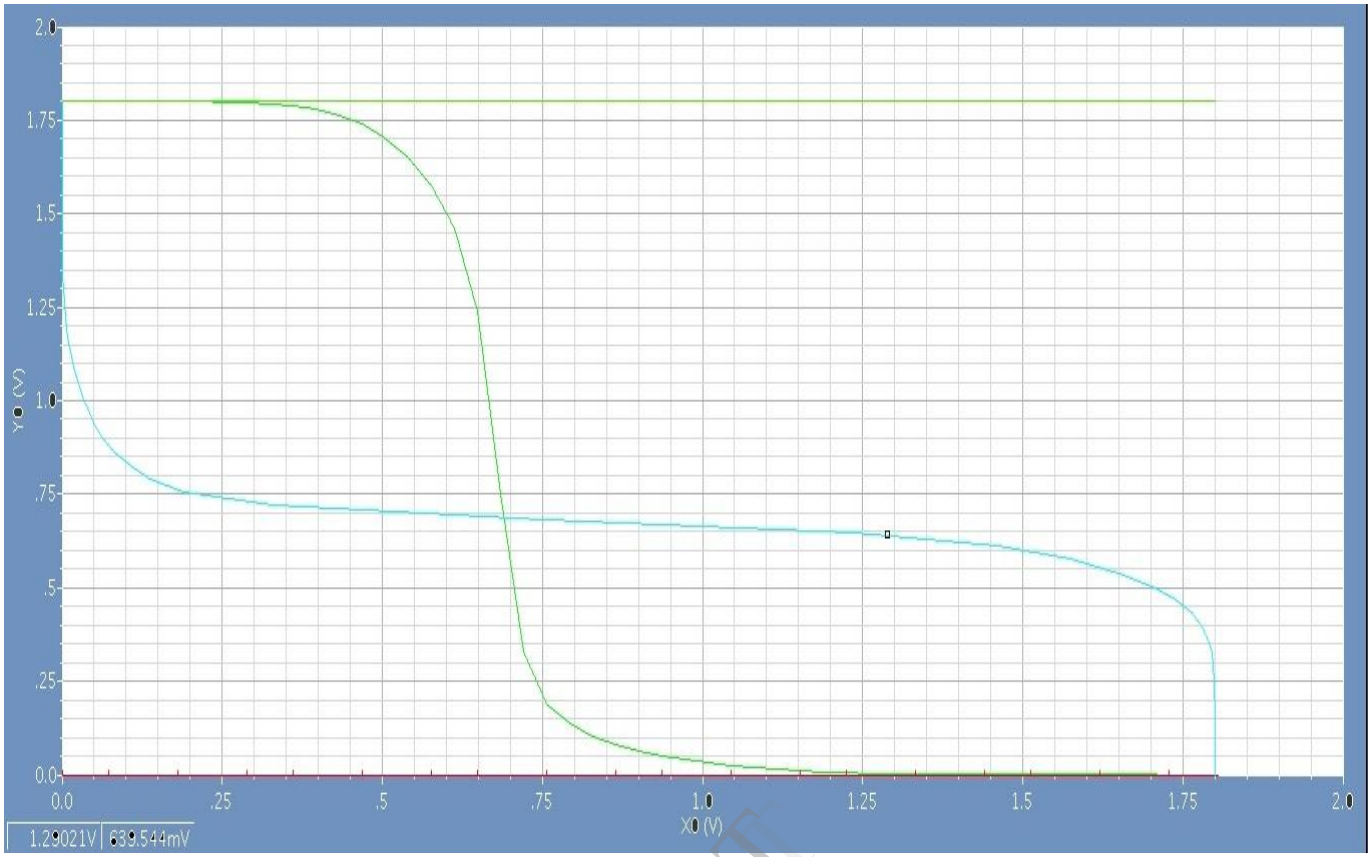

Figure - 6 Hold butterfly diagram

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In this Figure - 6 the better butterfly diagram displays from that we can able to calculate the SNM.

3.STATIC NOISE MARGIN (SNM)

In this section I am discussing about SNM for this we required butterfly diagram this diagram is depend on the various factors cell ratio, pull up ratio, supply voltage and also conditions like read, write, hold depend on the condition the butterfly diagram is changing. In this butterfly diagram to measure SNM we have to consider largest side of the square in the loop from that we can measure the diagonal that diagonal represent SNM[10]. To measure the SNM from that square we can use the formula.

$$SNM = \sqrt{s^2 + s^2} \quad (1)$$

s = side of the largest square in butterfly diagram.

THE RESULTS OF SNM

Position	Side	SNM
Top	0.5876	0.831
Bottom	0.6	0.848
Top	0.5	0.707
Bottom	0.3	0.424

Table - 1 SNM Results

Table - 1 indicates the SNM of the write circuit and hold circuit. If the SNM is more than the quality of the signal also good. So, we have to get the maximum SNM.

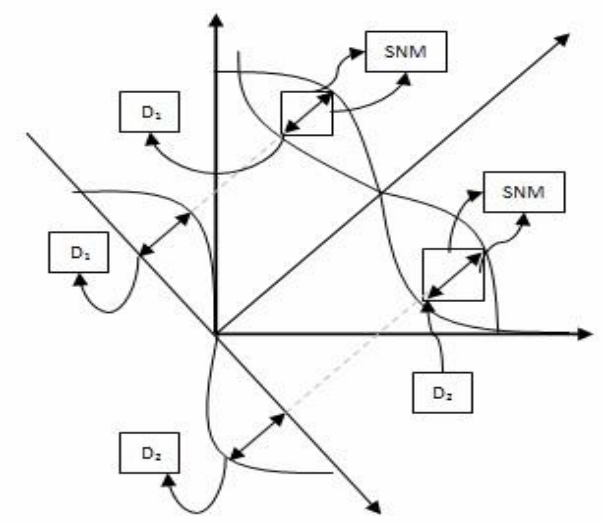

Figure - 7 SNM calculation

Figure - 7 indicates the calculation of SNM. In this figure it explains clearly we have to calculate the SNM of the butterfly diagram. In this diagram we have to calculate the diagonal of the maximum square possible in the loop[10].

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According to circuit we can get different shapes of curve and top side, bottom side may be different so, we can get different SNM then, we can count on the maximum SNM possible.

4. AVERAGE POWER

In the modern technology power consumption is the main criteria to utilization of the less power in the modern technology is required[14]. In the normal 6T SRAM the word line used only w but, in this we are using the two word lines w1 and w2 to make the better results.

By practical observation the below values are observed.

SRAM	Average power dissipation in transient.
8T SRAM	1.59E - 05
Basic SRAM	2.014E - 06
Improved SRAM	1.585E - 06
% Decrease 8T - Improved	90 %
% Decrease Based-Improved	21%

Table - 2 Average power

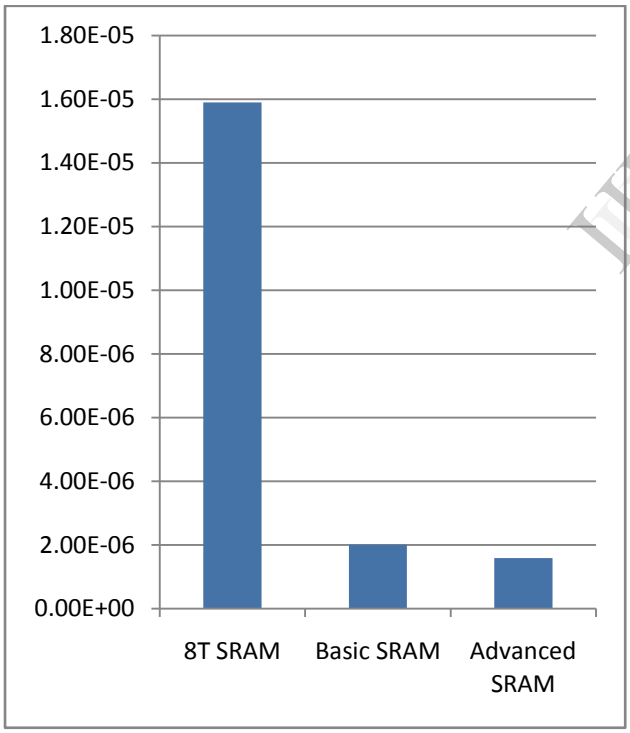

Table -3 Average Power

Table - 3 indicates the chart of table -2 how much the power utilization is decreased if the more power decreases than the Basic circuit then we can use our improved circuit in wide variety of application.

The Average power is decreased from the Basic SRAM to the improved SRAM is 90 % and the 8T SRAM to the improved SRAM is 21%. So, we can use this method interim of power utilization and better SNM of the circuit. By increasing scaling we can even reduces the power consumption and able to increases the wide applications for this circuit. According to (2) we can able to achieve less Average power from the Basic circuit by making inactive unused part.

5.TECHNOLOGY AND SCALING UTILIZATION

In this I utilized 180 nm technology for better results and even more utilization of Average power can be possible by using 65 nm technology we can able to achieve less Average power can be used with the improved technology The delay also reduces from the 65 nm technology compared to 180 nm technology[5],[7]. For more efficiency we can able to achieve by using 32 nm technology With improved technology we can able to achieve less delay and even less power also possible[6]. with improved scaling we can achieve less area than the Basic circuit.

6.CONCLUSION

This improved 6T SRAM gives the better Average power than the Basic 6T SRAM. This circuit is having several mode of operation and more flexibility towards the operating point and voltage variation we are free to use voltage range 0.8 to 1.8. The improved technology also minimizes the size of the device and everything it is mentioned. The cell size also we can decrease according to the requirement. The bit lines are independent so, we can able to achieve disturb free read and write operation in the improved SRAM according to the requirement we can able to manipulate the two word lines and we can achieve our requirement from this circuit. By latest technology and scaling factors the development of SNM and the improvement also can be possible by 32 nm technology.

7.FUTURE SCOPE

I implemented this analysis in 180 nm by giving the voltage of 1.8v. If the technology is increased that the voltage is minimized and power consumption can be obtained. The delay can be reduced by increased technology. Now a days this method is used in CNFET,FINFET. At present the latest technology is 7 nm technology by this high speed Micro processors able to built. If the technology increases the storage capacity increases by that we can able to design large storage memory units.

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8.REFERENCES

[1] An 8T-SRAM for Variability Tolerance and Low-Voltage Operation in High-Performance Caches Leland Chang, *Member, IEEE*, Robert K. Montoye, *Membe.*.

[2] A. J. Bhavnagarwala *et al.*, "The impact of intrinsic device fluctuationson CMOS SRAM cell stability," *IEEE J. Solid-State Circuits*, vol. 36,no. 4, pp. 658–665, Apr. 2001.

[3] J. Davis *et al.*, "A 5.6 GHz 64 kB dual-read data cache for thePOWER6™ processor," in *IEEE Int. Solid-State Circuits Conf.(ISSCC) Dig. Tech. Papers*, 2006, pp. 622–623.

[4] A. J. Bhavnagarwala *et al.*, "A transregional CMOSSRAMwith single,logic Vand dynamic power rails," in *Symp. VLSI Circuits Dig.*,2004, pp. 292–293.

[5] K. Zhang *et al.*, "A 3-GHz 70 Mb SRAM in 65nm CMOS technologywith integrated column-based dynamic power supply," in *IEEE Int.Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2005, pp.474–475.

[6] L. Chang *et al.*, "Stable SRAM cell design for the 32nm node and beyond,"in *Symp. VLSI Technology Dig.*, 2005, pp. 128–129.

[7] L. Chang *et al.*, "A 5.3GHz 8T-SRAM with operation down to 0.41 Vin 65 nm CMOS," in *Symp. VLSI Circuits Dig.*, 2007, pp. 252–253.

[8] K. Takeda *et al.*, "A read-static-noise-margin-free SRAM cell for low-VDD and high-speed applications," *IEEE J. Solid-State Circuits*,vol. 41, no. 1, pp. 113–121, Jan. 2006.

[9] B. Calhoun and A. Chandrakasan, "A 256 kb sub-threshold SRAM in65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig.Tech. Papers*, 2006

[10] E. Seevinck *et al.*, "Static-noise margin analysis of MOS SRAM cells,"*IEEE J. Solid-State Circuits*, vol. 22, no. 5, pp. 748–754, Oct. 1987.

[11] C. A. Adams and A. G. Aipperspach, "Methods and apparatus for accessingmemory," U.S. Patent 7,239,559. [12] R. Montoye *et al.*, "Adouble precision floating point multiply," in *IEEEInt. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2002, pp.336–337.

[13] W. K. Luk and R. H. Dennard, "Gated diode amplifiers," *IEEE Trans.Circuits and Systems II: Expr. Briefs*, vol. 52, no. 5, pp. 266–270, May2005.

[14] B. Sinharoy *et al.*, "POWER5 system microarchitecture," *IBM J. Res.Devel.*, vol. 49, no. 4/5, pp. 505–521, Jul./Sep. 2005.

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