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An Idea to Reduce the Power Consumption of Tablet in Low Power Mode.

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***Abstract*-Tablets and other mobile device requires long battery life. Nowadays it is attained by increasing battery size and using advanced technology batteries which in turn will increase the size, cost and weight of the final form factor. Additional increase in battery backup stays with the power controlling software which manage the underlying hardware to have a planned power supply to the components depending on the use case situation. This paper introduces a method to decrease the power consumption by a tablet to increase the battery back up by modifying the voltage of the components in the tablet to the lowest allowable voltage Vlow during low power state.**

Here we emphasize on the optimization method and discuss the expected power saving by optimizing 2.85V and 1.0V rails in a reference tablet.

Keywords: Standby, battery life, tablets, phones, power delivery

I. INTRODUCTION

Tablet is a basic requirement for most of us making it easy to be synced with fast-paced lifestyles. To do this efficiently, tablets' must have multitasking capability. They also have to be compact and have an increased battery life in order to keep working throughout the day.

Consumers now expect that a tablet should run efficiently for longer duration. Existing battery technologies are based on LI (Lithium-polymer) chemistry, which has helped increase battery life by keeping the battery size unchanged. Though greater capacity batteries can be used, this impacts the final product. Hence improving battery size and technology is not adequate to assure increase in battery backup of a tablet. Further, battery backup can be increased with the power management software that manage the underlying hardware to have a planned power supply to the components depending on the use case situation by switching the tablet power to the lower power states.

On other hand Battery backup depends on the system architecture, architects have to create an improved power consumption structure for each and every component in the tablet. As tablet stays most of the time in low power (standby) state, optimizing power intake from battery in this state will have a substantial influence on the battery life, there is scope of power optimization expected in the low power (standby) state and this paper tries to explore the power optimization that can be achieved.

II. PLANNED TECHNIQUE OF OPTIMIZATION

During low power state several components in the tablet are switched to sleep modes. In low power sleep mode, the current and potential difference to the components is reduced [2]. The magnitude of voltage will be determined by circumstance and the components connected. There is always a margin in the input voltage to the components from the voltage set by low power mode.

Now, in figure 1 let's look at the operating range v/s voltage for a component in a tablet.

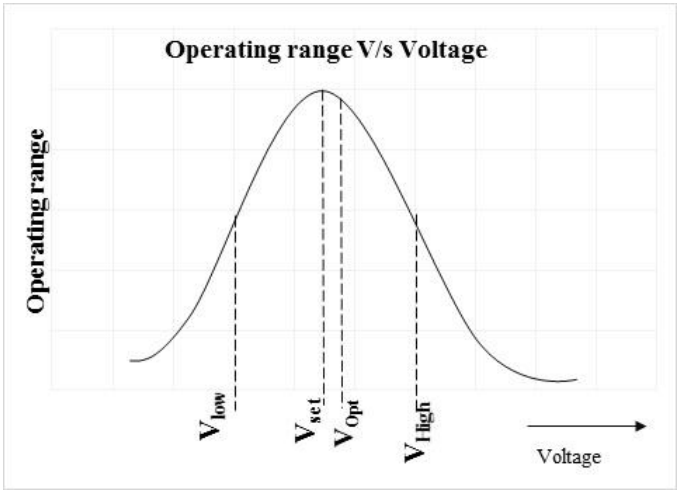

Figure 1: Operating range v/s Voltage

The power supply to the component is directed by the voltage regulator (VR) of that rail and this voltage regulator has to ideally supply V_{set} value required by the component, but in real applications voltage regulator is configured to supply V_{Opt} voltage, with V_{opt} greater than V_{set} in order to compensate the losses. From figure 1, looking at the voltage operating range of the component there is usually an allowable input voltage range, say this range is ±10% from the V_{set} value. This range is provided in order to bear the deviation in the input voltage after feeding losses and the leakage current. So for the

component to function properly with no abnormalities the voltage supplied to the module should be between V_{low} and V_{high}.

Now it's well-known that power [3] is given by

$$P = V*I \quad (1)$$

Where V = Voltage, I = Current

As explained earlier, current to the modules is reduced to the minimum value during the low power state.

Now, (1) for low power mode becomes

$$P_{low\text{-}power} = V*I_{low} \quad (2)$$

Where I_{low} is the low power state current and $P_{low\text{-}power}$ is the power consumption of the component in low power mode. Low power current is assumed to be constant in (2). Hence, $P_{low\text{-}power}$ would be proportional to voltage.

In (2) assuming I_{low} current to be constant

$$P_{low\text{-}power} \alpha V \quad (3)$$

And also transmission losses during low-power state is given by

$$Power\ Loss = I^2_{low} * R \quad (4)$$

Where I_{low} =Current, R=Resistance

As current is low, the losses is low and also the variation of voltage at the component is low. This allows us to decrease the voltage up to the lower allowable limit V_{low}.

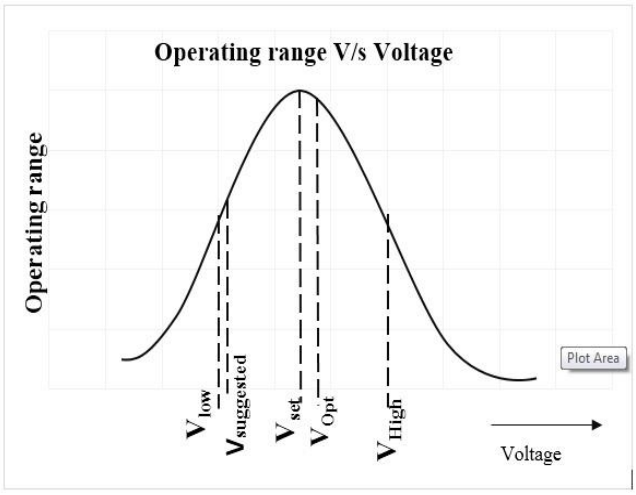

Figure 2: Proposed Operating Voltage Range

Now, idea is to reduce the voltage of the rail during low power mode to the value $V_{suggested}$ that is almost equal to V_{low} value as shown in figure 2. $V_{suggested}$ is still in the allowable safe operating voltage of the module. From (3), it can be inferred that decreasing voltage will decrease the power consumption by the component proportionally.

So far it was assumed that the current in low power state to be constant, now let's consider voltage and current dependency.

From leakage current equation of the semiconductor component [4],

$$I_{leak} = I_{sub\text{-}t} + I_{oxide} \quad (5)$$

$$I_{sub\text{-}t} = K_1 W e^{-V/nV\theta(1-e-V/V\theta)} \quad (6)$$

$$I_{oxide} = K_2 W \left\{\frac{V}{Tox}\right\} e^{-\alpha Tox/V} \quad (7)$$

From above equations it can be inferred that:

$$V \alpha I \quad (8)$$

Where V= voltage to the component and I= current to the component.

Hence ideally from (8) we can infer that by reducing the voltage, will proportionally reduce the current. This reduction will further contribute to the total power saving in low power state.

III. POWER SAVING EXPECTATION

To choose the percentage of voltage to be decreased on a particular rail needs a detailed analysis of the platform and the components connected on each rail and their behavior in low power mode. This paper tries to briefly analyze the rails that are 'ON' in low power mode and the modules on that particular rail. Firstly, let's understand the power tree of tablet during low power mode. Figure 3 is an indicative power map of a tablet during low power state [5] and the figure also indicates the components being active/partially active during the low power modes.

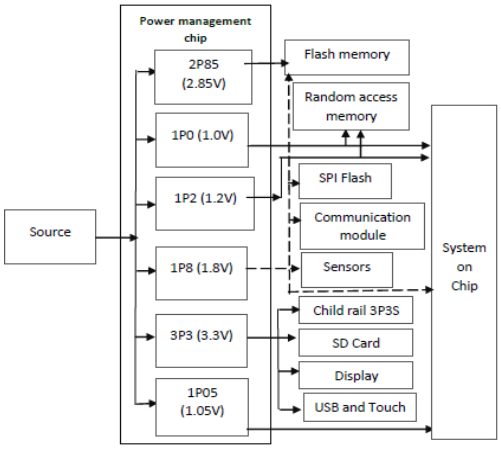

Figure 3: Reference Tablet Power tree in low power mode

From the above power tree it is observed that various components are on during low power sleep state, for experiment let's take up few rails from the figure 3 to optimize the power consumption.

Let's discuss the proportion of voltage that can be reduced and the expected power saving on each of the above mentioned rail.

A. Optimizing 2P85 Power Rail

During low power state flash memory is the only consumer on this rail and there is no flash memory access happening during low power mode. 1P8 rail supplying flash memory will take care of Self refresh of the memory. Hence, the proposal is to decrease the voltage of 2P85 rail to zero, that is turn OFF 2P85 rail in low power state to save the power.

So (1) Power consumption by 2P85 rail at V_{Opt} voltage is given by

$$P_{2P85} = V_{2P85} * I_{2P85} \quad (9)$$

Where $V_{2P85} = V_{Opt}$ voltage, I_{2P85} = Current in 2P85 rail at V_{opt} voltage.

1. Expected power saving:

In (1) substituting the value of voltage after 2P85 rail is turned off

$$P_{2.P85@0V} \approx 0W \quad (10)$$

Power saving expected is

$$P_{saving} = P_{2P85} - P_{2P85@0V} \approx 100\% \text{ of } P_{2P85} \quad (11)$$

So it can be ideally expected to have 100% power saving by turning off this rail, but practically the rail and leakage losses consume power. Yet, the power saving can be estimated to be near around 100%.

B. Optimizing 1P0 Power Rail

As the components on this rail are SOC and Random access memory (RAM), supply to this rail cannot be turned OFF. So, to optimize the power consumption by this rail during low power state we can decrease the voltage of this rail. According to the module's specification of RAM the tolerable low voltage V_{low} is 10% lower than the V_{set} (1.0V) value, i.e. 0.90V. Hence, during low power state the voltage can be reduced to 0.90V.

So (1) Power consumption by 1P0 rail at V_{Opt} voltage is given by

$$P_{1P0} = V_{1P0} * I_{1P0} \quad (12)$$

Where $V_{1P0} = V_{Opt}$ voltage, I_{1P0} = Current in 1P0 rail at V_{opt} voltage.

1. Expected power saving

V_{Opt} (operating voltage) of this rail is 1.05V and decreasing this voltage to 0.90V would be 14.28% decrease in the voltage. From (8) dropping voltage by 14.28% would decrease the current proportionately.

So (1) for Power consumption by 1P0 rail operating at 0.9V assuming current is reduced by 10%.

$$P_{1P0@0.9V} = V_{85.7\%} * I_{90\%.} \quad (13)$$

Power saving expected:

$$P_{saving} = P_{1P0} - P_{1P0@0.9V} \approx 24\% \text{ of } P_{1P0.} \quad (14)$$

Table 1 summarize expected power saving by the proposed method which is shown in table below.

TABLE 1. EXPECTED POWER SAVINGS.

Rail Name	V-set	V-opt	V-suggested	Expected power saving
2P85	2.85V	2.94V	0V	≈100%
1P0	1.0V	1.05V	0.90V	24%

IV. RESULTS

As a part of testing the proposed method, the rails mentioned above are subjected for optimization on a reference platform. A probing tool is used to poke the voltage regulator setting of these rails and decreases the voltage of these rails to the suggested voltage during low power state of the tablet. And the same tool was used to restores the voltage back to default value on low power mode exit. Table 2 summarize the rail level power measurement performed on the reference platform.

TABLE 2. ACTUAL POWER SAVINGS V/S EXPECTED POWER SAVING.

Rail Name	Voltage set			Expect'd power saving	Actual power saving
	Set (V)	*Operating (V)*	*Suggested (V)*		
2P85	2.85	2.94	0	≈100%	92%
1P0	1.0	1.05	0.90	24%	29%

Let's look at the impact of optimization on the voltage regulator efficiency,

TABLE 3. OPTIMIZATION IMPACT ON EFFICIENCY.

Rail Name	Before optimization	After optimization
2.85V_S	68%	NA
1.0V_A	82%	83.7

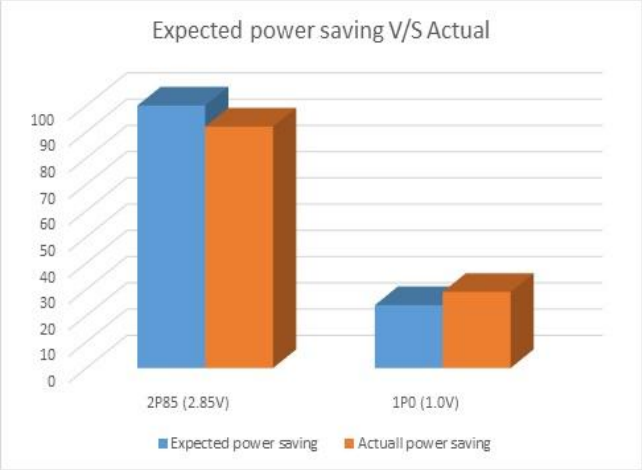

Figure 4: Power Saving Results

From table 2 and figure 4, in 2P85 rail there is small amount of increase in power consumed by the rail and component loss, so the actual power saving is bit lower than expected value. And in 1P0 the power saving is greater than the expected value as the efficiency of this voltage regulator is increased that has contributed to the increase in power saving.

Power saving contribution of these individual rail to the total platform power

$$P_{Total\_saving}=P_{Default}-P_{Optimized} \quad (15)$$

Where,$P_{Default=}$ Total platform power consumption before optimization and $P_{Optimized=}$ Total platform power consumption after optimization

It is observed that total power saving contributed by 2P85 and 1P0 rails to the overall platform (battery terminal) power consumption is around 2%

V. CONCULSION

The proposed method has been experimented in view of optimizing the power consumption and to increase the battery backup in Tablets during the low power mode. Based on theoretical calculations and the actual power measurements on the reference device, we can conclude that the proposed method will contribute around 2% of reduction in total platform power consumption during low power mode that is the proposed method can increase the battery backup of a tablet by around 2% during low power standby mode.

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