Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 8 Issue 07, July-2019

An Efficient VLSI Implementation of BIST based on Secure Scan Cell Logic

Neethu Shankar R S
M. Tech Scholar
Dr. Ambedkar Institute of technology
Bengaluru-560056, India

Mrs. B S Sudha
Associate Professor
Dr. Ambedkar Institute of technology
Bengaluru-560056, India

***Abstract*—BIST is a type of testing process which makes the machine to test by itself. BIST is one of the method in design for testability (DFT) technology. It is an establishment of circuits for the generation of test pattern which is used for testing of functions and comparison of functionality of circuits. BIST basically contains hardware test pattern generator for the purpose of generating the test patterns, circuit under test unit, output response compactor, Test controller unit, ROM, Input response unit which contains scan chains which contains the logic circuits and produces the corresponding outputs. In the proposed method these scan chains are replaced by secure cell which gives more security and also by the use of secure cell in the place of scan chain the power consumption greatly reduces and also the it gives less delay when compare to existing scan chain. Since BIST is used broadly to test the circuits the power and the delay are the two important factor that should be considered by the BIST designer, So in the proposed system secure cell is used in the place of scan chain to get better results. The proposed method has much resistance to the security attacks. The proposed secure cell based BIST is implemented by using verilog HDL language and the modelsim software is used for the simulation and the synthesis is done by using Xilinx and spartan 3 XC 3S 200 TQ 144.**

***Index Terms*— BIST, test pattern, Xilinx, modelsim.**

1. INTRODUCTION

Every circuit which is designed will not be error free there will be some errors occur in the chip after fabrication. These errors will cause the circuit to change its functionality or the circuit will not work properly. So to solve this problem BIST is used in every circuit. BIST is a method of testing the circuit for the errors; The separate design will be included in the circuit design called as BIST. This makes the circuit to test by itself by generating the pseudo random test patterns. The BIST is a method of DFT technique where DFT or design for testability. It is a technique which is used for testing the correctness of the circuits, The basic operation of the BIST is first it produces the pseudo random test patterns by using pseudo random test pattern generator this pattern generator it uses shift register, LFSR, phase shifter to generate the test patterns and then these test patterns are assigned to each secure cell, the test pattern for each secure cell is unique and also the test patterns will not be repeated again. The CUT or circuit under test unit consisting of circuit to be tested and also there output is stored. The ROM unit consists of standard circuit signature or output. The output response compacter as shown in the figure 1 it performs the compression of the output of the CUT circuit to a signature and the comparator compares circuit under test signature and the standard circuit signature if the signature matches it gives the output as 1 and if the signature does not matches it give the output as 0 this comparator it consists of series of xor gates. The test controller controls the complete operation of the BIST.

- Test controller
- Hardware test pattern generator
- Input multiplexer
- CUT or Circuit under test
- Output response compacter
- Comparator
- ROM

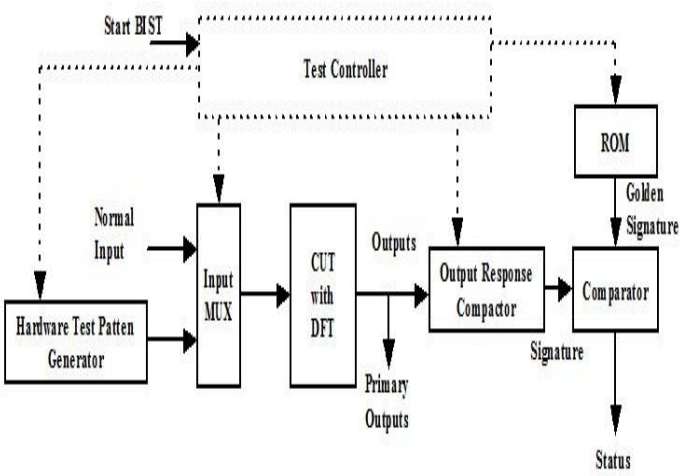

Figure 1: Basic BIST architecture

PRPG or Pseudo-Random Pattern Generator generates the pseudo test patterns that are required to run the device based on this test patterns the CUT operates and gives the output to the MISR or it is also called output response analyzer. The pseudo random test pattern generator consists of shift register, LFSR and Phase shifter which are used for generation of test patterns required for CUT circuit.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 8 Issue 07, July-2019

MISR or Multi-Input Signature Register is also called as output response analyzer which analyses the output from the CUT circuit. The output of the device for which pseudo random test patterns are given as input become the input for the MISR where this device analyzes the output of the CUT circuit and the output stored in the memory for the correctness. After analyzing MISR gives the output as 1 if the functionality of both the circuit matches and it gives 0 if both the circuit functionality dies not matches.

Since the MIST give the output as 1 and 0 based upon the analysis of the output of the device with input pattern and output of the circuit in the memory hence it is also called as output analyzer.

Master LBIST controller controllers the operation of the LBIST, The main operation of this controller is control of clock propagation, Initialization, Directing the test patterns to the particular secure cell for further operation.

2. PROPOSED SYSTEM

The proposed BIST architecture is based upon the implementation of secure cell logic in the BIST architecture. Where in the existing system at the input response this BIST architecture consisting of scan chains but in the proposed method the scan chains are replaced by the secure cell. By using this secure cell there is a great reduce in the power consumption and also the bist architecture gives the less delay when compare to excising system. In the proposed system the secure cell is having higher resistance to the security attacks. The proposed BIST architecture is shown in the figure 2. The secure cell which is used in the proposed BIST architecture is shown in the figure 3.The shadow register which is used in the BIST performs the input bit storage and the LFSR which will perform the generation of input bits these bits will be stored in the shift register and these stored bits will be driven to the phase shifter. The Phase shifter drives the multiple secure cells with a single phase. The already produced pseudo test patterns will not be the repeated patterns instead they are unlike to each other for a particular secure cell. It is also represented by the two different phases they are weighed pseudo random testing phase (phase=0) and the deterministic BIST phase (phase=1)

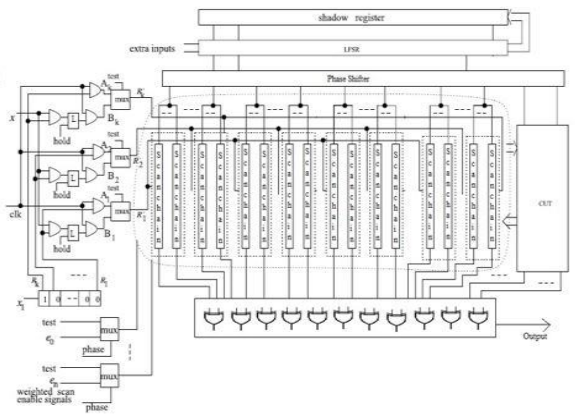

Figure 2: Proposed low power BIST based secure cell architecture

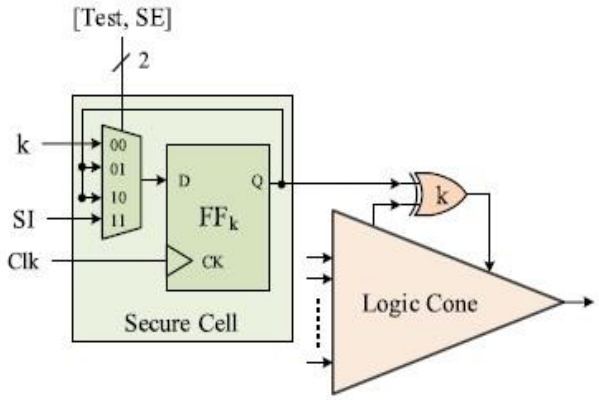

Figure 3: Secure cell architecture

In this method different secure cells are assigned to different weights. By using this technique it greatly reduces the size of phase shifter. Here each stage drives the one secure cell.

The compactor forms the signature by compressing the bits and the standard signature which is stored in the CUT unit of the BIST is compared with the signature that is generated by the compacter. The CUT unit is circuit under test unit where it consisting of the circuits whose functionality has zero errors. The BIST circuit also consists of XOR network whose output is 1 if the comparison of the signature is same and its output is 0 if there is a difference in the comparison of the signatures.

3. SIMULATION RESULTS

The simulation of the proposed system is performed using a tool called modelsim and the synthesis is done by using the Xilinx tool. The simulation of the proposed system is done for both fault circuit and without fault circuit. The simulation results for both fault and without fault is shown in the figure 3 and figure 4. As shown in figure 3 it represent the output of BIST for the fault circuit, In the proposed system the simulation is done for the adder circuit so in the figure 3 it should give the output by adding the inputs A and B, The output in the figure 3 is named as test circuit output which is giving the wrong results by the addition of two inputs A and B. So this represents that, there is fault in the given circuit. The figure 3 also shows the output of the LFSR, CUT circuit output, MISR output. In figure 3 by the addition of inputs A and B correct results of addition should get at the test circuit output but we are getting wrong results there so this shows that there a one bit error in the circuit.

In the figure 4 it represent the simulation results with no faults because as shown in figure 4, For the inputs A and B the output of addition at test circuit output is correct with no errors so the figure 4 is said to be simulation with no faults. This result represents that the given circuit in the CUT is having correct functionality when compared to the standard circuit.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 8 Issue 07, July-2019

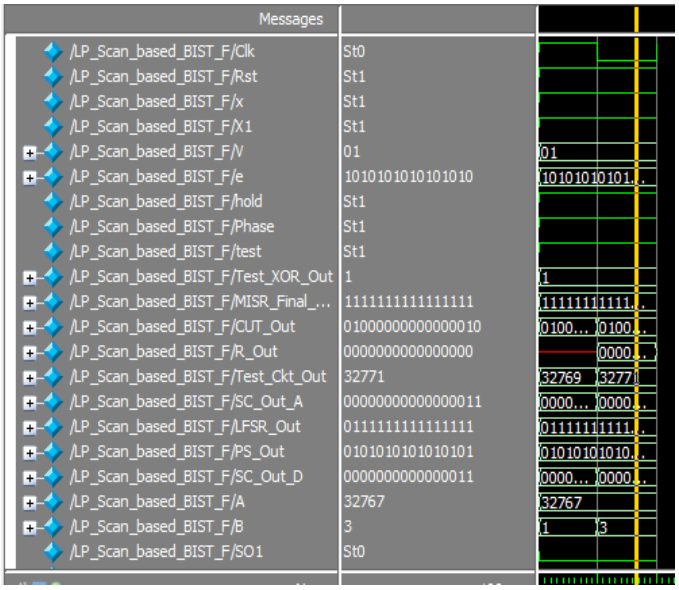

Figure 5: simulation of with fault output.

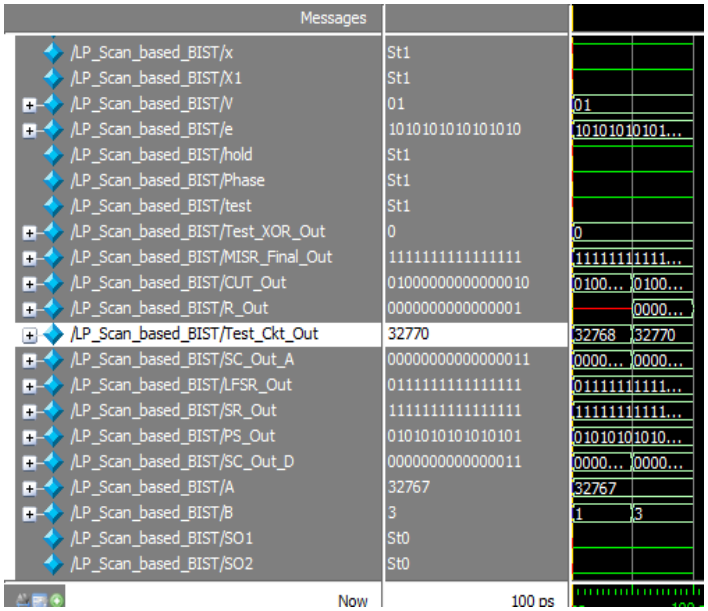

Figure 4: Simulation of without fault output

4. COMPARISION TABLE

BIST DESIGN	EXISTING DESIGN	PROPOSED DESIGN
LUT	88	80
Slices	67	62
Gate Count	1024	909
Delay	20.61ns	20.563ns
Gate or Logic delay	10.682ns	10.682ns
Path or Route delay	9.934ns	9.881ns
Power	338.44 mW	225.63 mW

Table 1: Comparison of proposed system and existing system.

The table 1 represents the comparison between the proposed secure cell based BIST and the excising scan chain based BIST. According to this comparison table, the proposed system gives better results when compared to excising system. The required number of LUT for the proposed system is 80 and for the exciting system is 88 which is greatly reduced in the proposed system and also slices and gate count is also reduced in the proposed system. Delay of the proposed system is 20.563ns and for existing system is 20.61 which is slightly reduced in the proposed system but the power consumed in the proposed system is 225.63mw and in the exciting system is 338.44mw where the power consumption is greatly reduce in the proposed method.

5. CONCLUSION

In the proposed system the Pseudo test pattern generator is used to produce the test pattern. The new separate test phases are used they are LP weight pseudo test pattern generation and the LP deterministic BIST. The initial phase selects the pseudo test pattern generation to reduce the random patters that used as the inputs. The test patterns are generated by the LFSR that are selected by the primitive polynomial and the separate inputs are given externally to the LFSR. The security cell reduces the delay time of the output produced and also it is faster. The result of the proposed system is compared with the existing system.

REFERENCES

[1] M. Filipek et al., “Low-power programmable PRPG with test compression capabilities,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 6, pp. 1063–1076, Jun. 2015.

[2] N. Z. Basturkmen, S. M. Reddy, and I. Pomeranz, “A low power pseudorandom BIST technique,” J. Electron. Test., Theory Appl., vol. 19, no. 6, pp. 637–644, Dec. 2003.

[3] A.S. Abu-Issa and S. F. Quigley, “Bit-swapping LFSR and scan-chain ordering: A novel technique for peak- and average-power reduction in scan-based BIST,” IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol. 28, no. 5, pp. 755–759, May 2009.

[4] A. Al-Yamani, N. Devta-Prasanna, E. Chmelar, M. Grinchuk, and A. Gunda, “Scan test cost and power reduction through systematic scan reconfiguration,” IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol. 26, no. 5, pp. 907–918, May 2007.

[5] Y. Huang, I. Pomeranz, S. M. Reddy, and J. Rajski, “Improving the proportion of at-speed tests in scan BIST,” in Proc. IEEE/ACM Int. Conf. Comput.-Aided Design, Nov. 2000, pp. 459–463.

[6] R. Kapur, S. Patil, T. J. Snethen, and T. W. Williams, “A weighted random pattern test generation system,” IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol. 15, no. 8, pp. 1020–1025, Aug. 1996

[7] Z. Jiang, D. Xiang, and K. Shen, “A novel scan segmentation design for power controllability and reduction in at-speed test,” in Proc. Asian Test Symp., Nov. 2015, pp. 7–12.

[8] R. Kapur, S. Patil, T. J. Snethen, and T. W. Williams, “A weighted random pattern test generation system,” IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol. 15, no. 8, pp. 1020–1025, Aug. 1996.

[9] G. Kiefer and H.-J. Wunderlich, “Deterministic BIST with multiple scan chains,” J. Electron. Test., vol. 14, no. 1, pp. 85–93, Feb. 1999.

[10] Y. Huang, I. Pomeranz, S. M. Reddy, and J. Rajski, “Improving the proportion of at-speed tests in scan BIST,” in Proc. IEEE/ACM Int. Conf. Comput.-Aided Design, Nov. 2000, pp. 459–463.

[11] S. Hellebrand, H.-G. Liang, and H.-J. Wunderlich, “A mixed mode BIST scheme based on reseeding of folding counters,” in Proc. Int. Test Conf., Oct. 2000, pp. 778–784.