An Efficient Low Leakage 1-bit Nano-CMOS based Full Adder Cells for Mobile Applications

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Abstract

A new technique for implementing low leakage 1-bit nano cmos based full adder cells for mobile applications is introduced here. The new technique employs a new transistor resizing approach for 1bit full adder cells to determine the optimal sleep transistor size which reduce the leakage power. The simulations are performed using tsmc 0.18 µm technology

Keywords—Low leakage power; Noise Margin; Ground bounce noise; Sleep transistor and Adder cell.

1. Introduction

Adders are heart of computational circuits and many complex arithmetic circuits are based on the addition .The vast use of this operation in arithmetic functions attracts a lot of researcher's attention to adder for mobile applications. In recent years, different logic styles have been proposed to implement 1-bit adder cells. The main aim of these adder cells is to reduce power consumption and increase speed. These studies have also carried out a systematic inquiry into different approaches realizing adders using CMOS technology [3].

For mobile applications, designers have to work within a very tight leakage power specification in order to meet product battery life and package cost objectives. The designer's concern for the level of leakage current is related to minimize power dissipation. For portable electronic devices this is equal to maximizing battery life. For example, mobile phones need to be powered for extended periods, but are fully active for much shorter periods.

Shortening the gate length of a transistor increases its power consumption due to the increased leakage current between the transistors source and drain when no signal voltage is applied at the gate. In addition to this, gate tunneling current also increases due to the scaling of gate oxide thickness. Hence, it has become extremely important to develop design techniques to reduce static power dissipation during periods of Inactivity. The power reduction must be achieved without trading-off performance. Because it makes harder to reduce leakage during normal operation. There are several techniques to reduce leakage power.

Power gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground [2].This device is turned off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides a substantial reduction in leakage at a minimal impact on performance [1].

This paper focuses on reducing sub threshold leakage power consumption.The remainder of this paper is organized as follows.In section II,proposed nano-CMOS full adder circuits,and its equivalent circuits are discussed.In section III,the performance analysis and simulation results of conventional CMOS full adder cell and proposed circuits are explained.Then the paper is summarized in section IV.

2. Proposed full adder circuits

Recently, power dissipation has become an important concern and considerable emphasis is placed on understanding the sources of power and approaches to dealing with power dissipation.

Static logic style gives robustness against noise effects, so automatically provides a reliable operation. Pseudo NMOS and Pass transistor logic can reduce the number of transistors required to implement a given logic function. But those suffer from static power dissipation. Implementing Multiplexers and XOR based circuits are advantageous when implement by the pass transistor logic. On the other hand, dynamic logic implementation of complex function requires a small silicon area but charge leakage and charge refreshing are required which reduces the frequency of operation. In general, none of the mentioned styles can compete with CMOS style in robustness and stability.

Fig 1 shows the conventional CMOS 28 transistor adder schematic diagram [2].This is considered as a Base case throughout this
paper. All comparisons are done with Base case.The CMOS structure consist of PMOS pull up and NMOS pull down networks to produce considered outputs

Transistor sizes are specified as a ratio of Width/Length (W/L). The sizing of transistors plays a key role in static CMOS style. In the conventional adder circuit, the transistor ratio of PMOS to NMOS is 2 for an inverter and remaining blocks also followed the same ratios when considered the remaining blocks as equivalent inverters. Modified adder circuits with sizing are proposed in Design1 and Design2.

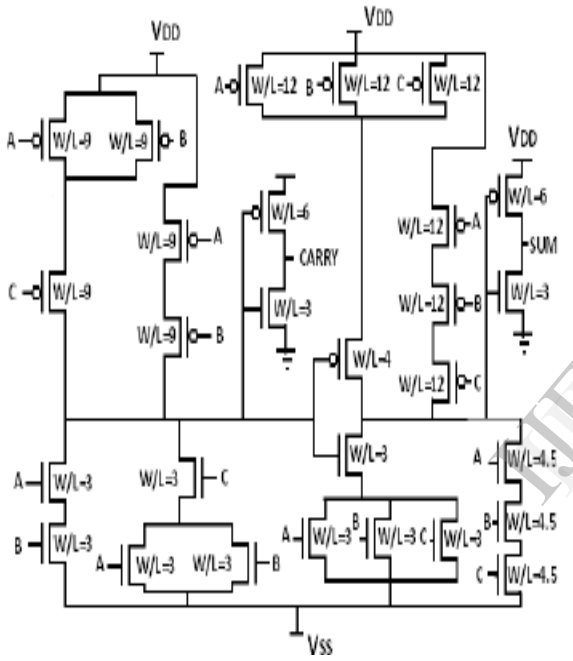

Figure 1.Conventional CMOS full adder

Further,power gating technique is used to reduce the leakage power,where sleep transistor is connected between actual ground rail and circuit ground.

Modified sizings are shown in Fig. 2 and Fig. 5 respectively. The sizing of each block is based on the following assumption.

Base case is considered as individual block as shown in Fig. 3. Each block has been treated as an inverter.Each block have the same inverter ratio. These sizing will reduce the standby leakage current greatly because sub threshold current is directly proportional to the Width/Length ratio of transistor. As size reduces the area occupied by the circuit will also reduce. This will reduce the silicon chip area and there will be a reduction in the cost.

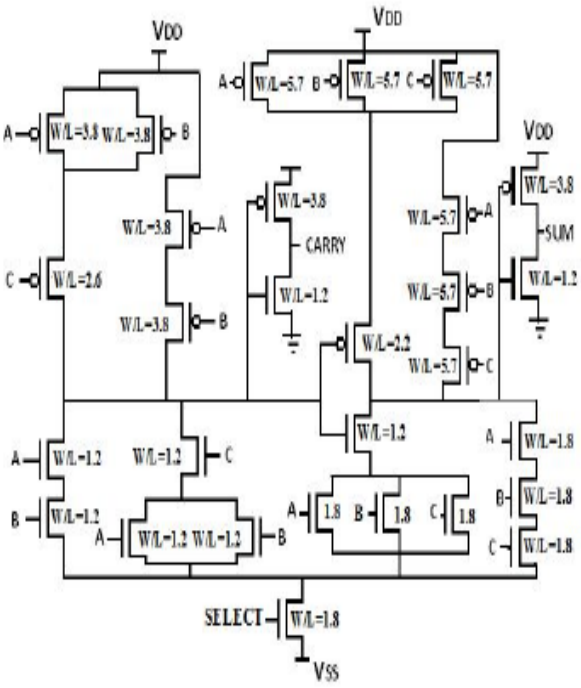

Figure 2. Proposed full adder (design1) circuit with sleep transistor

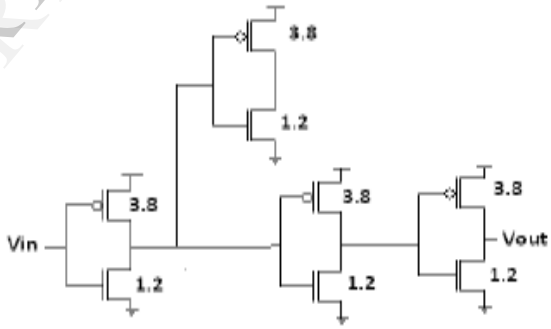

Figure 3.Equivalent circuit for design 1

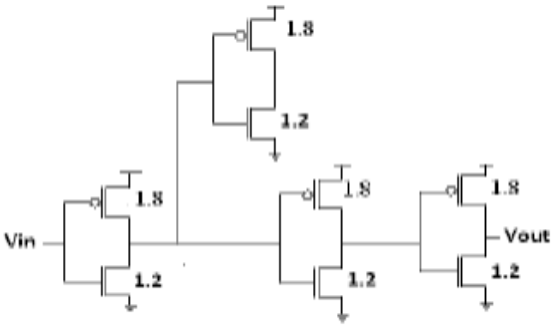

Figure 4. Equivalent circuit for design 2

Modified adder circuit i.e. Design2 shown in Fig. 5, the W/L ratio of PMOS is 1.5 times that of W/L ratio of NMOS and each block has been treated as an

equivalent inverter. The same inverter size has been maintained on each block as shown in the Fig. 4. The goal of this design is to reduce the standby leakage power.

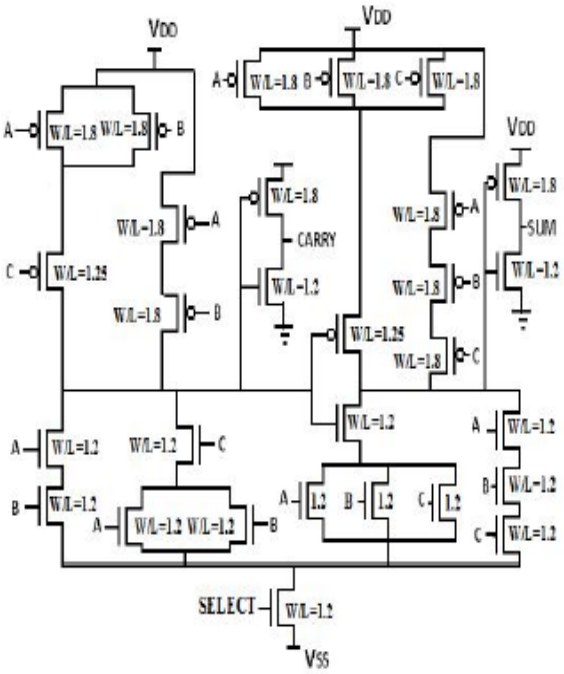

Figure 5. Proposed full adder (design2) circuit with sleep transistor

3. Performance analysis and simulation results

I have performed post layout simulations using Mentor Graphics EDA tool and the technology being employed for simulation is tsmc 0.18 µm technology.

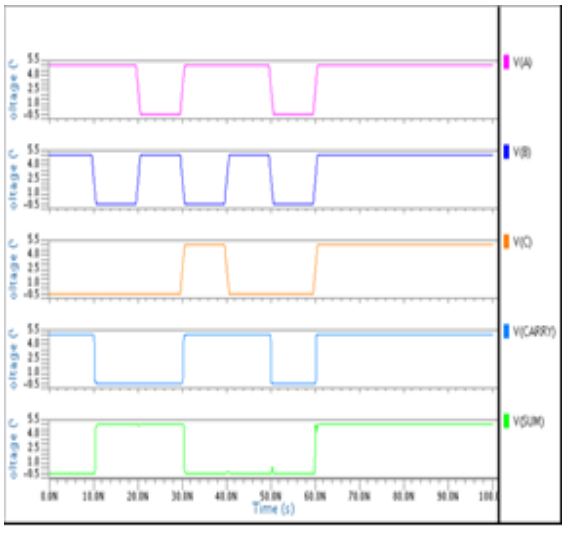

Figure 6. Conventional CMOS full adder waveform

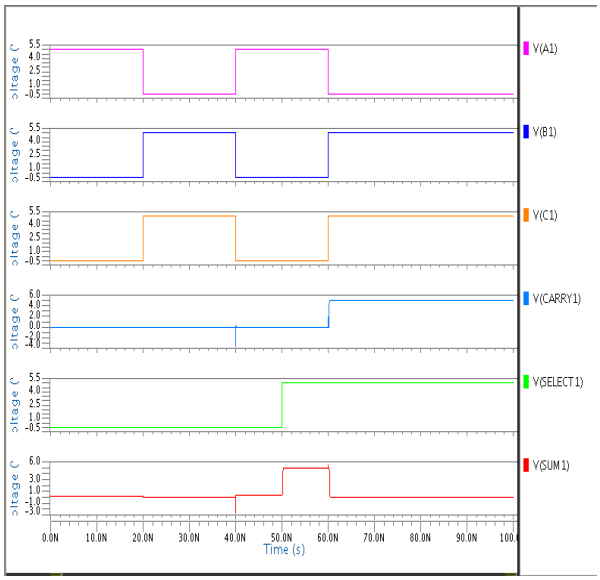

Figure 7. Proposed full adder (design1) waveform

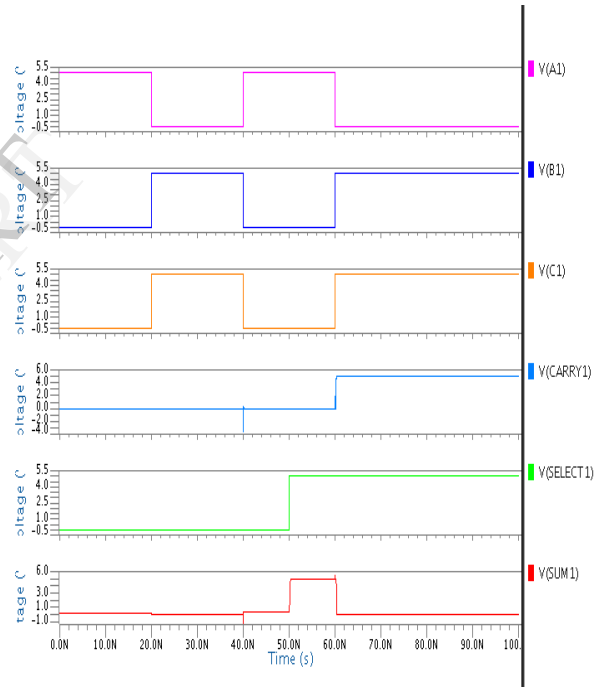

Figure 8. Proposed full adder (design2) waveform

The power dissipated by the circuit when the circuit is in active state is referred to as active power. Active power is measured by giving input vectors and calculating the average power dissipation during this time. Considered simulation time to calculate active power is 50ns. Input vectors have been given in such a way that it covers almost all input vector combinations. The same vectors and simulation time has been given to Base case to compare the results. This active power includes dynamic power as well as the static power so it is being named as an active power.

Table 1. Active power dissipation of 1-bit full adder cells

Design name	Base case	Design1	Design2
Active power(PW)	986.8624	295.5369	219.1464

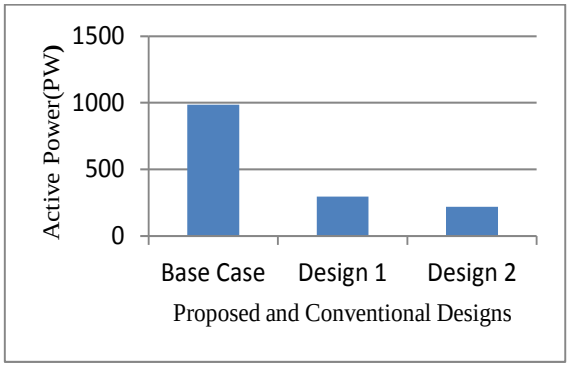

Figure 9.Active power dissipation comparison with proposed and conventional CMOS full adder cells

As shown in the Table and chart, both Design1 and Design2 active power is greatly reduced compared to the Base case. This reduction is almost 70.05% and 77.79% in case of Design1 and Design2 respectively compared to the Base case.

4. Conclusion

In this paper, low leakage 1 bit full adder cells are proposed for mobile applications. The proposed 1-bit full adder cells are designed with tsmc 0.18 µm technology. Both Design1 and Design2 active power is greatly reduced compared to the Base case. This reduction is almost 70.05% and 77.79% in case of Design1 and Design2 respectively compared to the Base case.

5. References

[1] M. V. D. L. Varaprasad, Rohit Bapna, Manisha Pattanaik, "Performance Analysis of Low leakage 1-bit Nano-CMOS Based Full Adder Cells for Mobile Applications, " *Proceedings of International Conference on VLSI Design & Communication Systems*, pp.233-238, January 2010.

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