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An Efficient Design of High Performance Different types of Oscillator for WI-FI and ISM bands of applications using 14nm FinFET Technology

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***Abstract*— In this paper, we propose an architecture of a CMOS based oscillators using actual capacitor and Inductor component. The proposed designs are based on 14 nm FinFET technology. We are designing these architectures for WI-FI and ISM band of frequency applications. The designed transistorized layout are easy to be integrated with low power consumption. The presented results are obtained using CMOS EDA tool Microwind 3.8 with FinFET 14nm technology with supply voltage of 0.80 V and IO VDD as 1.20 V. The obtained results are verified with the calculated by applying working formulas.**

Keywords – Physical design, CMOS Oscillator, ISM, WI-FI, Microwind 3.8

I. INTRODUCTION

Now a days, continuous advancement in CMOS technology is going on. With this advancement, more & more signal processing functions are implemented in the digital domain for low cost, low power consumption, higher performance and yield & higher re-configurability.

As the area of electronic devices is shrinking with time and VLSI technology shift towards nanometer features FinFET designs with trends of SOC in order to achieve low manufacturing cost. The oscillators are implemented with FinFET 14 nm MOS structures as, below CMOS 22nm technology transistor doesn't behave linearly with the change in parameters.

In this paper, we proposed different types of oscillators as Ring, Differential LC and Voltage Control Oscillator with foundry of 14 nm FinFET and comparison with the previous reference oscillator results. This proposed structure also have various advantages over the CMOS based foundries.

The modern CMOS design approach, we follows MOS modelling. In this paper we are using the BSIM-4 MOS modelling where we are having more than 300 MOS parameters for the voltage and current equations. Typically, FinFET models have over 1,000 parameters per transistor, and more than 20,000 lines of C code.

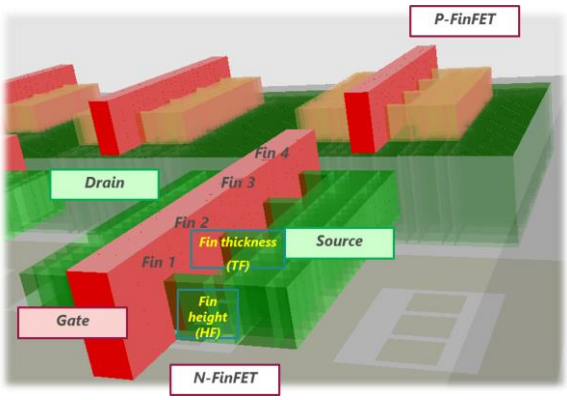

Fig. 1 : 3D structure of FinFET transistor

The total equivalent channel width is higher in FinFET than in MOSFET

For any design W and L are the important parameters that we need to consider. Below in the table are provided with some of the parameters;

TABLE 1: W and L for CMOS 45 nm Technology

MOS Parameter	Typical value
Width (W)	6 - 12 λ
Length (L)	2 λ

TABLE 2: Key parameters- FinFET 14nm Technology

FinFET Parameter	Typical value
Number of fins (NF)	2-5
Fin pitch (PF)	6 λ
Fin Thickness (TF)	1 λ
Fin length or gate length (LG)	2λ

The difference in physical design of the traditional MOS and FinFET is shown in the figure below.

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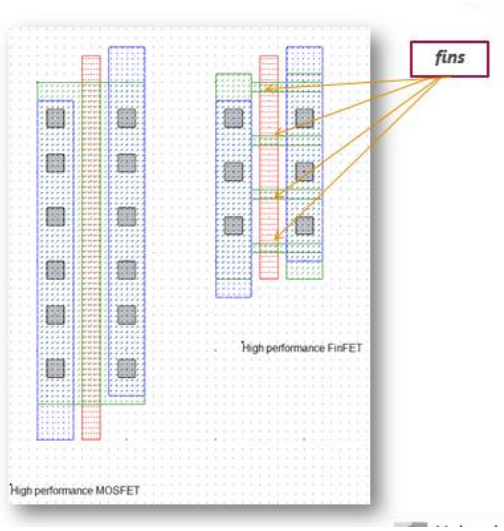

Fig. 2 : from MOSFET to FinFET

The FinFET device has a different layout style than the MOS device. Instead of a continuous channel, the FinFET uses fins. FinFET provides the same Ion current at a smaller size. FinFET provides lower leakage current Ioff at the same Ion.

The paper is organized as follows. In section II, overview of CMOS 45nm technology design, section III and IV describes proposed 14nm FinFET designs with result simulations. Finally section V concludes the paper.

II. OSCILLATOR DESIGN WITH CMOS 45 NM TECHNOLOGY

The CMOS based ring oscillator consists of odd number of inverter stages. The output frequency is equal to the inverse of the propagation delay of all the inverters.
A differential LC oscillator is a resonant circuit, tank circuit or tuned circuit consisting of L and C connected together. Here frequency is controlled using L and C components. Differential LC oscillator design provides linearity relationship between L and C values and frequency of oscillation.
VCO is oscillator whose oscillation frequency is controlled by a voltage input .The applied input voltage determines the instantaneous oscillation frequency. The VCO core is based on an inverter-type ring oscillator.

A. Ring Oscillator:

The ring oscillator made from five inverters has the property of oscillating naturally. The output oscillating frequency is equal to the inverse of the propagation delay of all inverters. It is a device composed of an odd number of inverters attached in a chain, with the output of the last inverter fed back into the first. The output oscillates between two voltage levels, representing true and false. The oscillations are due to the switching delay existing between the input and the output of each inverter.
The fastest oscillation is obtained with the minimum number of inverters which is 3, because it doesn't oscillate with only one.

B. Differential LC

CMOS based differential oscillator design is quite typical form of CMOS design as it involves capacitive and inductive effects. The schematic design is shown below.

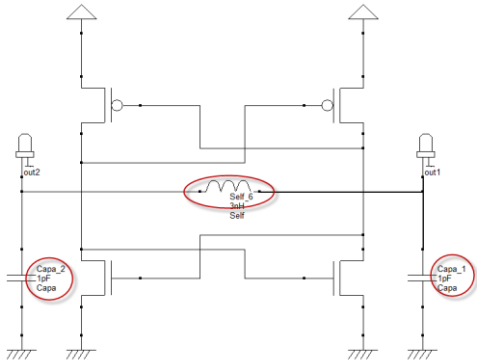

Fig. 3 : Schematic design of Diff. CMOS oscillator

For CMOS design implementation, we need to find out the current value of each transistor by calculating the W/L ratio.

TABLE 3 : W/L ratio with current

	Width(µm)	Length(µm)	No. of Fingers.	Current (I max)
P 1	1.660	0.040	2	1.746mA
P 2	1.660	0.040	2	1.746mA
N1	1.660	0.040	1	1.484mA
N2	1.660	0.040	1	1.484 mA

The values for MOS transistor are implemented. The physical layout is given below in the figure

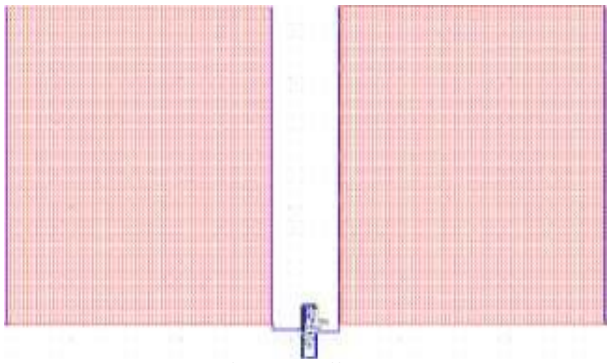

Fig. 4 : Physical desing of CMOS Diff LC oscillator with actual L and C components

The layout implementation is performed using a virtual inductor L1 and two capacitors C1 and C2 with the specified width and length in table above. Notice the large width of active devices to ensure a sufficient current to charge and discharge the huge capacitance of the output node at the desired frequency. Using virtual capacitors instead of on-chip physical coils is recommended during the development phase. It allows an easy tuning of the inductor and capacitor elements in order to achieve the correct behavior.
For the physical design, we used Capacitance = 1 pF each Inductance = 3 nH.

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C. Voltage Control Oscillator

A voltage-controlled oscillator or VCO is an electronic oscillator designed to be controlled in oscillation frequency by a voltage input. The voltage controlled oscillator (VCO) generates a clock with a controllable Frequency. The voltage controlled oscillator (VCO) generates a clock with a controllable frequency. The VCO is commonly used for clock generation in phase lock loop circuits. The clock may vary typically by +/-50% of its central frequency.

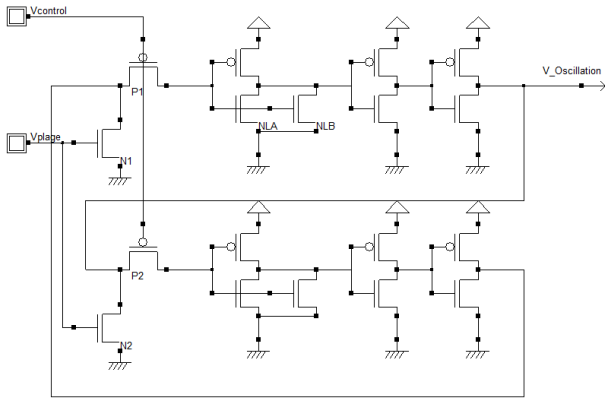

Fig. 5 : Schematic of VCO

The VCO is the most important functional unit in the PLL. It is commonly used for clock generation in phase lock loop circuits. Its output frequency determines the effectiveness of PLL. In addition to operating at highest frequency, this unit consumes the most of the power in the system. Obviously, this unit is of particular focus to reduce power consumption. PLL with multiple outputs means to design VCO with multiple outputs.

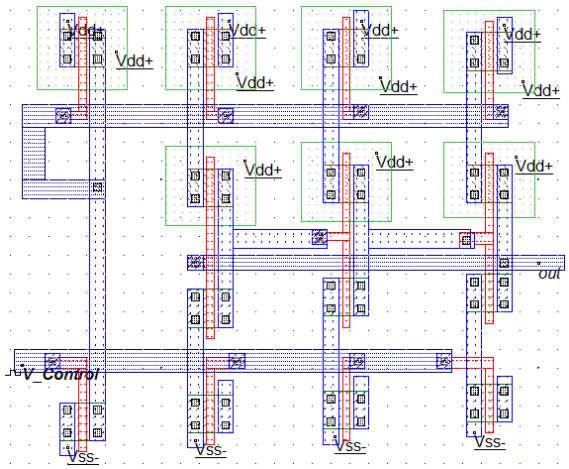

Fig. 6: Physical layout of VCO

The current-started inverter chain uses a voltage control 'Vcontrol' to modify the current that flows in the N1, P1 branch. The current through N1 is mirrored by N2, N3, N4, N5 & N6. The some current flows in P1. The current Through P1 is mirrored by P2, P3 and P4. Consequent by the change in 'Vcontrol' induces a global change in the inverter currents and acts directly on the delay.

III. PERFORMANCE ANALYSIS

For simulation here are the details;

For CMOS differential LC oscillator with keeping inductor value of 3nH and capacitor as 1pf each, the structure starts oscillating.

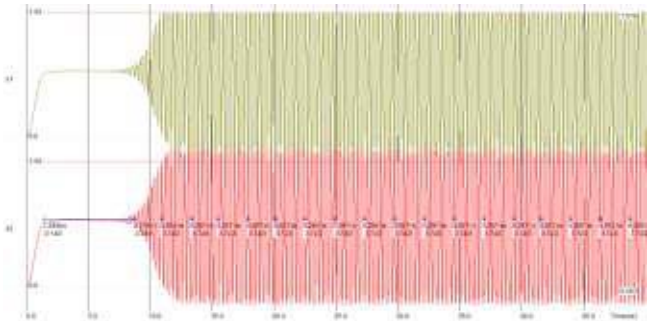

Fig. 7 : Transient analysis for Voltage.

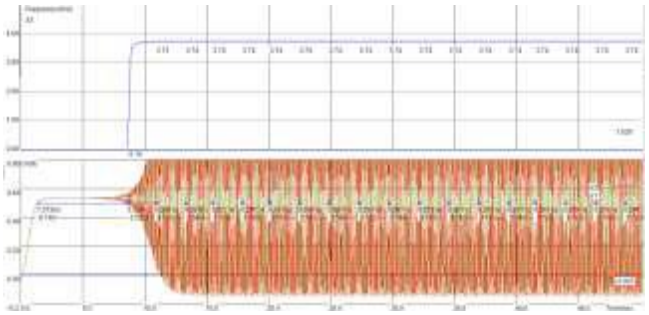

Fig. 8 : Frequency vs out curve

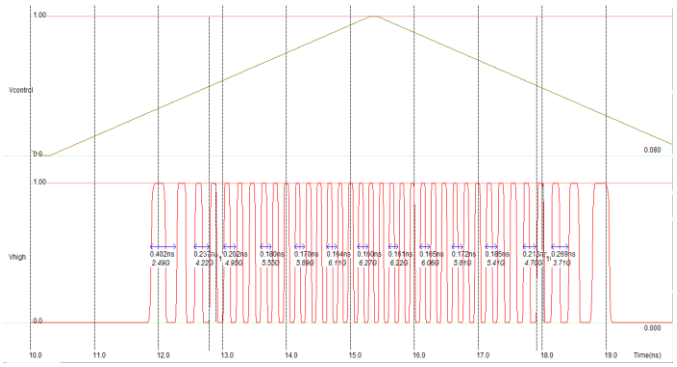

Fig. 9: DC Transient analysis for 'V_control' and 'Voltage_ctr_osc'

We chose to modify V_control very slowly, in order to see the influence on the oscillations. We put Control higher than 0.5 V, because there are no any oscillations under that value.

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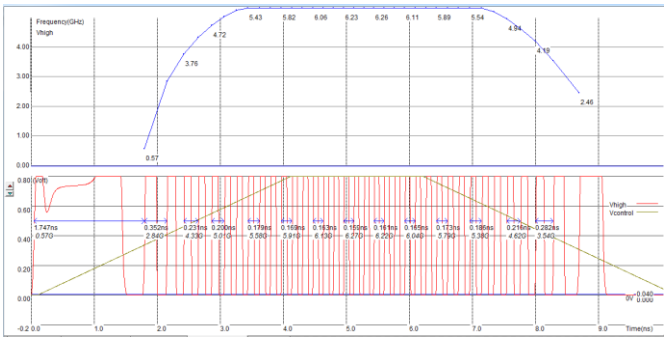

Fig. 10: Frequency and Voltage variation in VCO

Here we can notice on Figure, the oscillation frequency variation is not linear. The maximum frequency up to 6.12 GHz is obtained when V_control is maximal. The frequency swing of NCO is from 0.57 GHz to 6.26 GHz. It is possible to modify these values by implementing more inverters.

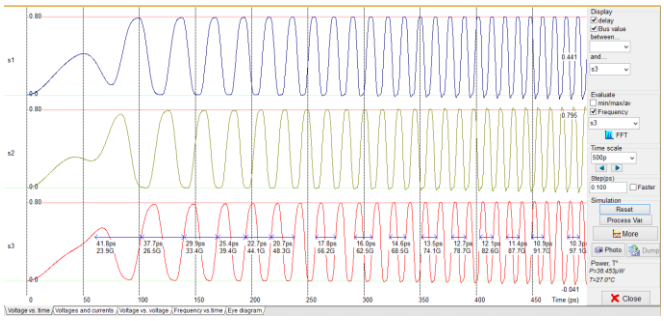

Fig. 11: Voltage vs current curve for FinFET base RO

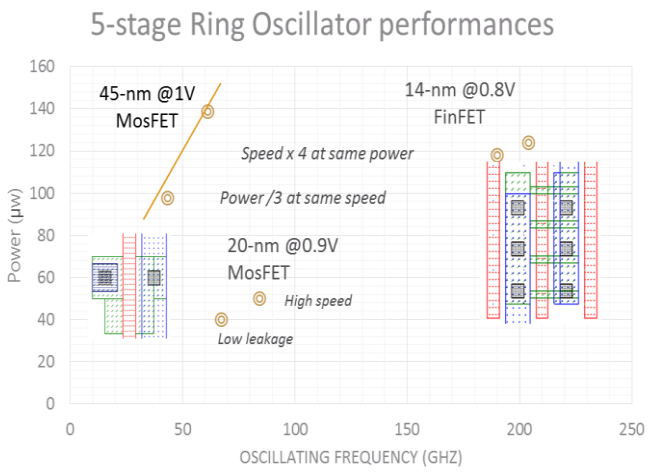

Fig. 12 : Performance of FinFET design

When we shifting form traditional CMOS technology to the FinFET technology, the performance of the design in terms of area, power consumption, delays etc. can be improved as shown in the figure above.

IV. CONCLUSION

For Ring Oscillator:

TABLE 4: Simulation result for CMOS based Ring Oscillator

Ring Oscillator		
No. of Stages	**Calculated**	**Simulated**
5	24.64 GHz	24.57 GHz
9	14.24 GHz	13.74 GHz
11	11.65 GHz	11.20 GHz
13	9.86 GHz	9.51 GHz

For Differential LC Oscillator:

TABLE 5: Simulation result for CMOS based Ring Oscillator

LC Oscillator		
No. of Stages	**Calculated**	**Simulated**
L= 3nH, C=1pF	4.11 GHz	4.08GHz
L= 3nH, C=1.2pF	4.02 GHz	4.05 GHz
L= 3nH, C=2.7pF	2.5 GHz	2.47 GHz

For VCO:

This paper presents the simulation and Implementation of different types of oscillators for specific applications of WI-FI and ISM bands. The Design and Realization of structures include the physical design and simulations. Design, Area and power parameters are optimized by working on physical layout design.

a) The measured tuning range of the proposed High performance VCO design is 0.60 to 3.23 GHz.

b) The measured tuning range of the proposed High performance VCO design is 1.42 to 1.53 GHz for full swing V_Controll as clock input and Vplage as constant DC supply of 0.667 Vfrom 0v to 1V.

c) The on screen power estimation of the design is 60.126uW, which is quite less as compared to the normal VCO design.

We can again fine-tuned the oscillator design by designing and optimizing the functional physical parameters. The frequency of oscillation can be achieved for ISM and WI-FI bands of frequency applications.

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