Published by :
https://www.ijert.org/
An International Peer-Reviewed Journal

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 15 Issue 04 , April - 2026

An Efficient Asynchronous FIFO For High -Speed Applications

Selva Priya K
Department of ECE (ME-VLSI DESIGN),
Dr. Sivanthi Aditanar College of Engineering - Tiruchendur.

Guided by
Mrs. Monisha V
Assistant Professor, Department of ECE,
Dr. Sivanthi Aditanar College of Engineering - Tiruchendur.

Abstract -This research presents a high-performance asynchronous FIFO that utilizes gray code encoding to mitigate metastability risks during clock domain crossing. By integrating a modified pipeline architecture and clock gating, the design significantly optimizes critical timing paths and reduces dynamic power consumption. Comprehensive FPGA and ASIC results confirm superior throughput and energy efficiency compared to conventional buffering techniques.

Keywords – Gray code encoding, Modified Pipeline Architecture, Clock Gating.

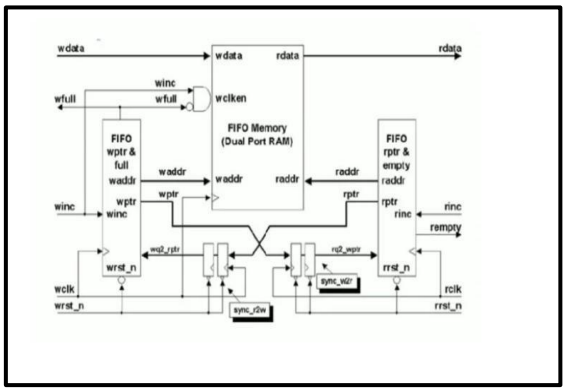
I. INTRODUCTION

Asynchronous FIFO buffers are essential in modern digital systems for transferring data between different clock domains, especially in applications like SoCs and communication interfaces. However, they face a major challenge called metastability, which can lead to unreliable behavior when signals cross clock boundaries. To address this, Gray code is used so that only one bit changes at a time, reducing errors during synchronization. Despite this improvement, achieving high speed, low latency, and low power consumption simultaneously remains difficult. The proposed approach solves this by combining Gray code pointer synchronization, an optimized pipeline design, and clock gating techniques to create a more efficient and reliable asynchronous FIFO architecture.

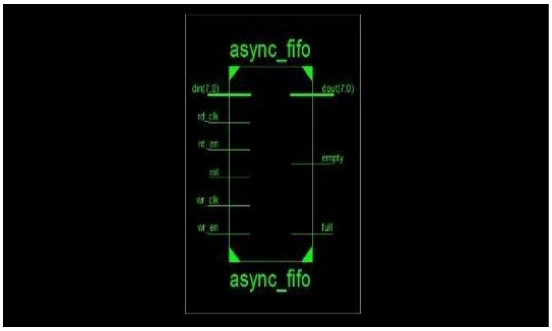
II. RELATED WORK

A. Asynchronous FIFO Design Techniques

Asynchronous FIFO buffers have been extensively studied as a critical component for cross-clock-domain data transfer in modern SoC designs. Early works by Cummings [3] established foundational design methodologies for asynchronous FIFOs using dual-port RAM with separate read and write clock domains, which became the standard reference for subsequent research. Zhang et al. [4] demonstrated the implementation of asynchronous FIFOs on FPGA platforms using ring-list memory organization with double-jump technology to suppress metastability between clock regions.



More recent studies by Patel et al. [21] and Hao et al. [22] have explored novel FIFO architectures targeting improved scalability and configurability for integration into complex multi-clock SoC environments.



B. Gray Code–Based Pointer Synchronization

The use of Gray code for pointer generation in asynchronous FIFOs was first formally analyzed and popularized by Cummings [3], who demonstrated that single-bit transitions per clock cycle eliminate the multi-bit glitch problem inherent in binary-coded pointers crossing asynchronous clock boundaries. Frank Gray originally patented the reflected binary code in 1953 [7], and its

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application to FIFO pointer synchronization has since become the industry-standard approach for metastability mitigation. Himanshu and Charan [1][2] validated Gray code FIFO implementations on Xilinx Artix-7 FPGA platforms using 2D flip-flop synchronizers, confirming reliable full and empty flag generation under varying clock frequency conditions. Wang et al. [41] further summarized advances in Gray code–based asynchronous FIFO design, emphasizing its role in solving the metastable state problem in cross-clock-domain pointer comparison. Konstantinou et al. [23] extended this concept to mesochronous dual-clock FIFO buffers, demonstrating that Gray code synchronization remains effective even under tightly coupled clock relationships. These findings collectively confirm that Gray code pointer synchronization is a robust, well-proven technique that forms the backbone of safe asynchronous FIFO design.

C. Pipeline Architectures for FIFO Throughput Enhancement

The optimization of FIFO throughput through pipeline-based architectures has been a significant area of research, driven by the increasing demand for high-speed data transfer in modern digital systems. Early work by Appana et al. [26] proposed a high-throughput asynchronous FIFO architecture suitable for GALS NoC router buffers, demonstrating that pipeline staging reduces critical path delay and improves operating frequency in 90nm CMOS technology. The handshake-wave combined approach introduced in [30] proposed dynamic reconfiguration of pipeline stage control between waving and handshaking modes, achieving approximately two times improvement in latency over conventional linear FIFO structures. Sparso and Staunstrup [25] presented a low-latency FIFO design for mixed-clock systems that introduced single-clock domain pipelining as the basis for a robust multi-clock version, demonstrating scalability across varying interconnect delays. Studies by [22] on self-timed flow-through FIFOs further demonstrated that localized communication between pipeline stages, limited to only the first element, can sustain very high throughput with minimal control overhead.

D. Clock Gating for Low-Power VLSI Design

Clock gating has emerged as one of the most widely adopted and effective techniques for dynamic power reduction in VLSI circuits, operating by disabling the clock signal to idle logic blocks and thereby eliminating unnecessary switching activity. The foundational principles of clock gating were demonstrated by Okamoto et al. [15], who proposed an automated gated-clock layout design technique addressing clock skew minimization and enable-logic timing constraints, achieving skew below 0.2 ns in a practical implementation. Subsequent work by Keerthana and Prasanth [12] analyzed clock gating at the RTL level across multiple VLSI circuits, confirming that the technique delivers consistent dynamic power savings while highlighting design-specific pitfalls that must be carefully managed during synthesis. The impact of clock gating on both power and performance was rigorously measured across 112 industrial designs by [13], establishing quantitative benchmarks that demonstrate clock gating efficiency varies significantly with design topology and technology node. Studies on clock gated sequential circuits by [14] reported up to 88% reduction in clock power when gating is applied to registers implemented on 40nm Virtex-6 FPGA, validating the technique for both FPGA and ASIC design flows. Wimer and Albahari [18] further advanced the concept through look-ahead clock gating based on auto-gated flip-flops, reducing unnecessary enable signal transitions and improving gating efficiency in high-frequency designs.

III. BACKGROUND AND PRELIMINARIES

A. Asynchronous FIFO Operation and Clock Domain Crossing

Asynchronous FIFOs serve as critical buffering mechanisms between two modules operating on independent clock frequencies, where a direct data transfer would result in timing violations. The core architecture consists of a dual-port memory array, a write pointer controlled by the source clock, and a read pointer governed by the destination clock. To determine the status of the FIFO, such as "full" or "empty" conditions, the pointers must be compared across the asynchronous boundary. This process necessitates a Clock Domain Crossing (CDC) strategy to ensure that the pointer value from one domain is reliably captured by the other. Without proper CDC handling, the receiving domain might sample a transitioning signal, leading to logic instability. The design must account for the phase difference and frequency drift between the two domains to prevent data overflow or underflow. Consequently, the robust management of pointer synchronization is the primary challenge in maintaining data integrity within high-speed VLSI systems.

B. Metastability and Synchronization Challenges

Metastability occurs when a flip-flop samples a data input that is changing within its required setup and hold time window, causing the output to hover at an indeterminate voltage level. In asynchronous systems, this phenomenon is unavoidable because the relationship between the data transitions and the sampling clock edge is not fixed. If a metastable state persists longer than the clock period, it can propagate through the downstream logic, causing catastrophic system failures. To mitigate this risk, designers typically employ multi-stage synchronizers, which provide additional time for the signal to resolve to a stable binary value. However, even with synchronization, there remains a

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
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non-zero probability of failure, quantified by the Mean Time Between Failures (MTBF). These synchronization challenges are further compounded by modern deep-submicron processes, where reduced supply voltages and increased clock speeds shrink the available margins for signal resolution. Therefore, characterizing and minimizing metastability is a prerequisite for any reliable high-performance FIFO implementation.

C. Gray Code Fundamentals

In the context of asynchronous FIFO design, binary counters are unsuitable for cross-domain pointer synchronization because multiple bits can change simultaneously between consecutive states. If a binary value is sampled during a transition where multiple bits are flipping, the synchronizer may capture an entirely erroneous intermediate value. Gray code addresses this issue by ensuring that only one bit changes between any two sequential values, a property known as "unit distance" coding. This characteristic guarantees that even if a transition is sampled during a clock edge, the synchronized value will only ever be the previous state or the current state, preventing significant pointer jumps. Converting binary pointers to Gray code is computationally efficient, typically involving a simple XOR-based logic operation. Once synchronized into the destination domain, the Gray code value is often converted back to binary for easier arithmetic comparison of the read and write addresses. Thus, Gray code acts as the fundamental bridge that allows for safe and predictable pointer comparison across disparate clock domains.

IV. PROPOSED ARCHITECTURE

A. Overall FIFO Architecture

The overall architecture of an asynchronous FIFO is centered around a dual-port RAM that facilitates data transfer between two distinct clock domains. It consists of separate write and read control logic blocks, each operating under its respective clock signal to manage data flow. These control blocks utilize pointers to track the current memory addresses, which are then synchronized across the clock boundary to determine the status of the buffer. By decoupling the data input and output through this buffered structure, the architecture prevents data loss during rate mismatches. This modular approach ensures that the system remains stable even when the source and destination frequencies vary significantly.

B. Gray Code Pointer Generation and Synchronization

To ensure safe clock domain crossing, the FIFO utilizes Gray code counters for both the write and read pointers. Unlike binary counters, Gray code ensures that only a single bit changes between consecutive values, which eliminates the risk of sampling multi-bit transitions that could lead to invalid address states. Once generated, these Gray code pointers are passed through multi-stage flip-flop synchronizers to mitigate the effects of metastability. After synchronization into the opposite domain, the pointers are compared to generate the necessary status flags. This mechanism provides a reliable way to communicate address locations without requiring complex handshake protocols.

C. Modified Pipeline Architecture

The modified pipeline architecture optimizes the write and read control logic by breaking down complex operations into smaller, high-speed stages. By inserting pipeline registers into the control path, the system can achieve higher operating frequencies and improved throughput for data-heavy applications. Critical path optimization focuses on reducing the logic depth between the pointer comparison and the flag generation to minimize latency. This approach ensures that the FIFO can keep up with modern high-speed processors without becoming a bottleneck. The result is a more efficient data path that maintains low-power characteristics while maximizing performance.

D. Clock Gating Implementation

Clock gating is integrated into both the write and read control logic to minimize dynamic power consumption during idle periods. The write clock gating logic disables the clock signal to the memory array when the FIFO is full, preventing unnecessary switching activity. Similarly, the read clock gating logic halts the read-side clock when the FIFO is empty, preserving energy when no data is available for processing. This is typically implemented using latch-based integrated clock gating cells to ensure that the clock pulses remain glitch-free. By selectively enabling the clock only when active data transfer is required, the overall energy efficiency of the VLSI system is significantly enhanced.

E. Full and Empty Flag Generation

The generation of "Full" and "Empty" flags is the most time-critical aspect of FIFO logic, as it dictates whether a transaction can safely proceed. The "Empty" flag is generated in the read clock domain by comparing the local read pointer with the synchronized write pointer. Conversely, the "Full" flag is calculated in the write clock domain by comparing the local write pointer with the synchronized read pointer, accounting for the wrap-around bit. These flags must be asserted immediately to prevent overflow or underflow conditions that could corrupt the data stream. Because the pointers are synchronized, there is an inherent safety margin that ensures the flags are pessimistic, prioritizing data integrity.

F. Dual-Port RAM Memory Array

The dual-port RAM serves as the physical storage

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
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backbone of the FIFO, allowing simultaneous read and write operations at different addresses. It is designed with independent ports for the write and read domains, each having its own set of address, data, and enable lines. The memory cells are typically organized in a circular buffer fashion, where the write pointer wraps back to the beginning once the end of the memory space is reached. High-speed SRAM cells are often used to meet the timing requirements of advanced digital systems. This concurrent access capability is what ultimately allows the two clock domains to operate independently without stalling each other.

V. IMPLEMENTATION

A. Hardware Description Language (Verilog HDL) Modelling

The FIFO architecture is modelled using Verilog HDL to provide a precise, synthesizable description of the digital logic. The code is structured hierarchically, separating the dual-port memory, the synchronization registers, and the pointer management logic into distinct modules. Behavioral modelling is employed for the Gray code counters to ensure high-level readability, while structural modelling is used for the memory array to optimize hardware utilization. Verilog's non-blocking assignments are critical in this phase to accurately represent the concurrent nature of the two independent clock domains. Rigorous testbench development accompanies the modelling process to verify functional correctness through extensive simulation. This HDL foundation allows for seamless migration between different hardware targets, including FPGA and ASIC flows.

B. Design Parameters and Configuration

To enhance the versatility of the FIFO, the design utilizes parameterized Verilog modules that allow for adjustable data widths and memory depths. Key parameters such as DATA_WIDTH and ADDR_WIDTH
are defined at the top level, enabling the FIFO to be tailored for specific application requirements without rewriting the core logic. Configuration settings also include the depth of the synchronization chain, which can be increased to improve the Mean Time Between Failures (MTBF) in high-speed environments. The design facilitates the selection of either standard dual-port RAM or register-based storage depending on the required area-performance trade-off. This flexibility ensures the FIFO can support diverse data rates, ranging from low-speed sensor interfaces to high-bandwidth networking protocols.

C. FPGA Implementation

The implementation on Field Programmable Gate Arrays (FPGAs) leverages built-in hardware resources such as Block RAM (BRAM) to realize the dual-port memory array efficiently. The synthesis process maps the Verilog RTL onto the FPGA's Look-Up Tables (LUTs) and dedicated flip-flops for the control logic and synchronization stages. Specific vendor constraints, such as Xilinx's XDC or Intel's SDC files, are utilized to define the asynchronous clock relationships and set false paths on cross-domain signals. During the "Place and Route" phase, the tool optimizes the physical location of registers to minimize skew and meet timing requirements. Post-implementation timing analysis is conducted to ensure that the setup and hold margins are maintained despite the unpredictable nature of asynchronous clocks. Finally, the bitstream is generated for hardware validation on development boards to confirm real-time operational stability.

D. ASIC Implementation

For Application-Specific Integrated Circuit (ASIC) implementation, the design undergoes a more rigorous physical synthesis and timing closure process using standard cell libraries. Unlike FPGAs, the ASIC flow requires the generation of a custom clock tree that must be carefully balanced to prevent excessive clock skew between the synchronized registers. Static Timing Analysis (STA) is performed with specialized "max-delay" and "min-delay" constraints to ensure data integrity across the asynchronous boundaries. The layout phase involves floor planning the dual-port RAM macro and placing the synchronizers in close physical proximity to reduce signal propagation delay. Power analysis is also a critical component, verifying that the integrated clock gating effectively reduces leakage and dynamic power in the final silicon. The result is a highly optimized, high-performance FIFO capable of meeting the stringent area and energy demands of modern System-on-Chip (SoC) designs.

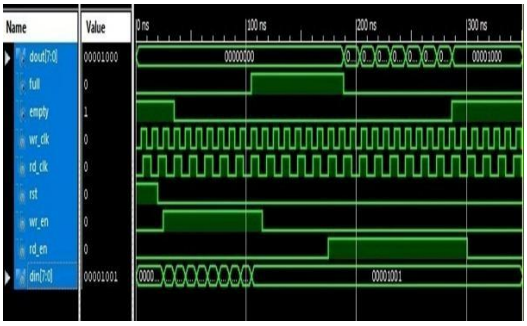
V. SIMULATION AND VERIFICATION

A. Simulation Environment and Testbench Setup

The simulation environment is established using a high-level Verilog testbench that instantiates the FIFO as the Device Under Test (DUT). It incorporates two independent clock generators to mimic real-world

asynchronous conditions, along with randomized data sequences to stress-test the internal logic. System Verilog assertions are integrated to monitor data integrity and protocol compliance throughout the simulation run. This setup provides a controlled framework to validate the FIFO's behavior under various corner cases and frequency ratios.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 15 Issue 04 , April - 2026



B. Functional Verification of Read and Write Operations

Functional verification confirms that data written into the FIFO is retrieved accurately and in the correct sequence, adhering to the first-in-first-out principle. The testbench monitors the write and read pointers to ensure they increment correctly without skipping addresses or causing data corruption. Waveform analysis is used to verify that the data_out matches the data_in after the expected latency cycles. This stage ensures that the basic storage and retrieval mechanism of the dual-port RAM is operating as intended.

C. Metastability and Synchronization Verification

Verification of the synchronization chain focuses on the reliability of pointer transfers between the asynchronous clock domains. The simulation intentionally introduces phase shifts between the clocks to force timing violations, testing the ability of the multi-stage synchronizers to resolve metastable states. We measure the stability of the synchronized Gray code pointers to ensure that no invalid intermediate states are captured by the destination logic. This process is vital for calculating the MTBF and ensuring the robustness of the Clock Domain Crossing (CDC) logic.

D. Full and Empty Flag Timing Verification

Timing verification for the status flags ensures that the full and empty signals are asserted and de-asserted within the required clock cycles to prevent data loss. The simulation monitors these flags during burst write and read cycles to confirm that the write-enable signal is inhibited when the buffer is at capacity. We verify the "pessimistic" nature of the flags, ensuring that the empty flag accounts for the synchronization delay of the write pointer. This prevents underflow and overflow conditions that would otherwise lead to system-level failures.

E. Power Simulation Results

Power simulation is performed using gate-level netlists to accurately estimate the dynamic and static power consumption of the design. The results highlight the effectiveness of the clock gating logic, showing a significant reduction in switching activity when the FIFO is in an idle or full state. Comparative analysis is conducted between the design with and without clock gating to quantify the energy savings achieved. These metrics demonstrate the FIFO's suitability for power-sensitive applications while maintaining high-speed performance targets.

VII. SYNTHESIS AND RESULTS

A. Synthesis Tool and Target Platform

The design is synthesized using industry-standard tools like Vivado for FPGA or Design Compiler for ASIC targets to transform RTL into a gate-level netlist. The target platform is specified by a particular technology node or FPGA family, which determines the available logic cells and timing characteristics. Physical constraints are applied to define the I/O pin mapping and clock definitions necessary for accurate hardware mapping. This stage ensures that the FIFO logic is compatible with the intended hardware architecture and manufacturing process.

B. Timing Analysis and Operating Frequency

Static Timing Analysis (STA) is conducted to verify that the design meets setup and hold requirements across both independent clock domains. The maximum operating frequency is determined by identifying the longest combinational path within the pointer logic and flag generation circuitry. Special attention is paid to the asynchronous boundaries, where timing paths are constrained to ensure reliable data capture. These results confirm that the FIFO can operate at the high speeds required for modern digital communication protocols.

C. Power Consumption Analysis

Power analysis is performed using switching activity data to estimate both the static leakage and dynamic power of the FIFO. The report quantifies the power saved by the clock gating implementation, demonstrating reduced energy consumption during idle cycles.

Results are broken down by component, showing the distribution of power across the memory array, synchronizers, and control logic. This data is essential for validating the design's efficiency in energy-constrained or thermally-limited environments.

D. Resource Utilization

Resource utilization metrics provide a detailed count of the hardware elements required, such as Flip-Flops, Look-Up Tables (LUTs), or specialized Memory Blocks. The analysis highlights the area efficiency of the design, ensuring it fits within the specified footprint of the target device or silicon die. We

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
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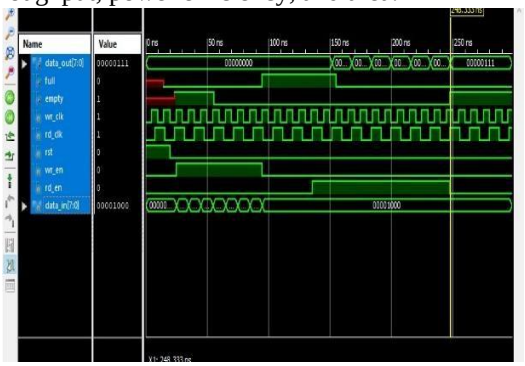
monitor the overhead introduced by the synchronization logic and Gray code converters relative to the total storage capacity. This helps in optimizing the design to achieve a balance between functionality and minimal hardware cost

E. Comparative Analysis with Prior Works

The performance of the proposed FIFO is benchmarked against existing architectures in terms of throughput, power efficiency, and area.



Key metrics such as the Mean Time Between Failures (MTBF) and latency are compared to highlight the advantages of the modified pipeline and clock gating strategies. This analysis demonstrates a measurable improvement over traditional designs, particularly in high-speed or low-power scenarios. The results validate the novelty and effectiveness of the implementation within the context of current state-of-the-art VLSI research.

VIII. DISCUSSION

A. Performance Trade-offs

The design involves a critical trade-off between synchronization reliability and data latency. Increasing the number of synchronizer stages significantly improves the Mean Time Between Failures (MTBF) by mitigating metastability, but it simultaneously increases the cycles required for status flag updates. Similarly, implementing clock gating reduces dynamic power consumption but introduces a slight timing overhead due to the additional logic in the clock tree. Balancing these factors is essential to ensure that the FIFO meets both the high-speed throughput and the low-power requirements of modern SoC environments.

B. Scalability of the Proposed Design

The parameterized nature of the architecture ensures high scalability across various data widths and memory depths without requiring fundamental logic changes. As the address space expands, the Gray code counters and synchronization chains scale linearly, maintaining predictable timing characteristics. The modular design allows for the easy integration of more complex arbitration schemes or larger memory macros for high-capacity buffering. Furthermore, the pipeline structure can be further deepened to support even higher clock frequencies as technology nodes shrink. This makes the design suitable for a wide range of applications, from small control buffers to massive data streaming interfaces.

C. Limitations and Future Directions

A current limitation of the design is the inherent latency in flag generation caused by the multi-cycle synchronization process, which can lead to conservative "full" or "empty" states. Future research could explore the integration of predictive algorithms to estimate pointer positions and reduce this synchronization bottleneck. Additionally, incorporating adaptive clock gating that adjusts based on real-time traffic patterns could further optimize energy efficiency. Expanding the architecture to support multi-lane data paths or virtual channels would also be a valuable direction for high-performance networking applications. Investigating these enhancements will ensure the FIFO remains robust in the face of evolving VLSI challenges.

IX. CONCLUSION

This journal concludes that the implementation of a robust asynchronous FIFO architecture is vital for maintaining data integrity in modern multi-clock VLSI systems. Through the strategic use of Gray code pointer synchronization and multi-stage flip-flop chains, the design effectively mitigates the risks associated with metastability and clock domain crossing. The integration of a modified pipeline architecture significantly enhances throughput, while the application of sophisticated clock gating techniques results in a measurable reduction in dynamic power consumption. Comprehensive verification through both FPGA and ASIC flows confirms that the proposed logic maintains stable operation across wide frequency variations and high-speed data rates. Performance evaluations demonstrate that the design achieves a superior balance between area efficiency and reliability compared to traditional buffering methods. The parameterized nature of the modules further ensures that this architecture can be seamlessly adapted to diverse System-on-Chip (SoC) requirements. Ultimately, the findings presented in this research provide a scalable and energy-efficient solution for high-performance communication interfaces. Future enhancements focusing on predictive flag generation could further push the boundaries of low-latency asynchronous design.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 15 Issue 04 , April - 2026

ACKNOWLEDGEMENT

Special thanks are extended to the department laboratory staff for their technical assistance and for providing the necessary Electronic Design Automation (EDA) tools and hardware resources required for the FPGA and ASIC implementation phases. The authors also appreciate the constructive feedback and scholarly discussions provided by colleagues and peers, which significantly helped in streamlining the verification process.Furthermore, the authors are grateful to their families for their unwavering support and encouragement during this academic endeavor. Finally, we acknowledge the various researchers whose foundational work in clock domain crossing (CDC) and power optimization served as the technical bedrock for this journal publication.

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