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An Efficient And Power Optimized Cascode Stage RF Tuned Class-E Power Amplifier

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Abstract— An efficient and power optimized cascode modulated CMOS class-E RF tuned power amplifier (PA) is presented in this paper. The main advantage of the proposed technique over other conventional modulation techniques is that it will provide a higher output power dynamic range and power added efficiency (PAE). Morever, an external supply modulator is not required if this technique is employed. A cascode modulated signal is applied to the gate of the power amplifier which in turn modulates the output power. The RF tuning of the proposed Class-E amplifier results in a PAE of approximately 64% which is an improvement over other conventional techniques. The cascode modulated CMOS class-E RF tuned power amplifier operates at a frequency of 2.4 GHz with 20.1 dBm output power and is implemented using 180 nm technology.

***Keywords*— Cascode, Modulation, RF tuning, Output power, Dynamic range, Power added efficiency.**

I. INTRODUCTION

Linear RF power amplifiers consume large amounts of energy, dissipate heat and take up space in base stations. Significantly more efficient PA technology will be instrumental to the evolution of mobile systems. The main requirements for future power amplifier technology are high linearity to satisfy higher-order modulation schemes, greater average output power levels and broader operating bandwidths (more than twice today's typical 20MHz).

The interest in highly efficient power amplifiers particularly Class-E power amplifiers for microwave applications has significantly increased now-a-days. Linear RF power amplifiers consume large amounts of energy, dissipate heat and take up space in base stations. Class-E power amplifiers achieve significantly higher efficiency than conventional Class-B or Class–C amplifier. In Class-E, the transistor operates as an on/off switch and the load network shapes the voltage and current waveforms to prevent simultaneous high voltage and high current in the transistor; that minimizes power dissipation, especially during the switching transitions.

Class-E power amplifier achieves 100% theoretical efficiency and potentially robust performance. Many aspects of the Class-E power amplifier has been extensively studied. One of the most important aspects of the Class-E amplifier operation is the use of a finite dc-feed inductance.

The benefit of using a finite dc-feed inductance is as follows:

- a reduction in overall size and cost
- a higher load resistance, which typically results in a more efficient output matching network
- a possible reduction in the required supply voltage, which might enable the implementation of the Class-E PA in low-voltage technologies.

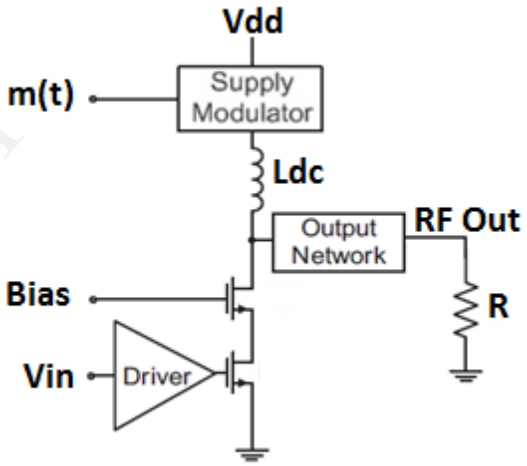

Figure 1. Conventional Supply Modulation technique

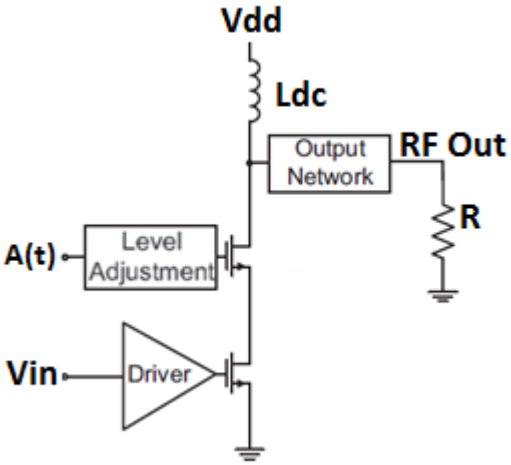

Figure 2. Proposed cascode modulation technique

Switching PAs, the class-E topology in particular are widely used at RF frequencies since they provide high efficiency and circuit simplicity [1]-[4].

The paper is organized as follows. Section 2 throws light on the available literature on Class-E power amplifiers. Section 3 highlights the different implementation methods that can be considered for the power amplifier design. Section 4 specifies the design approach and in section 5 the Class-E amplifier design has been discussed. Section 6 shows the comparision between the literature available and the current work. The conclusion has been given in section 7.

II. LITERATURE REVIEW ON CLASS-E POWER AMPLIFIER

Several researches have been conducted on the Class-E power amplifier till date, but there is very less reported work on RF tuned Class-E amplifier. Some of the literature surveys done are summarized as follows:

A. Cascode Class-E Amplifier

Daniel Sira et al. [4] in the year 2010, proposed a power control method for cascode modulated CMOS class-E power amplifier architecture which resulted in a high 36 dB output power control range (PCR). In the year 2011, he modified the prototype [2] by using an EDGE modulated signal for testing and obtained an output power dynamic range of 35dB. The peak power added efficiency (PAE) was found to be 35%. The concept of the cascode power control of class-E RF PA operating at 2.2GHz with 18dBm output power was implemented in a 0.18 µm CMOS technology.

B. Class-E Power Amplifier with negative capacitance

Yonghoon Song et al. in the year 2010 [5] proposed a class-E power amplifier (PA) with double-resonance circuit to reduce voltage stress on CMOS transistors where the voltage waveform applied to the CMOS transistor was shaped by harmonic control. A negative capacitance was also implemented for efficiency enhancement, compensating for surplus capacitance from parasitic components on the drain node thereby achieving high efficiency. Advantage of the proposed cascode differential class-E RF PA is that the design is fabricated using a 0.13 µm CMOS technology and it delivers 31.5 dBm output power with 54% drain efficiency and 51% power-added efficiency at 1.8 GHz.

C. Class-E RF tuned Power Amplifier

S.H.L. Tu et al. in the year 2012, developed a simple and novel low distortion output-power-control prototype architecture based on high-Q compensated varactors [1]. Advantage of the proposed architecture is that the capacitors used in the proposed architecture are responsible for tuning of RF PAs and power-control in switching-mode amplifiers. The architecture was implemented using 180 nm CMOS technology.

III. VARIOUS PROPOSED METHODS FOR CLASS-E POWER AMPLIFIER IMPLEMENTATION

A number of authors have recommended the use of cascode modulation technique rather than going for conventional supply modulation technique for designing an efficient Class-E power amplifier.

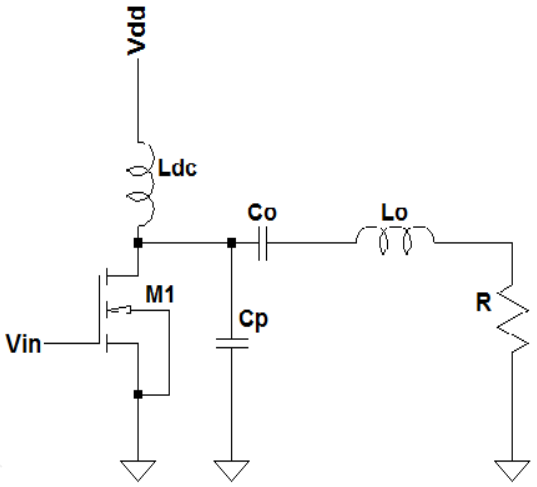

Figure 3. Diagram of basic Class-E Power Amplifier

The basic Class-E power amplifier [3] is shown in figure 3.

For the design of the Class-E power amplifier we have basically two power control techniques.

A. Power Supply Modulation Technique

The power supply modulation technique is as shown in Fig. 1. The supply modulator modulates the PA supply voltage according to the amplitude signal A(t). The power supply modulation of a switch-mode PA shows that the output power is directly related to the supply voltage. The average output power of the class-E PA is proportional to the square of the supply voltage according to

$$P_{out} = \frac{8}{\pi^2+4}\frac{{V_{dd}}^2}{R_L} \approx 0.5768\frac{{V_{dd}}^2}{R_L}$$

The DR is the maximum range over which the PA average output power can be controlled. It can be written as

$$DR(dB) = P_{out,max} - P_{out,min} = 20\log\frac{V_{DD,max}}{V_{DD,min}}$$

where $P_{out,max}$ and $P_{out,min}$ are the maximum and minimum output power in dBm.It is assumed that the load impedance is constant. The supply voltage varies between 0.1–1.8V which results in 25.1 dBm output power dynamic range. The main

drawbacks of the supply modulation technique are limited output power dynamic range and high sensitivity to load variations. Since the supply modulator pulls a high current to the PA, the placement of the modulator in the high power path (in series with the RF choke) makes efficiency the most important parameter.

B. Cascode Modulation Technique

To control the output power of the power amplifier we use Cascode Power Control Technique(CPCT) as shown in Fig. 2 where we change the gate voltage of cascode transistor instead of power supply by applying a bias voltage. Input dynamic range of Cascode Power Control Technique is about one threshold voltage lower than the conventional Supply Voltage Power Control Technique(SVCPT) [3] for the same Power Control Range. The advantage of Cascode Power Control Technique is wider Power Control Range as compared to Supply Voltage Power Control Technique.

C. *RF Tuning*

To achieve a relatively higher efficiency and power control we go for RF tuning [1] of the prototype. In the proposed design RF tuning of the basic Class-E amplifier has been done by using an additional inductor. The tuning could also have been done using an additional capacitor but since it will take a relatively high value of capacitance it may not be practically realizable. The RF tuned power amplifier results in a better PAE and PCR. It also causes a significant improvement in the output power also. This is shown in the comparision table.

IV. DESIGN APPROACH

The basic Class-E amplifier which involves the use of a finite dc-feed inductor is designed at first by using some standard design formulas. Efficiency is maximized by minimizing power dissipation, while providing a desired output power. Cascode modulation technique is used in order to achieve high output power dynamic range, higher voltage swing, stress relief and improved power added efficiency (PAE). After the cascode modulated Class-E Power Amplifier is designed, suitable RF tuning is done with the help of varactors/high-Q compensated inductors.

V. CLASS-E POWER AMPLIFIER DESIGN

A. Class-E power Amplifier Design:

The figure shown below shows the Class-E Amplifier design .

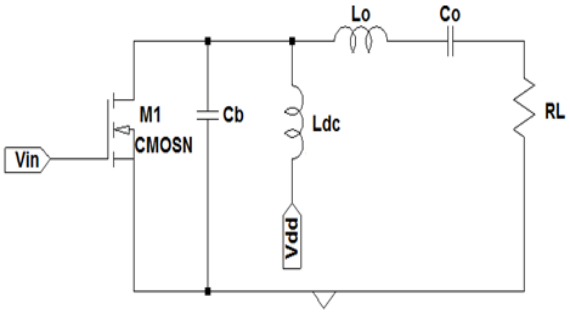

Figure 4. Diagram of basic Class-E Power Amplifier

As shown in figure 4, the basic class-E amplifier utilizes a single transistor which acts as a switch (M1). The output network consists of series resonant circuit (C0 and L0) and shunt capacitor (Cb). The main advantage of the class-E is that the parasitic output capacitance of the active device becomes an element in the output network design. The class-E amplifier requires a small number of passive components (as compared to the class-F amplifier) what makes it a promising candidate for the CMOS integration. The role of the output network in class-E amplifier is to shape the drain voltage and device current in such a way that there is no instantaneous overlap between them.

There are three conditions which have to be fulfilled in order to achieve a high efficiency. The first is called the zero voltage switching (ZVS) condition and the second is zero voltage derivative switching (ZVDS) condition. The ZVS condition dictates that the voltage across the switch has to be zero at the instance the switch goes ON. The ZVDS condition says that the derivative of the voltage across the switch has to be zero. These two conditions guarantee that the power loss during the switch turn-on is minimized. The third condition is that the rise of the voltage across the switch has to be delayed until the switch is turned OFF to reduce the turn-off transition loss. If the amplifier meets the three conditions it is called an optimum class-E amplifier.

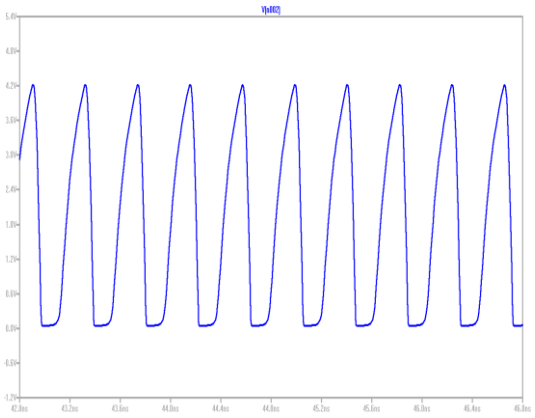

Figure 5. Plot of drain voltage(v) vs time(ns)

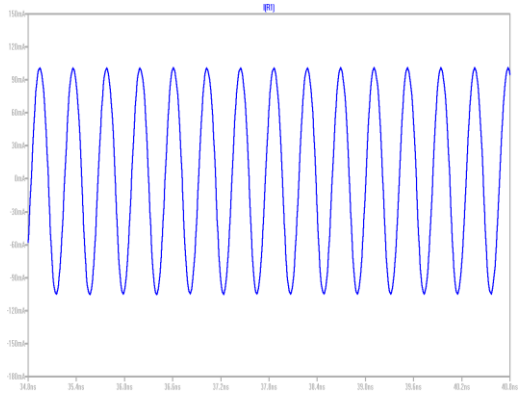

Figure 6. Plot of Inductor Current (mA) vs time (ns)

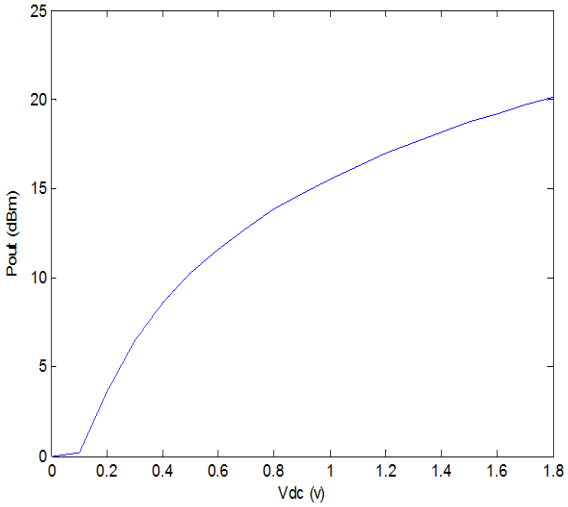

Figure 7. Plot of Vdc (v) vs Pout (dBm)

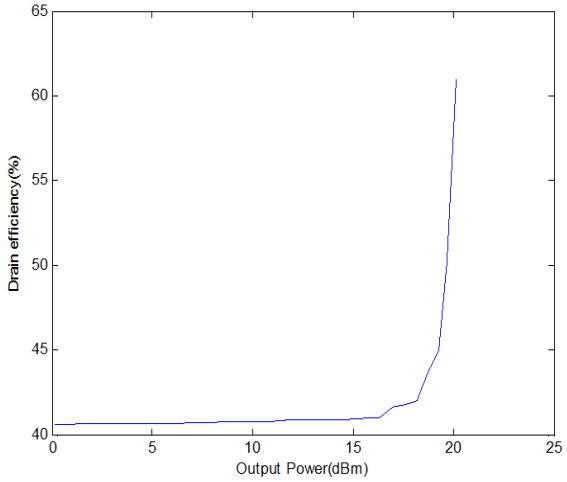

Figure 8. Plot of Power Added Efficiency (%) Vs Pout (dBm)

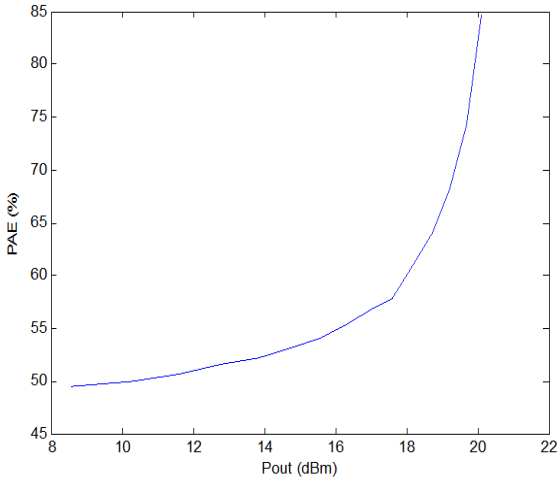

Figure 9. Plot of PAE (%) vs Pout (dBm)

B. Class-E RF tuned Power Amplifier Design:

The figure given below shows a RF tuned Class-E RF power Amplifier.

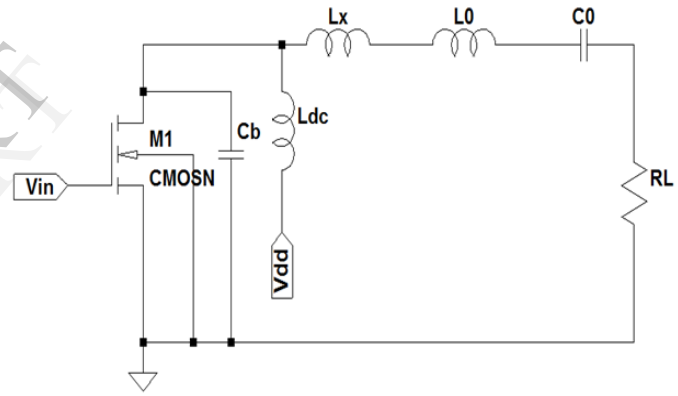

Figure 10. Diagram of Class-E RF Tuned Power Amplifier

As shown in the fig.10 an additional inductor Lx has been used to provide RF tuning so that the output power can be controlled and better dynamic range and PAE can be obtained. Usage of additional varactors is also possible instead of an inductor.

When the switch is ON the current flowing through the active device is equal to the DC current minus the output current.When the switch is turned OFF the DC current minus the output current will charge the shunt capacitor Cb. The shape of the drain voltage of the active device in the OFF state, which equals to the voltage across the capacitor Cb, is controlled by the output network. The output network is designed to turn the voltage across Cb back to zero (fully discharge the Cb) before the switch is again turned ON. The output current is filtered by the ideal series resonant circuit and therefore it is assumed to be sinusoidal. It can be seen that the sinusoidal output current is a sum of partial sinusoid

currents through the switch (during ON state) and through the shunt capacitor Cb (during OFF state).

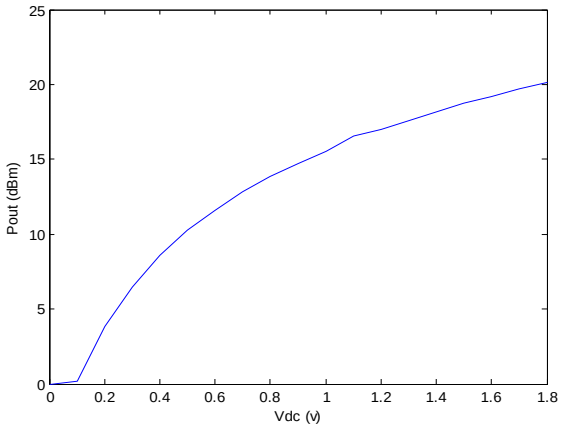

Figure 11. Plot of Vdc (v) vs Pout (dBm)

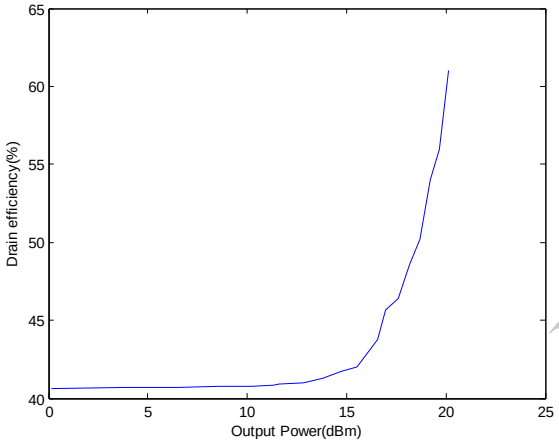

Figure 12. Plot of Drain Efficiency (%) Vs Pout (dBm)

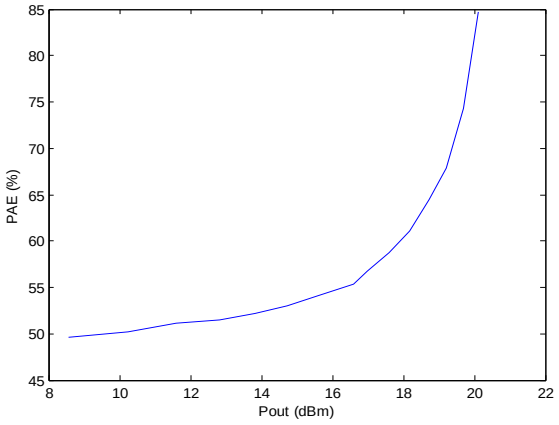

Figure 13. Plot of PAE (%) Vs Pout (dBm)

C. *Level Shifter:*

The level shifter has the capability of generating a wide range of output signals. To interface the low voltage to high voltage circuits, level shifters are required and these in turn add delay . The level shifter implemented here comprises of an amplifier and a buffer stage.

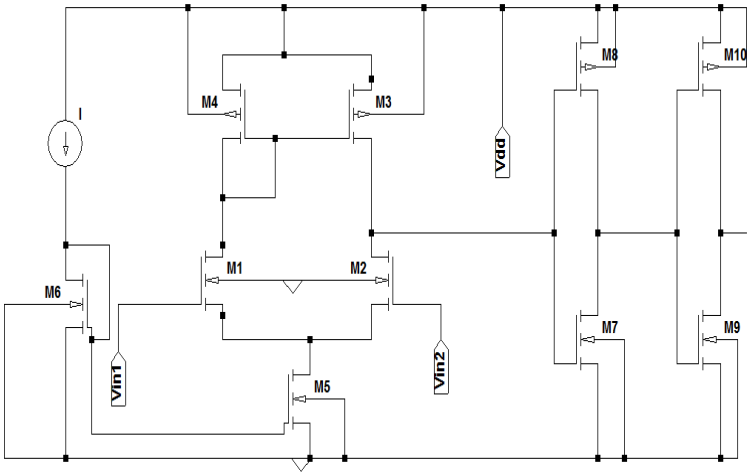

Figure 14. Level Shifter

The simulated waveform of the conventional level shifter is as shown below.

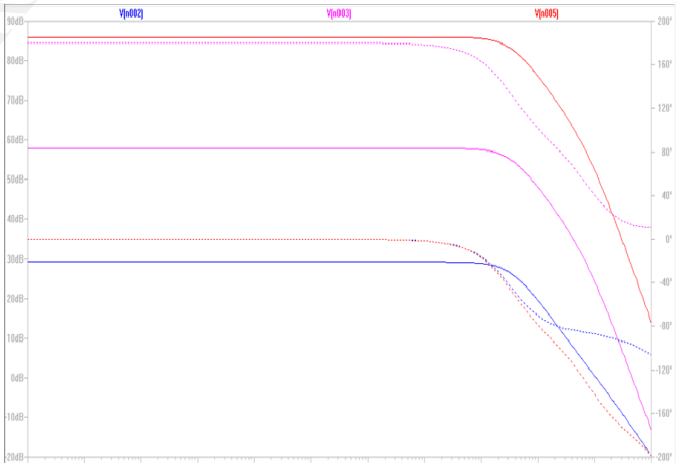

Figure 15. Conventional level shifter o/p waveform

The output waveform of the level shifter along with some dc offset is given to the input of the cascode RF tuned Class-E power amplifier. This cascode modulated signal is given to the input (Vbias) of the power amplifier as shown in fig.16 for level adjustment.

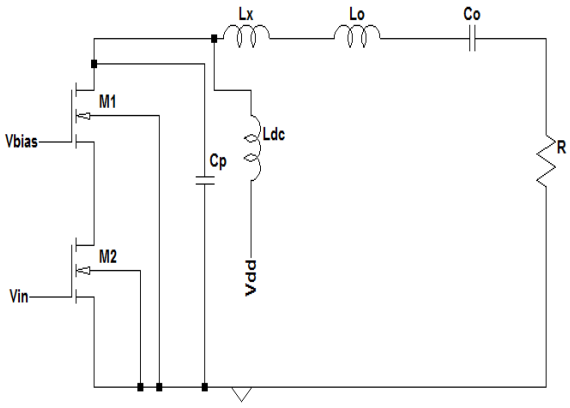

Figure 16. Cascode modulated class-E power amplifier

VI. IMPLEMENTATION & RESULTS

The design is implemented using LtSpice and the various plots between various specifications of the Class-E power amplifier have been obtained by using Matlab. The table below summarizes the comparision of the existing work available in literature with the current work.

TABLE 1: COMPARISION WITH EXISTING WORK

	Tech(nm)	Freq (GHz)	Power Supply (V)	Peak Pout (dBm)	Peak PAE (%)	Pout Dynamic Range (dBm)
Ref[1]	350	2	3	13	50	-------
Ref[2]	180	2.2	1.6	18	35	35
Ref[3]	130	2.4	2.0	18.6	57	34.5
Ref[12]	180	2.4	2.4	23	42	-------
Ref[14]	250	1.4	1.5	25	49	17
This work	**180**	**2.4**	**1.8**	**20.1**	**64**	**18**

VII. CONCLUSION

This paper has undergone an extensive review of the existing research works on Cascode modulated Class-E RF power Amplifiers. The design was implemented using 180 nm technology. The design operates at a frequency of 2.4 GHz and a power supply voltage of 1.8v. The peak output power is found to be 20.122 dBm which is an improvement over that of the value obtained in the previous works as available in literature. The power added efficiency was found to be 64 % which is 7% more than the earlier works. The dynamic range was found to be 18 dBm.

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