An Efficient Advanced High Speed Full-Adder Using Modified GDI Technique

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Abstract

In this paper, high performance full adder circuit is proposed. A full-adder is one of the essential components in the designing of digital circuit, many improvements have been made to reduce the architecture of a full- adder. The proposed method for designing a one bit full adder aims on GDI(Gate Diffusion Input). Analysis is based on some simulation parameters like number of transistors, power, delay, power delay product of the digital circuit. The proposed full adder using GDI technique used to reduce the power up to 0.135nw .

Index Terms: *CMOS,CPL,DPL, GDI, PDP,TFA*

I.INTRODUCTION

Most of the VLSI applications extensively use logic gates and arithmetic circuits (AND, OR Addition, subtraction and multiplication are examples of the most commonly used operations).Full Adder cell is the most significant and basic block of an arithmetic unit of a system. Obviously, improving its performance directly leads to improving the performance of the whole system.

One bit full adder cell is the widely used in arithmetic circuits thus, ornamental their performance is critical for ornamental the overall module performance recently building low power VLSI systems has emerged as highly in demand because of the fast growing technologies in mobile communication and computation .So designers are forced with more constraints like high speed, high throughput, reduced area and at the same time low power consumption The goal of this paper is designing a high speed full adder cell with low power using GDI techniqueThe most important performance parameters of the VLSI systems are power consumption, speed, and reliability. Designing low-power VLSI systems has become an important because of the fast growing technology in mobile computation and communication.

Different techniques have been presented for low power full adder. The composition of the rest of this paper is organized as follows: Literature Survey of different full adders is presented in section [2], different full adder's performance and results are shown in section [3] and the conclusion is presented in section [4].

II. LITERATURE SURVEY OF FULL ADDERS

2.1 Full Adder design using the complementary pass- transistor logic (CPL Logic)

The internal logic structure shown in fig 1 has been adopted as the standard configuration in most of the enhancement developed for the 1-bit full-adder module. In this pattern the adder module is formed by three main logic blocks a XOR/XNOR gate to obtain XOR and XNOR from Block 1 and XOR blocks or multiplexers to obtain SUM(So), CARRY(Co) out puts from BLOCK 2 and BLOCK 3.

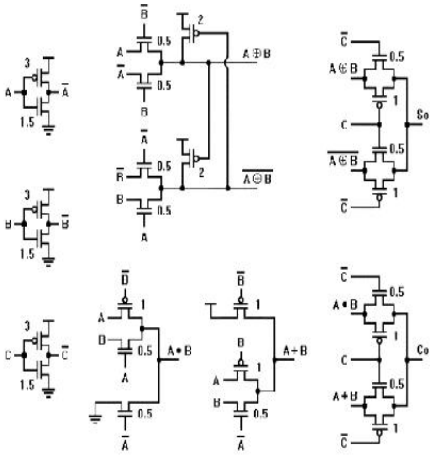

Fig 1: Block diagram of full adder cell

There are standard topologies of implementation for the full-adder cells which are used as the basis of comparison in this paper.CMOS logic design have been used to implement the low- power 1-bit adder cells.The complexity of full CMOS pass gate logic can be reduced dramatically by adopting another circuit called CPL. The main idea behind CPL is to use a entirely NMOS pass transistor network for the logic operations. All the input signals are applied in paired form. That is every input signal and its inverse should be provided. The circuit also produces paired output, to be used by subsequent CPL.

CPL Schematic:

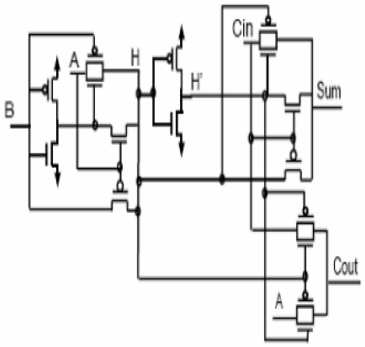

Fig 2: Schematic of CPL Full adder cell

2.2 Full Adder design using dual pass transistor logic (DPL Logic)

The other new full-adder have been designed using the logic styles (Fig.3) presents a full-adder designed using a DPL logic style .Here XOR or XNOR gates and pass transistors based MUX is used to obtain *So*. In Fig. 3, the SR-CPL logic style was used to build these XOR/XNOR gates. In both cases, the AND/OR gates have been built using a powerless and groundless pass-transistor configuration and a pass-transistor based multiplexer to get the *Co* output .

DPL Schematic:

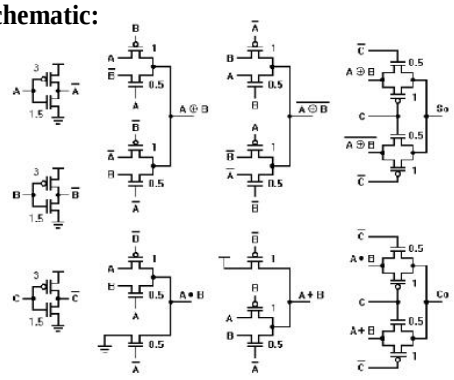

Fig 3: Schematic of DPL Full adder cell

2.3 Transmission Function Full Adder(TFA)

Vahid foroutan, keivan navi and majid haghparast says that Transmission function full adder is based on transmission function theory. Transmission Function one bit full Adder is one of the full adder implementation techniques. Transmission function full adder consists of 16 transistors, as shown in Fig.4 . A, B and Cin are the inputs and Sum and Cout are the outputs. This circuit uses both NMOS and PMOS transistors. There is no voltage drop problem but it requires double the number of transistors to design the function. This full adder is low power intense but they are good for designing XOR and XNOR gates. The main disadvantage in this logic style, is lack of driving capability and more number of transistors will be needed.

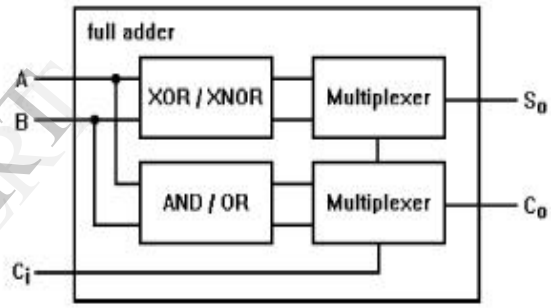

Fig.4 Transmission function full adder

2.4 Full Adder Using Majority Function

Keivan Navi, Mehrdad Maeen, Vahid Foroutan, Somayehtimarchi And Omidkavehei says that the majority function is a logic circuit that performs as a majority vote to dertermine the output of the circuit. Fig.5 is a Full Adder using majority function. The action of full adder is as follows: if three inputs are given to the full adder as A,B and Cin then it should calculate and give two 1-bit outputs as sum and cout.

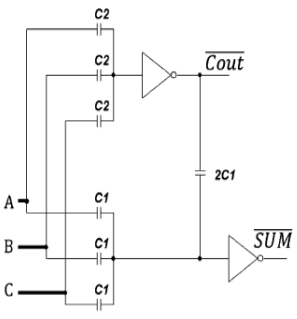

Fig. 5 Full adder using majority function

Two inverter gates are used in this full adder. The static CMOS inverter is used as the inverter gate. Carry signal is generated by majority function and at the same time sum signal is generated by majority not function. By considering majority function truth table, the majority function returns logic 1, only if there is more logic 1's than logic 0 is given at the input. The Majority not is the reverse of the majority function.

2.5 Full Adder design using GDI technique

Gate diffusion input is a novel technique for low power digital circuit design in an embedded system. This technique allows lessening in power consumption, delay and area of the circuit. This technique can be used to decrease the number of transistors compared to conventional CMOS design. Recently, a novel design called Gate-Diffusion Input (GDI) is proposed by Morgenstern *et. al.*. It is a genius design which is very flexible for digital circuits. Besides, it is also power efficient without huge amount of transistor count. Although GDI has the above advantages, it still has some difficulties that are needed to be solved. The main problem of a GDI cell is that it needs twin-well CMOS or silicon on insulator (SOI) process to realize. Thus, it will be more luxurious to understand a GDI chip. However, if only standard Pwell CMOS process can be used, the GDI scheme will look the problem of lacking driving capability which makes it difficult to understand a viable chip. In this paper, a modified GDI scheme is proposed to accept the general CMOS The basic GDI cell and truth table is shown below. In that the source of the PMOS in a GDI cell is not connected to VDD and the source of the NMOS in a GDI cell is not connected to GND.

BASIC GDI CELL:

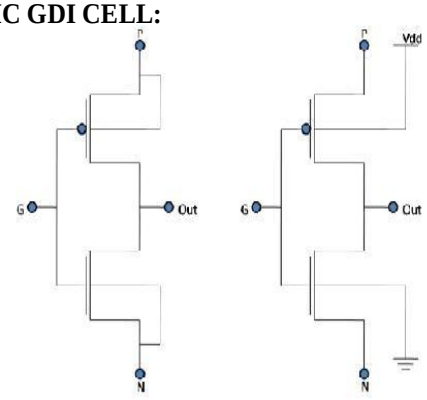

Fig 6: GDI basic cell

This characteristic gives the GDI cell two extra input pins to use which makes the GDI design more flexible than an common CMOS design. However, this feature is also the major cause of its difficulty: special CMOS process required. To be more explicit, the GDI scheme needs twin-well CMOS or silicon on insulator (SOI) process to implement which is of course more luxurious than the standard p-well CMOS process.

Some modifications in the standard CMOS inverter derives the basic GDI cell, where the source of NMOS and PMOS are fed by input signals.GDI cell consists of three input terminals G, P and N. The various functions that can be implemented with basic GDI cell, which consists of only two transistors is as shown in below.

Table:I The various functions of GDI basic cell

N	P	G	Out	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

The main advantage of GDI is large number of functions can implemented using basic GDI cell From it can be seen that large number of functions can be implemented using the basic GDI cell. MUX design is the most difficult design that can be implemented with GDI, which requires only 2 transistors, which requires 8-12 transistors with the traditional CMOS or PTL design. Many functions can be implemented efficiently by GDI by means of transistor count shows the comparison between GDI and the static CMOS design in terms of transistors count. A. Bazzazi and B. Eskafi says that Full adder cell with the GDI technique is implemented to design a high performance and low power full adder cell. Fig 7 shows the new adder implemented in GDI technique.

GDI cell contains three inputs – G (common state input of NMOS and PMOS), P (input to the source or drain of PMOS) and N (input to the source or drain of NMOS). a, b, cin are taken as one bit input for one bit full adder. Sum and carry are generated by using inputs. There are 24 transistors in full adder cell. Full

adder is divided into two stages, GDI technique is used in first cell to generate XOR and XNOR functions.

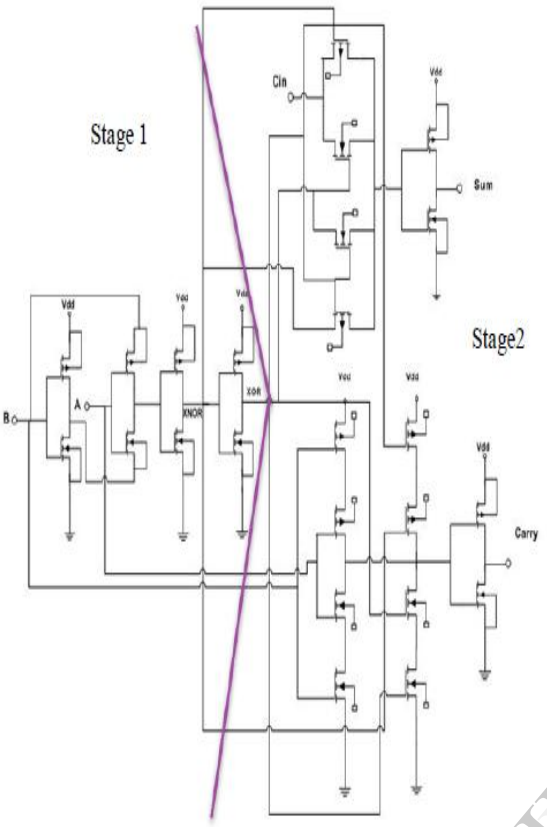

Fig. 7 New adder implemented in GDI technique

Full swing with low voltages is shown in first stage and complementary outputs with other inputs will be fed to the second stage. Sum and carry is generated in second stage. This full adder is implemented in HSPICE in 0.18um CMOS technology with supply voltage of 1.8v. The power consumption of this adder is 0.78uw and delay is 50ns.

2.6 Full Adder Using Mod2f Cell

Mod2f Full Adder cell of Fig. 8 , which has 14 transistors, generates full swing XOR and XNOR signals by utilizing a pass transistor based Differential Cascode Voltage Switch circuit. As mentioned in this leads to higher speed and better performance in comparison with the circuit proposed in . Then it utilized this circuit jointly with a pass-transistor network to generate a non full swing Sum signal and with a transmission gate network to generate a full swing Cout signal. Due to using pass transistor networks, the output signals of Mod2f do not provide a good driving power.

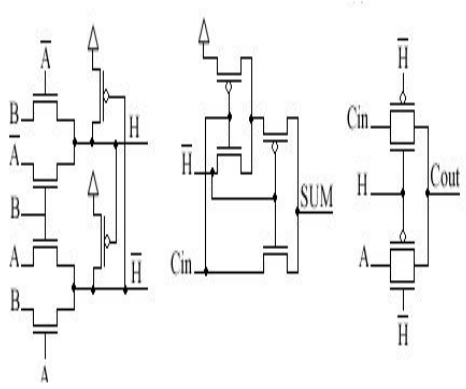

Fig.8 Mod2f Full Adder cell

2.7 Full Adder Using 24T

Full Adders are based on a fully symmetric CMOS style, called Bridge style. FA24T has 24 transistors and Bridge has 26 transistors. In FA24T a Bridge circuit generates C_{out} and another Bridge circuit is utilized in series with the prior one to generate Sum, while in Bridge Full Adder, C_{out} and Sum signals are produced in a parallel manner. The body of FA24T has two transistors less than Bridge and has better power consumption. However in FA24T the Sum generator should wait to receive the C_{out} signal from the C_{out} generator, therefore the delay of FA24T is more. Although the series structure of FA24T forms a weak driver in the output, however the output inverters provide a good driving power to the cascaded cells. Hence, FA24T has a better drivability. The advantages of CMOS Bridge style is higher performance, robustness, and symmetry.

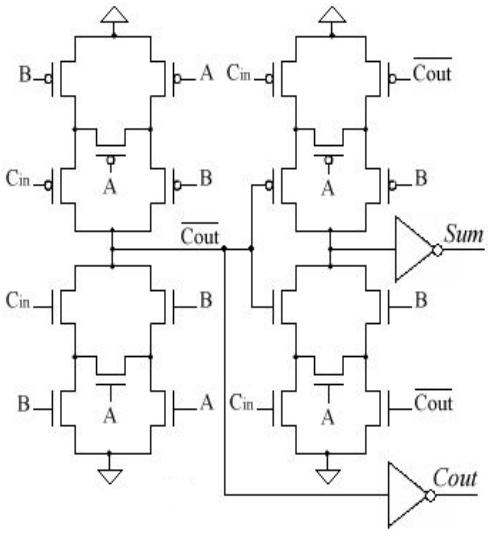

Fig.9 24T Full Adder

2.8 Full Adder Using N-CELL

N-CELL1 has 14 transistors and utilizes the low-power XOR/XNOR circuit and a pass transistors network to produce a non full swing Sum signal and uses four transistors to generate a full swing C_{out} signal, which do not provide enough driving power. However N- CELL1 Full Adder cell has 12 transistors.

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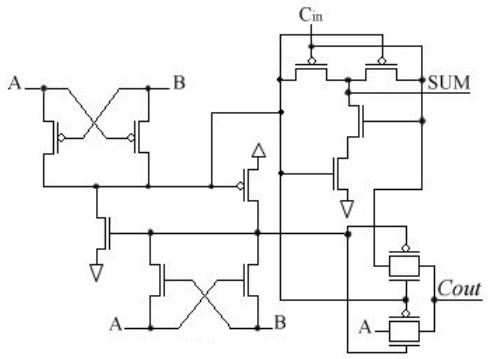

Fig.10 N-CELL Full Adder cell

2.9 The proposed full adder cell with modified GDI technique

Gate-Diffusion-Input (GDI) method is based on the use of a simple cell as shown in figure .11 The modified GDI cell same as normal CMOS inverter but it has some significant differences .

1)GDI cell contains three inputs - G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS).

2) Bulks of both NMOS connected to N and PMOS connected P .So it can be randomly biased at contrast with CMOS inverter. All the functions are not possible in standard P-Well CMOS process, but can be effectively implemented in Twin-Well CMOS or SOI technologies.

But the modified GDI cell is shown in figure 11 can be implemented in N-Well CMOS Technology by connecting Bulks of NMOS to GND and PMOS to VDD .Here, whenever the P and N terminals are connected to logic 0 should not use GND and logic 1 VDD. That is need to generated logic 0 and logic 1 signals separately and can be connected.

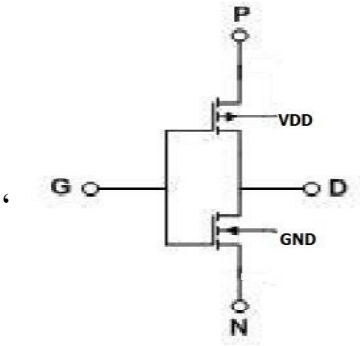

Fig. 11- Modified GDI basic cell

Table II: Some logic functions that can be implemented with a single GDI cell

N	P	G	D
'0'	B	A	A'B
B	'1'	A	A'+B
'1'	B	A	A+B
B	'0'	A	AB
C	B	A	A'B+AC
'0'	'1'	A	A'

Table II shows how a simple change of the input configuration of the simple GDI cell corresponds to very dissimilar Boolean functions. Most of these functions are complex in CMOS.The standard PTL implementations very simple because only 2 transistors per function in GDI design method. OR function is the input variable in adder equation. The modified GDI technique used for generating of XOR function. It uses only 6 transistors to generate the XOR function.

The goal of this paper is to design a high performance and low power full adder cell with the GDI technique. The full adder cell has eighteen transistors that is shown in figure12. In the first stage of this cell, the modified Gate Diffusion Input technique is used for generating XOR functions. This phase shows full adder move back and forth with little voltage. The Sum and Carry outputs are generated from the first stage. Since the adder cells are usually cascaded to form a usual arithmetic circuit and their capabilities must be ensured. The proposed full-adder cell schematic and layout are shown in the figure 12.

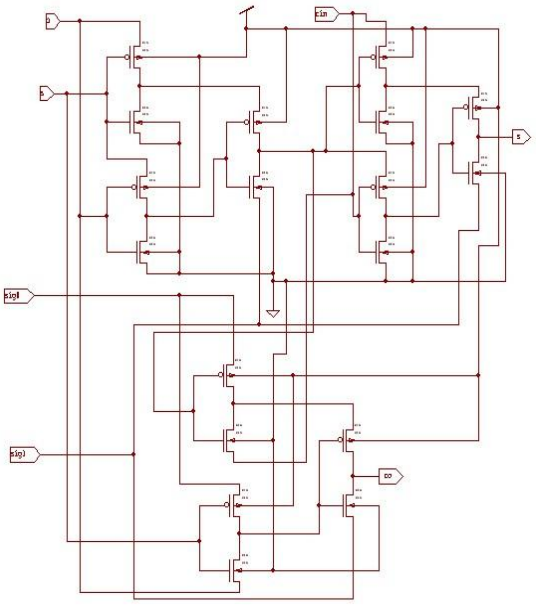

Fig.12- The proposed full adder cell with modified GDI technique

III SIMULATION RESULT

1-bit Full Adder cells including FA24T, CPL, DPL, N- CELL, Mod2f, Transmission function full adder, Full adder using Majority function, full adder cell with GDI technique and also our Modified full adder using Modified GDI technique have been prototyped and simulated. Simulations were done by the aim of minimizing the power consumption by adopting minimum-size transistors. Advantages of Proposed full adder using Modified GDI are good driving capability and better power delay performance. The power dissipation is 0.135nw and delay 1.68 ns.

Table III survey of other full adder with full adder using modified GDI technique

Adders	Number of transistors	Supply voltage	Technology	Power	Delay (sec)	Power delay product
Full Adder Using CPL Logic	26	1.8V	0.18µm	29.18 µw	$1020*10^{-12}$	2973.6 Ws
Full Adder Using DPL Logic	28	1.8V	0.18µm	26.510 µw	$41*10^{-12}$	1086.91 Ws
Transmission Function Full Adder	16	1.8V	0.18µm	3.0357 µw	$0.1325*10^{-9}$	0.4022fj
Full Adder Using Majority Function	4	0.8V	0.18µm	0.5451 µw	$0.687*10^{-9}$	0.3745fj
Full Adder Cell With GDI Technique	24	1.8V	0.18µm	0.78 µw	$50*10^{-9}$	39aj
Full Adder Using Mod2f Cell	-	1.8V	0.18µm	2.238 µw	$0.877*10^{-10}$	$19.62*10^{-17}$j
Full Adder Using 24T	24	1.8V	0.18µm	1.669 µw	$1.379*10^{-10}$	$23.01*10^{-17}$ j
Full Adder Using N-Cell	-	1.8V	0.18µm	1.622 µw	$0.632*10^{-10}$	$10.25*10^{-17}$ j
The Proposed Full Adder Cell With Modified GDI Technique	18	1.8V	0.18µm	0.135 nw	$1.68*10^{-9}$	--

IV. CONCLUSION

The aim of this work is two have been power reduction and speed increase in the full adder. In this operation the GDI technique was introduced. By using technique full adder could reduce the power consumption. As a result, the full adder works with 0.138 nw power consumption.

In this paper, various types of full adder cells designs have been reviewed from the most recent published research work. The assessment of full adder cells with each other in term of power, delay, supply voltage and transistors count is done. Different logics are used in this paper to build the full adder to reduce the power, delay, and power delay product and transistor count.

REFERENCES

[1].M.Moaiyeri, R. Faghih Mirzaee, K.Navi, "Two New Low Power and High Performance Full Adders", Journal of Computers, Vol. 4, No. 2, February 2009.

[2].R. Shalem, E. John, L.K. John, "A novel low-power energy recovery full adder cell", in: Proceedings of the Great Lakes Symposium on VLSI, February 1999, pp. 380–383.

[3].Keivan Navi, Mehrdad Maeen, Vahid Foroutan, Somayeh timarchi And Omidkavehei, "A Novel Low Power Full Adder Cell For Low Voltage", integration, the VLSI Journal 42, 2009

[4].Mariano Aguirre, Monico Linares, "An alternative logic approach to implement high-speed low-power full addercells", ACM Proc. Symp.Integrated circuits and system design,pp.166-171,Florianolpolis, Brazil, September,2005.

[5].B.Sathiyabama And Dr.S.Malarkkan, "Novel Low Power HybridAdders Using 90nm Technology for DSP Applications," ISSN:2278-067X, volume 1, Issue 2 (May 2012). [6]

[6].A. Bazzazi And B.Eskafi, "Design And Implementation Of Full Adder Cell With Gdi Technique Based On 0.18um Cmos Technology", volume 2, 2009

[7].Dr.P.T.Vanathi,Dr.J.Ramesh, K.Revathy, R.Preethi, C.Haritha Laxmi and K.Keerthana, "Performance Analysis Of High Performance Adder Architectures", 2012.

[8].K. Navi, O. Kavehie, M. Rouholamini, A. Sahafi, S.Mehrabi, "A Novel CMOS Full Adder," 20th International Conference on VLSI Design held jointly with 6th International Conference on Embedded Systems (VLSID'07), pp. 303-307, Jan. 2007, Bangalore, India.

[9].Keivan Navi, Omid Kavehei, Mahnoush Ruholamini, Amir Sahafi, Shima Mehrabi and Nooshin Dadkhahi, "Low-Power and High-Performance 1-Bit CMOS Full Adder Cell" JOURNAL OF COMPUTERS, VOL. 3, NO. 2, FEBRUARY 2008.

[10].Fartash Vasefi and Z. Abid, "Low Power N-bit Adders and Multiplier Using Lowest Number of Transistors 1- bit Adders", IEEE conference proceeding of CCECE/CCGEI, Saskatoon, May 2005,pp.1731-1734.

[11].A.R, Saberkari, SH. Shokouhi, "A Novel Low-Power-Voltage Cmos 1-Bit Full Adder Cell with the GDI Technique", Proceeding of The 2006 IJME-INTERTECH conference.

[12].C. H. Chang, J. Gu and M. Zhang, "A review of 0.18um full adder performance for tree structured arithmetic circuits",IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 13, No. 6, pp.686- 695, June 2005

[13].Vahid Foroutan, Keivan Navi and Majid Haghparast "A New Low Power Dynamic Full Adder Cell Based on Majority Function", World Applied Sciences Journal 4, 2008

[14].A. M. Shams, T. K. Darwish and M. A. Bayoumi. "Performance Analysis of Low Power 1-Bit CMOS full adder cells", IEEE Transaction on VLSI Systems, Vol. 10, Feb. 2002.

[15].C. H. Chang, J. Gu and M. Zhang, "A review of 0.18um full adder performance for tree structured arithmetic circuits", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 13, No. 6, pp.686- 695, June 2005

[16].K. Navi, O. Kavehie, M. Rouholamini, A. Sahafi, S.Mehrabi, "A Novel CMOS Full Adder," 20th International Conference on VLSI Design held jointly with 6th International Conference on Embedded Systems (VLSID'07), pp. 303-307, Jan. 2007, Bangalore, India.