All Optical Implementation of Mach-Zehnder Interferometer based Reversible Sequential

B. Surya
Department of VLSI DESIGN

***Abstract*—This work presents all optical reversibleimplementation of sequential counters using semiconductoroptical amplifier (SOA) based Mach-Zehnder interferometer(MZI) switches. All the designs are implemented usingminimum number of MZI switches and garbage outputs. Thisdesign ensures improved opticalcosts in reversible realization of all the counter circuits. The theoretical model is simulated to verify the functionality of the circuits. Design complexity of all the proposed memory elements has been analyzed.**

Keywords—Reversible computing, Mach-Zehnder Interferometer(MZI), counter, optical cost, optical delay, garbage

I. INTRODUCTION

Like Boolean logic functions, reversible logic function [1-3]is a special type of logic function where there always existsa bijective mapping between inputs to outputs. For a givenreversible function, it is always possible to extract originalinputs from its outputs correctly, that means it ensures noloss of information while retrieving original data. Theconcept of reversible logic was first introduced by Landauer[1] and Bennet [4]. According to their claims, if a process orfunction is reversible, then there is no loss of informationwhich causes heat generation from the system. They alsoexperimentally established that a certain amount of energy(KT ___ _ Joules) would be dissipated as heat in thetraditional logic computation for every bit of informationloss during the computing process. So, it is seen that if alogic circuit can be made reversible, then it ensures zeroheat dissipation [2] and no loss of informationcharacteristics.The problems withtraditional logic circuit has beenhighlighted by Ralph Merkle from Xerox PARC, whoexperimented [6] on 1GHz computer processor packed with1018 traditional logic gates in a volume of 1 cm3operating at a room temperature and found that a huge amount of powernearly 3MW releases from the surface area of thatprocessor. Now a day's, the VLSI industry is facing seriouschallenges due to the heat generation problem in IntegratedCircuits (IC) and this problem will become severe in next10-20 years according to Moore's Law [7] due to theincreasing miniaturization and the exponential growth ofnumber of transistors in integrated circuits. To address theseissues, the reversible computing has evolved as analternative as it promises zero power dissipation [2] incircuit simulation. Reversible logic has applications in the several emerging technologies like ultra low power CMOSdesign, optical computing [5], nanotechnology [6] and DNAcomputing [1]. Design of the reversible carry-look-aheadadder using control gate and its physical implementationhave been first reported in [8] where the circuit is poweredby their input signals only and does not need any additionalpower supplies.Recently, the researchers are aiming at the development ofthe optical digital computer system for processing binarydata usingoptical computation. Photons are the source ofoptical technology. This photonic particle provides unmatched speed with information as it has the speed oflight. The installation of optical components in the electronic computer system produces optical-electronichybrid network. The researchers are trying to combine theoptical interconnects with the electronic computing devices.The implementation of reversible logic circuits with opticaltechnology can be performed using Semiconductor OpticalAmplifier (SOA) based Mach-Zehnder Interferometer(MZI) switches which has significant advantages of the highspeed, low power, fast switching time and ease offabrication [11-10].The optical computing concept in design and synthesis ofreversiblelogic circuit has first been introduced in [12].Generalized implementation of reversible gate like Toffoli,Fredkin, and CNOT using optical technology has beenreported in [10], where MachZehnderinterferometer (MZI)is used to implement all-optical reversible logic gates.Reversible implementation of NOR gate using SOA basedMZI switches is realized in [11]. The optical implementation of functionally reversible Mach-Zehnder Interferometer based binary adder has been proposed in[12], where two new optical reversible gates ORG-I andORG-II have been proposed in addition to existing Feynmangate to implement the architecture. The implementation ofAll-optical XOR gate using SOA-based MZI and microresonators has been reported in [13] and [14], respectively.Apart from use of MZI to design reversible gates, TOAD(terahertz optical asymmetric demultiplexer)-based and allopticalfiber-based implementation of Fredkin gate ispresented in [15] and [16], respectively.The sequential circuit is one of the most importantcomponents of the computer system and the efficient of thememory element is a primary concern in this circuit. As thereversible circuit promises information lossless and no heatgeneration property, an intensive research is going on design and implementation of the sequential circuit using reversibletechnology.In the initial phase of the reversible logic circuit design, theresearchers have primarily focused on the design andimplementation of the reversible combinational circuitsbecause the researchers have predicted that the feedback isnot allowed in reversible computing. However, based on hisfundamental work reported in [3], Toffoli argued that "asequential network is reversible if its combinational part(i.e., the combinational network obtained by deleting

thedelay elements) is reversible" i.e. feedback can be allowedin the reversible computing. The first design of thereversible sequential circuit with JK latch having thefeedback loop from the output has been presented byFredkin in [19]. Further, Rice has also proved in [17] that the sequential reversible networks are also reversible innature.The necessity for the sequential reversible logic is discussedby Toffoli [3] and Frank [18], but any structure for itsofsequential element in the form of a JK flip-flop usingconservative logic has been proposed by Fredkin andToffoli [19]. Picton has presented a reversible RS-latch in[22]. But Picton's model faces one problem that this modelcannot avoid fan-out problem which is essential property ofthe reversibility.This fan-out problem of Picton's model [22] has been solvedby Rice [17] in 2006. In [18], Rice has implementedreversible RS latch. Recently, Rice [20] has analyzed thedesign of the reversible RS latch in details. The workproposed in [21] has shown that how transistor can be usedto design reversible sequential circuit from the physical implementation point of view.Till date, insufficient number of works on reversiblememory element has been reported. Some preliminaryworks on the reversible implementation of latches, flipflops,shift register, counters using quantum technologyhave been reported. We have reviewed works where alloptical functionally reversible gates are designed by variousresearchers. Getting inspired by the existing works in thedomain of reversible implementation of sequential circuits,after several investigations we have focused on thedesigning of all optical implementation of reversiblecounters.The rest of the paper is organized as follows. Section IIIdescribes reversible preliminaries. The proposed techniquewith examples is discussed in Section IV. Finally, section V concludes the work.

II. BACKGROUND

In this section, first, the fundamental of reversible logic andcircuit is introduced. Next, the optical architecture of MZIswitch and its working principle are explained. Design ofbasic reversible gates like CNOT, Toffoli, and Fredkinusing all optical MZI switches are presented [10-11].

A. Reversibility:
A fan-out free circuit (*Cnf*) with circuit depth (*d*) over the setof input lines X ={*x1, x2, …,xn*} is said to be reversible (*Rc*)if the mapping from input to output is bijective (*f* : B*m*_ B*n*)and the number of inputs (*m*) is equal to number of outputs(*n*) i.e. *m* = *n* and also the circuit consists of reversible gates(*gi*) only i.e. *Cnf =g0 .g1.g2. … .g(d-1),*where *gi* represents *i*threversible gate of the circuit.

*B. MZI Architecture:*Design of reversible logic gates like NOT, *k*-CNOT, Toffoli,Fredkin, Peres may be possible in many ways. Among them, the quantum and optical technology are two veryprominent.From the quantum technology point of view, the basicquantum gates such as NOT, CNOT, V and V+ are used toimplement the reversible gates. In optical domain, MZIbased optical switches are used to implement opticalreversible gates [10-11].An optical MZI switch can be designed using thefollowing components: two Semiconductor Optical Amplifiers (SOA-1, SOA-2) and two couplers (C-1, C-2) as shown in Fig. 1.MZI switch has two inputs ports namely, A and B and twooutput ports known as bar port and cross port, respectively.The optical signals coming at port B and port A at the inputside are the control signal (_2), and the incoming signal (_1),asfollows.

• When both incoming signal at port A and control signal atport B are high (i.e. A=1, B=1), then the light will appearat the output bar port and no light is seen at the outputcross port.

• Again, due to the absence of control signal at input port Band the presence of incoming signal at input port A (i.e.A=1, B=0), then the light appears at the output cross portand no light at the output bar port is observed.

• In all other cases, (i.e. A=0, B=1 and A=0, B=0), no lightappears at output bar port and output cross port.
The logic values of the absence of the light and the presence of light are denoted by 0 and 1, respectively. From theperspective of boolean functions, the above behavior of MZIswitch can be written as R (Bar Port) =*A.B* and S (CrossPort) =*A*__

C. Beam Combiner (BC) and Beam Splitter (BS):
Beam combiner (BC) simply combines the optical beam while the beam splitter (BS) splits the beam into two opticalbeams. According to [11-12], the optical cost and the delayof beam combiner and beam splitter are very negligible.Hence, while calculating optical cost of a circuit, they areassumed to be zero.

D. Optical cost and delay
As the optical cost of BS and BC is comparatively small, theoptical cost of a given circuit is the number of MZI switchesrequired to design the realization. Optical delay is estimated as the number of stages of MZI switches multiplied by aunit _*.E. Design of reversible gates with MZI*
MZI-based optical design of functionally reversible Feynman and Fredkin gate are depicted in Fig. 2(a) and Fig.2(b), respectively. Standard optical cost and delay of somereversible benchmarks are presented in Table-I.

III. PROPOSED WORK

In this section, we present all optical implementation ofcounters with the property of functional reversibility.Semiconductor Optical Amplifier (SOA) based Mach-Zehnder Interferometer (MZI) switches are used to designthe sequential circuits. Our primary objective in this work isto achieve the reversible implementation of counters withminimum number of ancilla lines and MZI switches. Alloptical implementation of MZI-based asynchronous andsynchronous counter is presented. Mathematical modeltosimulate the proposed architecture has also been presented.Finally, design complexities of all the counters are analyzed.

A. Asynchronous Counters

Asynchronous counter is known as ripple counter.Design architecture and working principle of all opticalfunctionally reversible asynchronous down counter ispresented here. The mathematical model for simulation ofthis memory element is described.

A.1. Design of 2*-bit positive edge triggered down counter*The schematic diagram of MZI based 2-bit positive edgetriggered down counter is depicted in Fig. 3(a), which isconstituted with two positive edge triggered D flip flops viz.FF-0 and FF-1. Each of the positive edge triggered D flipflopconsists of three MZI switches viz. MZI-1, MZI-2 andMZI-3, two beam combiner (BC) namely BC-1, BC-2 andfour (expect the last flip flop viz. FF-1) beam splittersnamely BS-1, BS-2, BS-3, BS-4.For proper understanding, we discuss the signal flowcharacteristic of the counter as shown in Fig. 3(a). A lightfrom input port CP (Clock Pulse) directly incidents on MZI-1 of FF-0 and acts as incoming signal. Similarly, anotherlight signal from input port D0 directly enters into MZI-1 ofFF-0 and acts as control signal of MZI-1.The light from barport of MZI-1(B1) and a part of light from cross port ofMZI-3(C3) is combined by BC-1 together to producecontrol signal of MZI-2. In the same way, the outputlightsfrom cross port of MZI-1 (C1) and MZI-2 (C2) arecombined by BC-2 and acts as control signal of MZI-3. Aconstant light signal (denoted by 1) incidents on the beamsplitter (BS-1) and splits into two parts, where one partactsas incoming signal of MZI-3 and another part againincidents on another beam splitter (BS-2) and splits into twoparts. One part appears to MZI-2 as incoming signal andanother part that goes to next flip flop (FF-1) acts as aconstant input light signal. The light from the cross port ofMZI-3(C3) is the final output Q0 where as another lightsignal which emits from the cross port of MZI-2 (C2) goesback to port D0 and acts as incoming signal.A part of light comes from BS-5 of FF-0 incident on MZI-1of FF-1 and acts as clock pulse of FF-1. Again, D1 acts asthe input value of FF-1. We have obtained both the signals(clock pulse and input signal) for FF-1 and as the designarchitecture of FF-1 is same as FF-0, we omitted the controlflow description of FF-1.

A.2. Operational principle of 2*-bit positive edge triggered down counter*The operational principle of all the optical asynchronousdown counter as shown in Fig 3(a), is described below.Here, the presence of light is denoted as 1 state and absenceof light is denoted as 0 state.

• ***State I:*** Let Q0=0 and Q1=0. As D0 is directly connectedto __ , hence, the value of D0 is 1. Now, the value of clockpulse is 1 i.e.,

both the control signal and incoming signalare present in MZI-1. Hence, according to the workingprinciple of MZI, only bar port of MZI-1 of FF-0 emitslight which incidents on BC-1 and as a result, an outputlight signal emits from BC-1. On the contrary, the crossport of MZI-1 emits no light which incidents on BC-2.Now, the output signal of BC-1 acts as the control signalof MZI-2 and the input signal of MZI-2 is also present.Therefore, the cross port of MZI-2 emits no light, as aresult, no light incidents on BC-2. The output signal ofBC-2 emits no light and as a consequence, the controlNo. of signal of MZI-3 is absent. As the input signal of MZI-3 ispresent, the cross port of MZI-3 of FF-0 receives lightwhich is the final output Q0 i.e. Q0=1.Now, this Q0 acts as incoming signal of MZI-1 of FF-1and D1, which is directly connected to the ___ , acts ascontrol signal of MZI-1. Therefore, both the incoming signal and control signal are present at MZI-1as both thevalue of D1 and Q0 are 1. Hence, the operational principle of FF-1 becomes similar to FF-0 and the cross port ofMZI-3 of FF-1 emits light i.e. the final output Q1=1. So the next state becomes Q1=1 and Q0=1.

State II: Now, Q1= Q0= 1. Again the clock pulse (CP = 1)and D0 (equals the value of) act as incoming signal andcontrol signal of MZI-1 of FF-1 respectively. Hence, onlyincoming signal is present at MZI-1. According to the working principle of MZI, the bar port of MZI-1 of FF-0emits no light and cross port of MZI-1 of FF-0 emits lightwhich incidents on BC-2. So the output signal of BC-2 ispresent that acts as control signal of MZI-3. Again, the input signal of MZI-3 is also present. So the cross port of MZI-3 receives no light i.e. the value of final output Q0=0.This output Q0 acts as incoming signal of MZI-1 of FF-1and D1 is directly connected to___. So the value of D1 is 0.

As both the incoming signal and control signal are absent at MZI-1 of FF-1, no operation is performed in FF-1.Hence, the final output value of FF-1 does not change and it is same as the previous state's output value of Q1.Therefore, the final output of FF-1 is Q1=1.So the nextstate becomes Q1=1 and Q0=0.

• ***State III:*** Now, Q1 =1 and Q0 =0. The value of D0(directly connected to __) is 1 and the value of clockpulse is 1 i.e. both the control signal and incoming signalare present at MZI-1. So the situation becomes same asthat of FF-0 at first stage. Hence, according toworkingprinciple of FF-0 described in first stage, the final outputof FF-0 is 1 i.e. Q0=1.As Q0 acts as incoming signal of MZI-1 of FF-1 and D1 isdirectly connected to ___ , so the value of D1 is 0.Therefore, only incoming signal is present at MZI-1 ofFF-1. This situation is same as FF-0 of second stage.Hence, according to the working principle of FF-0 as described in second stage, the final output of FF-1 is 0 i.e.Q1=0. So the next state becomes Q1=0 and Q0=1.

• ***State IV:*** In this state, Q1=0, Q0=1 and the value of D0(control signal of MZI-1) is 0. As the value of clock pulseis 1, only incoming signal is present at MZI-1 of FF-0.This situation is same as FF-0 of second stage. Hence,according to working principle of FF-0 as described in second stage, the final output of FF-0 is 0 i.e.Q0=0.FF-0 FF-1

Now, this Q0 acts as the incoming signal of MZI-1 of FF-1and D1 is directly connected to complement of Q1. So thevalue of D1 is 1. As the incoming signal is absent at MZI-1of FF-1, no operation is performed in FF-1. Therefore,

thefinal output value of FF-1 is not changed and it is same asprevious state of Q1. Finally, the output of FF-1 is Q1=0. So the next state becomes Q1=0 and Q0=0.The states of the counter are shown in Table II. The pictorialrepresentation of positive edge triggered asynchronous upcounter, negative edge triggered asynchronous down and upcounter is depicted 3(d),respectively.*A.3.*

In the synchronous counter, all the flip-flops are triggeredsimultaneously. As we have already explained the workingprinciple of asynchronous counter with detailed diagram,hereonly the pictorial representation of all optical reversiblearchitecture of MZI based synchronous up counter (negativeedge triggered) and down counter (positive edge triggered)is depicted in Fig. 3(f) and Fig. 3(g), respectively.Analysis of design complexities of all optical reversiblecounters is presented in table III.

IV. CONCLUSION

In this work, various architectures of MZI basedfunctionally reversible all optical counters have beenproposed. As far as our knowledge is concerned, the design of reversible all optical counter is a newer one. Ourproposed design can be generalized for *n*-bit counter also.The proposed design techniques implement all the optical functionally reversible counters with minimum number ofancillary lines and minimum optical cost. Mathematical model has also been formulated.

REFERENCES:

[1] C. H. Bennett "*Logical reversibility of computation*. IBMJournal of Logical Research and Development", 6:525–532, November 1973.
[2] T.Toffoli, "*Reversible computing*", Tech. Memo-MIT/LCS/TM-151, MIT Lab for Comp. Sci, 1980.
[3] C. H. Bennett, "*Notes on the history of reversiblecomputation*", IBM Journal of Research and Development, 32:16–23, January 1988.
[4] R. Cuykendall, D.Andersen, "*Reversible optical computingcircuits*", Optics Letters 12(7), 542-544 (1987)
[5] G. E. Moore "*Cramming more components onto integratedcircuits*", *Electronics*, 38, January 1965