Algorithmic Noise Tolerant (ANT) Architecture based Low Power Multiplier

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Abstract:- **In this paper, we propose a reliable low power multiplier using ANT architecture with compensation method to reduce the error of fixed-width multiplier for DSP applications. The input number based compensation method is carried out on array multiplier. The proposed architecture not only achieves low power consumption and area efficiency also involves in efficient precision reduction. By using the partial product terms of input correction vector and minor input correction vector, the truncation error is lowered and the hardware complexity of the fixed-width multiplier is simplified. The fixed width RPR is implemented using Xilinx in order to compare the number of Replica's or Redundancy of the multiplier block. This gives a quite basic understanding of the difference between the proposed and the Fixed width RPR blocks. Finally the multipliers are used in low power FIR filters is implemented Xilinx software.**

Index Terms- Algorithmic Noise Tolerant(ANT),Fixed-Width Multiplier, Reduced Precision Replica(RPR).

I.INTRODUCTION

Multipliers play an important role in today's digital signal processing and various other applications. In high performance systems such as microprocessor, DSP etc addition and multiplication of two binary numbers is fundamental and most often used arithmetic operations. Statics shows that more than 70% instructions in microprocessor and most of DSP algorithms perform addition and multiplication. So, these operation dominates the execution time. That's why, there is need of high speed multiplier. The demand of high speed processing has been increasing as a result of computer and signal processing applications. Currently, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip. The rapid growth of portable and wireless computing systems in recent years drives the need for ultralow power systems. A novel algorithmic noise tolerant (ANT) technique combined VOS main block with reduced-precision replica (RPR), which combats soft errors effectively while achieving significant energy saving. However, the RPR designs in the ANT designs are

designed in a customized manner, which are not easily adopted and repeated. The RPR designs in the ANT designs can operate in a very fast manner, but their hardware complexity is too complex. As a result, the RPR design in the ANT design is still the most popular design because of its simplicity. However, adopting with RPR should still have extra area overhead and power consumption. In this paper, the proposed system is an easy way of using the fixed-width RPR. In order not to increase the critical path delay, we restrict the compensation circuit in RPR must not be located in the critical path. As a result, it can realize that the ANT design with lower power consumption, and lower critical supply voltage.

II.ANT ARCHITECTURE DESIGNS

The ANT technique includes both main digital signal processor (MDSP) and error correction (EC) block. To meet ultralow power demand, VOS is used in MDSP. However, under the VOS, once the critical path delay T_{cp} of the system becomes greater than the sampling period T_{samp}, the soft errors will occur. In the ANT technique, a replica of the MDSP but with reduced precision operands and shorter computation delay is used as EC block. Under VOS, there are a number of input-dependent soft errors in its output, $y_a[n]$; however, RPR output $y_r[n]$ is still correct since the critical path delay of the replica is smaller than T_{samp}. Therefore, $y_r[n]$ is applied to detect errors in the MDSP output $y_a[n]$. Error detection is accomplished by comparing the difference $|y_a[n] - y_r[n]|$ against a threshold Th. Once the difference between $y_a[n]$ and $y_r[n]$ is larger than Th, the output $\hat{y}[n]$ is $y_r[n]$ instead of [n]. As a result, $\hat{y}[n]$ can be expressed as

$$\hat{Y}[n] = Y_a[n], \text{ if } |Y_a[n] - Y_r[n]| \leq T\,h$$
$$Y_r[n], \text{ if } |Y_a[n] - Y_r[n]| \geq T\,h \quad \rightarrow (1)$$

Th is determined by

$$Th = \max |Y_o[n] - Y_r[n]| \quad \rightarrow (2)$$

Where $y_o[n]$ is error free output signal. In this way, the power consumption can be greatly lowered while the SNR can still be maintained without severe degradation. Comparing with the Full-Width RPR the Fixed-Width RPR has great advantage.

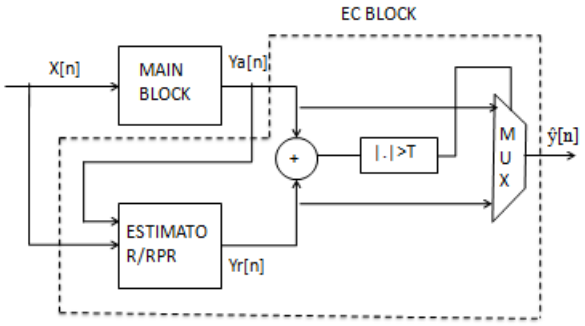

Fig.1 ANT Architecture Design

III. PROPOSED ANT ARCHITECTURE WITH FIXED-WIDTH MULTIPLIER

In this paper, the proposed fixed-width RPR block in the ANT design is shown in fig.2 which can not only provide higher computation precision, lower power consumption, and lower area overhead in RPR, but also perform with higher SNR, more area efficient, lower operating supply voltage, and lower power consumption in realizing the ANT architecture. It demonstrate our fixed-width RPR-based ANT design in an ANT multiplier. The fixed-width designs are usually applied in DSP applications to avoid infinite growth of bit width. Cutting off n-bit least significant bit (LSB) output is a popular solution to construct a fixed-width DSP with *n*-bit input and n-bit output. The hardware complexity and power consumption of a fixed-width DSP is usually about half of the full-length one. However, truncation of LSB part results in rounding error, which needs to be compensated precisely. It is used to reduce the truncation error with constant correction value or with variable correction value . The circuit complexity to compensate with constant corrected value can be simpler than that of variable correction value; however, the variable correction approaches are usually more precise.

IV.MAIN BLOCK

The main block which consisting of multiplier. In the existing ANT multiplier design consist of the Baugh-Wooley multiplier. It has the normal design of half adders and full adders. Baugh-Wooley Multiplier is a high speed multiplier using the shift and adds method. This parallel multiplier uses lesser adders and minimum iterative steps. But in the proposed multiplier design is uses the Wallace tree multiplier. That is also having its own regular structure. It even reduces the amount of full adders and

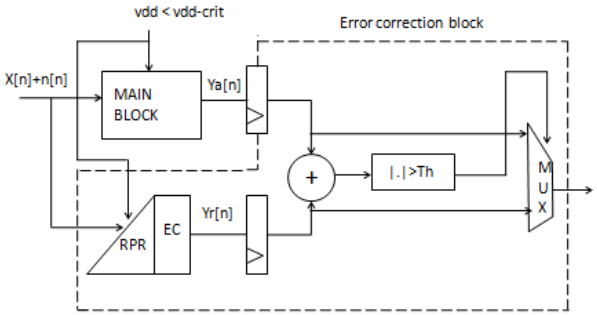

Fig.2 ANT Architecture with Fixed Width RPR.

half adders used. Wallace tree multiplier consists of three step process, in the first step, the bit product terms are formed after the multiplication of the bits of multiplicands and multipliers, in second step, the bit product matrix is minimized to lower number of rows using half and full adders, this process will follows till the last addition remains, in the final step, finally addition is done using adders to obtain the result.

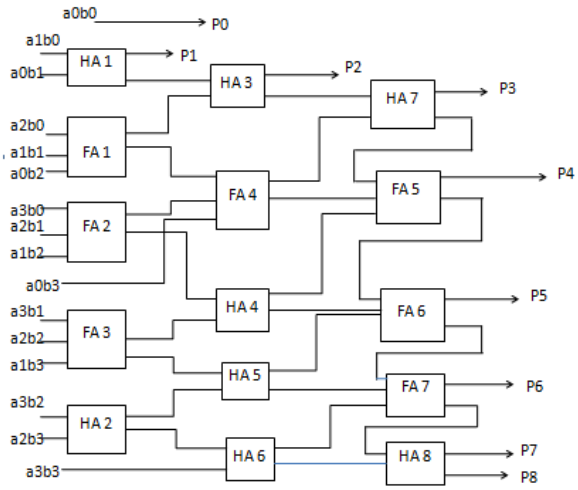

Fig.3 4x4 Bit Wallace Tree Multiplier

A. ERROR COMPENSATION CIRCUIT

The error compensation circuit which is combined with the RPR block. And the error which is not placed in the critical path. So, the error compensation will be easier one. However, under the VOS, once the critical path delay Tcp of the system becomes greater than the sampling period Tsamp, the soft errors will occur. In the ANT technique a replica of the MDSP but with reduced precision operands and shorter computation delay is used as EC block. In many high-speed digital signal processing (DSP) and multimedia applications, the multiplier plays a very important role because it dominates the chip power consumption and operation speed. Truncation error compensation techniques have been presented to design an error compensation circuit with less truncation error and less hardware overhead. The compensation methods can be divided into two categories: compensation with constant correction value and

compensation with variable correction value. Circuit complexity to compensate with constant corrected value can be simpler than that of variable correction value; however, the variable correction approaches usually can be more precise.

B.REDUCED PRECISION REDUNDANCY(RPR)

A MDSP system incorporating RPR . The MDSP block is subject to VOS, which results in soft errors in its output $y_a[n]$. When a soft error in MDSP is detected using an error control (EC) block, the RPR output $y_r[n]$ is used as an output estimate ŷ[n]. Both the outputs [Ya[n] and Yr[n]] of main block and the RPR block output are sent by using two Flip flops. In order to get the output from the flip flops we have a multiplexer. The two inputs are from the main block Ya[n] and the RPR block Yr[n]. The selection line which is used to the formula in equation (2).

C. REDUCED PRECISION REDUNDANCY FOR FIR FILTERS

Two main types of digital filters are commonly used in signal processing applications, Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters. FIR filters are purely feed-forward and show good stability and numerical properties while IIR filters include feedback paths that can lead to numerical problems when finite precision is used. The technique proposed for Finite Impulse Response (FIR) filters is the use of reduced precision replicas to detect and correct errors. This approach significantly reduces the overhead required for protection. The use of reduced precision in FIR filters is straightforward as they do not have feedback paths.

VI. ERROR COMMPENSATION VECTOR FOR FIXED-WIDTH RPR DESIGN

In the ANT design, the function of RPR is to correct the errors occurring in the output of MDSP. In the case of using fixed-width RPR to realize ANT architecture, we need to compensate huge truncation error due to cutting off many hardware elements in the LSB part of MDSP. In the MDSP of *n*-bit ANT Baugh–Wooley array multiplier, its two n-bit numbers, multiplier (A) and multiplicand (B), to be multiplied. A and B can be represented as

$$A = -a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i\, 2^i \quad \rightarrow (1)$$

$$B = -b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i\, 2^i \quad \rightarrow (2)$$

Where the a_i's and b_i are the bits in A and B, respectively, and an-1 and bn-1 are the sign bits. The product, P = A x B, is given by the equation:

$$P = AXB = \left(-a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i\, 2^i\right) x \left(-b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i\, 2^i\right)$$

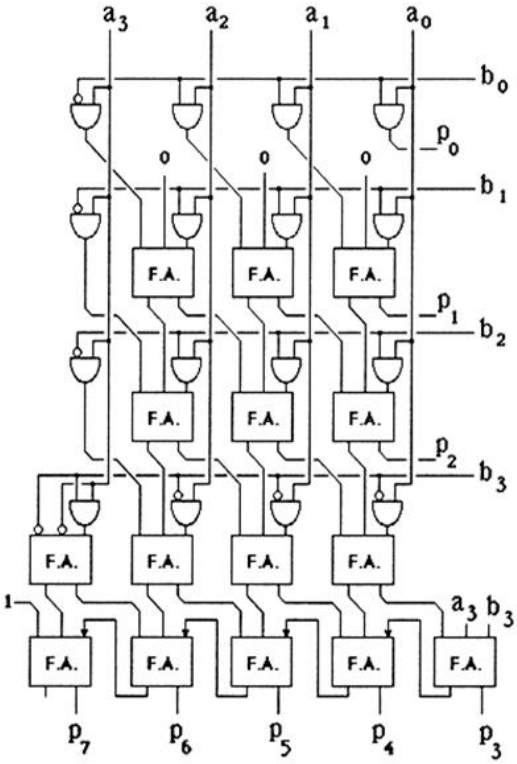

Fig.3 4x4 Baugh-Wooley Multiplier

The fixed-width Baugh–Wooley partial product array can be divided into four subsets, which are most significant part (MSP), input correction vector [ICV(*β*)], minor ICV [MICV(*α*)], and LSP. In the fixed-width RPR, only MSP part is kept and the other parts are removed. Therefore, the other three parts of ICV(*β*), MICV(*α*), and LSP are called as truncated part. The truncated ICV(*β*) and MICV(*α*) are the most important parts because of their highest weighting. Therefore, the Redundancies are removed by removing the truncated errors. So as to remove the replica at the MDSP output. The architecture of the Proposed RPR is sleeved to half where entire ANT architectural area is cut to down, they can be applied to construct the truncation error compensation algorithm. P_t is the output of the fixed-width multiplier in RPR. P_t can be expressed as

$$P_t = \sum_{j=\frac{n}{2}+1}^{n-1} y_j\, 2^j \sum_{i=\frac{3n}{2}-j}^{n-1} x_i\, 2^i + f(ICV) + f(MICV)$$

$$P_t = \sum_{j=\frac{n}{2}+1}^{n-1} y_j 2^j \sum_{i=\frac{3n}{2}-j}^{n-1} x_i 2^i + f(EC)$$

where f(EC) is the error compensation function, f(ICV) is the error compensation function contributed by the input correction vector ICV(β), and f (MICV) is the error compensation function contributed by minor input correction vector MICV(α).

VII. SIMULATED RESULTS

The ANT architecture using baugh-wooley multiplier is simulated by xilinx and microwind software is shown in fig.4,fig.5,fig.6.Here the two inputs are A and B.

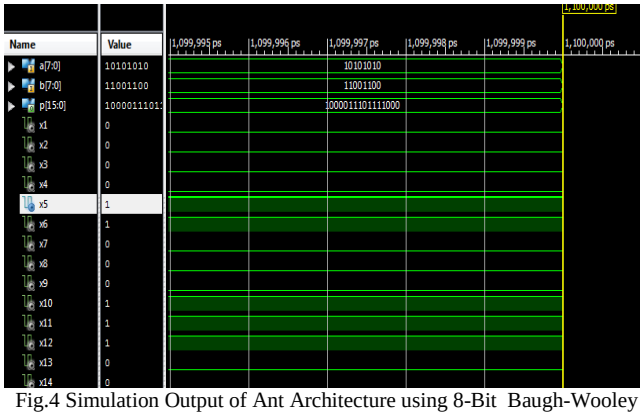

Fig.4 Simulation Output of Ant Architecture using 8-Bit Baugh-Wooley Multiplier

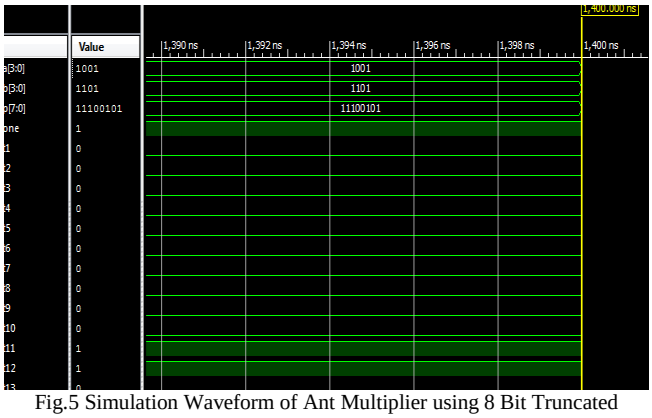

Fig.5 Simulation Waveform of Ant Multiplier using 8 Bit Truncated Baugh-Wooley Multiplier

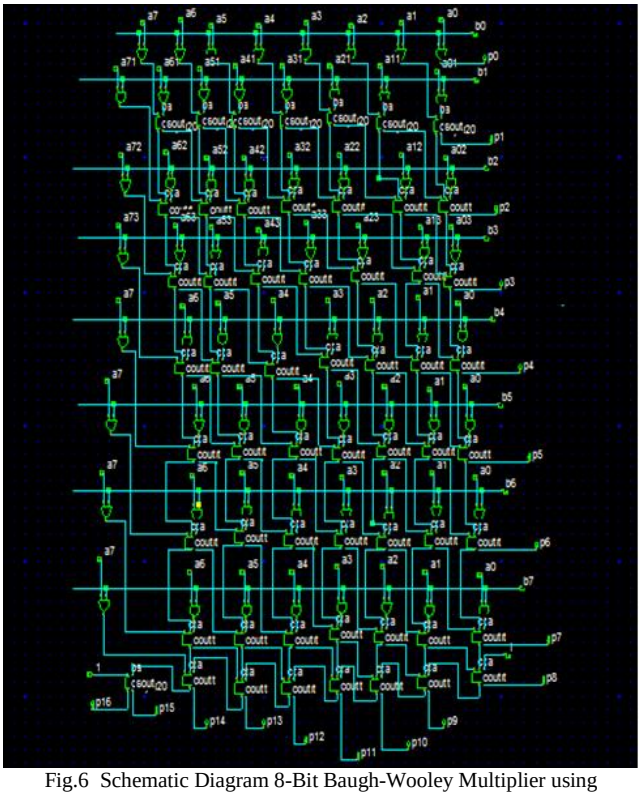

Fig.6 Schematic Diagram 8-Bit Baugh-Wooley Multiplier using Microwind

The ANT architecture using wallace tree multiplier is simulated by Xilinx and microwind software is shown in fig.7,fig.8 and fig.9.

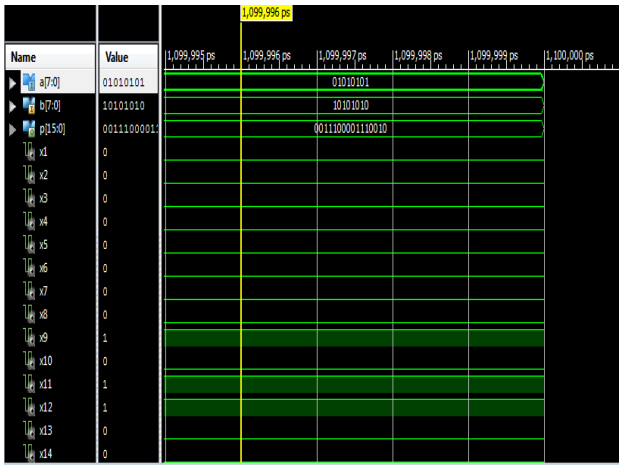

Fig.7 Simulation Output of ANT Architecture using 8 Bit Wallace Tree Multiplier

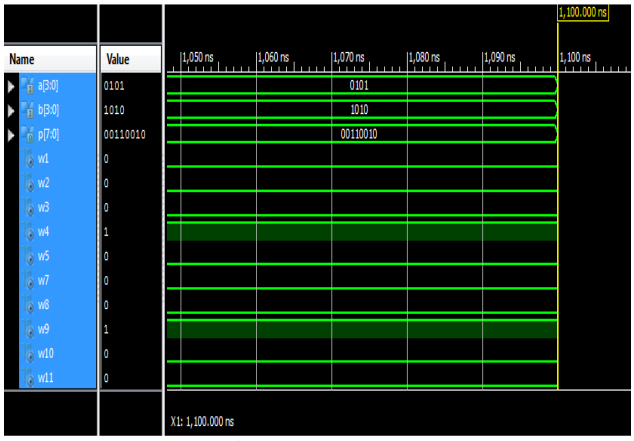

Fig.8 Simulation Waveform of Ant Multiplier using 8 Bit Truncated Wallace Tree Multiplier

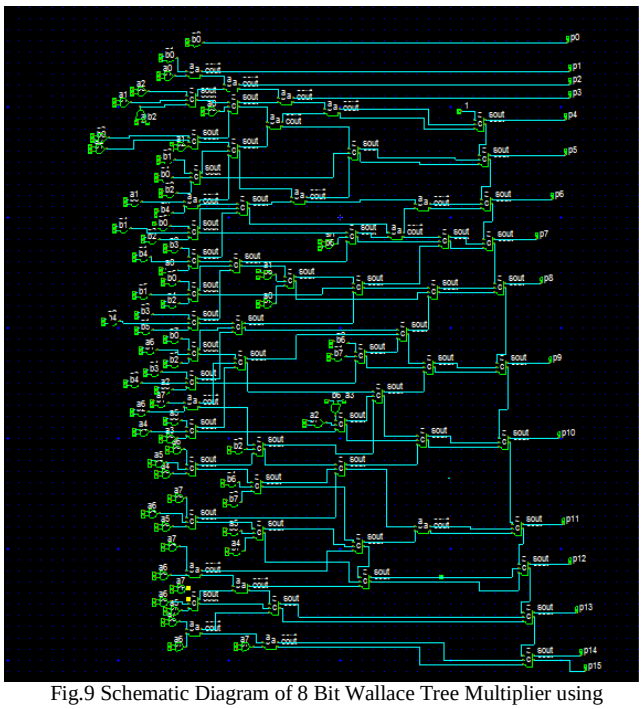

Fig.9 Schematic Diagram of 8 Bit Wallace Tree Multiplier using Microwind

The ANT architecture using second order FIR is simulated by Xilinx is shown in the fig.10.

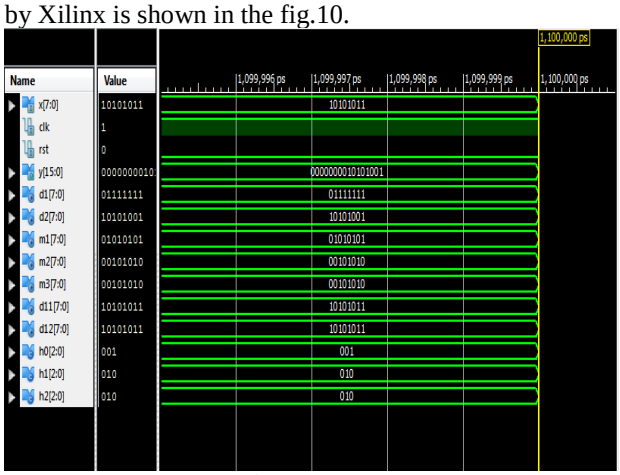

Fig.10 Simulation Output of ANT Architecture Using Second Order FIR Filter.

VIII. CONCLUSION

In this paper, a novel algorithmic noise tolerant fixed-width RPR multiplier design is presented. The proposed system uses 8 bit baugh-wooley multiplier and 8 bit wallace tree multiplier is implemented by using xilinx. It has 1V supply voltage and power consumption can be saved by 25% by using Fixed-width RPR based ANT architecture with Wallace tree multiplier circuit even reduce the amount of power and time. Using error compensation block in Fixed-Width RPR ANT multiplier, Baugh-Wooley Multiplier and Wallace Tree Multiplier power consumption is saved by 18%. and has lower product error than that of a fixed-width multiplier and still maintains low complexity .The use of Reduced Precision Redundancy for Finite Impulse Response (FIR) filters has been considered. A technique to avoid error propagation in the feedback path and numerical issues due to reduced precision in the replicas has been proposed.

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