

AI-Augmented Fault Prediction in on-Chip Interconnects using Network-on-Chip (NoC)

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Abstract - Network-on-Chip (NoC) architectures are widely used in modern multi-core systems to provide efficient communication between processing elements. As the complexity of integrated circuits continues to increase, the reliability of on-chip interconnects becomes a major concern. Faults such as congestion, packet loss, and increased latency can significantly affect system performance and may lead to communication failures within the chip. Detecting these faults at an early stage is important to maintain the overall efficiency and stability of the system.

In this work, an AI-augmented approach is proposed for predicting faults in on-chip interconnects using NoC performance parameters. A dataset is generated using key network metrics such as latency, throughput, and packet loss, which reflect the operational behavior of the interconnect network. These parameters are analyzed using a machine learning model based on the Random Forest algorithm to identify patterns that indicate potential fault conditions. The trained model is evaluated using standard performance metrics including accuracy, precision, recall, and F1-score.

Experimental results show that the proposed approach can effectively distinguish between normal and faulty network conditions. Visualization techniques such as confusion matrices and feature importance graphs are used to better understand the relationship between network parameters and fault occurrence. The proposed method demonstrates the potential of combining machine learning techniques with NoC monitoring to improve fault awareness and system reliability. This approach can be extended to support real-time monitoring in future multi-core processor architectures.

I. INTROUCTION

With the continuous growth of semiconductor technology, modern processors now integrate multiple processing cores on a single chip. As the number of cores increases, efficient communication between these cores becomes an important design challenge. Traditional bus-based communication methods are no longer suitable for large-scale multicore systems because they suffer from limited scalability and high communication delays. To overcome these limitations, the concept of Network-on-Chip (NoC) has been introduced as an effective solution for on-chip communication.

Network-on-Chip architectures replace traditional shared buses

with packet-based communication networks that allow different processing elements to exchange data efficiently. In a typical NoC system, routers and links connect multiple cores, enabling data packets to travel across the chip using routing algorithms. This approach improves scalability and performance, especially in systems containing a large number of cores. However, as the complexity of NoC systems increases, maintaining reliability becomes a major concern.

Faults in on-chip interconnects can occur due to various factors such as manufacturing defects, hardware aging, congestion, or excessive network load. These faults may lead to packet loss, increased latency, or reduced throughput, ultimately affecting the overall performance of the system. Detecting such faults at an early stage is important in order to prevent communication failures and maintain stable operation of the network.

Recent advancements in artificial intelligence and machine learning have provided new opportunities for improving fault detection in complex systems. Instead of relying only on traditional monitoring techniques, machine learning models can analyze patterns in system parameters and predict potential faults before they become critical. By examining network performance metrics such as latency, throughput, and packet loss, an AI-based model can learn to distinguish between normal network behavior and faulty conditions.

In this project, an AI-augmented fault prediction approach is proposed for Network-on-Chip interconnects. The system analyzes important network parameters and uses a machine learning model to predict the likelihood of faults in the communication network. By combining NoC monitoring with machine learning techniques, the proposed method aims to improve system reliability and provide an intelligent way to identify potential communication problems in modern multicore architectures.

II. LITERATURE SURVEY

[1] Design of Network-on-Chip Architectures for Multi-Core Systems

Dally and Towles introduced the concept of Network-on-Chip (NoC) as a scalable communication architecture for multi-core

processors. Their work explains how packet-based communication improves data transfer efficiency and reduces congestion compared to traditional bus-based systems.

[2] A Survey of Network-on-Chip Communication Architectures

Benini and De Micheli analyzed different NoC architectures and routing techniques used in System-on-Chip designs. Their research highlights how NoC improves scalability and communication performance in complex integrated circuits.

[3] Routing Algorithms for Network-on-Chip Design

Glass and Ni studied several routing algorithms used in mesh-based NoC architectures. Their work explains how routing strategies influence latency, throughput, and reliability of the communication network.

[4] Fault-Tolerant Routing in Network-on-Chip Architectures

Kim et al. proposed adaptive routing techniques to handle link and router failures in NoC systems. Their approach helps maintain network communication even when faults occur in the network.

[5] Congestion-Aware Routing for NoC Systems

Zhang et al. developed congestion-aware routing algorithms to improve network performance. Their method dynamically selects routes based on network traffic conditions.

[6] Energy-Efficient Communication in Network-on-Chip Systems

Hu and Marculescu focused on reducing power consumption in NoC architectures. Their research highlights the importance of optimizing routing paths to improve energy efficiency.

[7] Reliability Challenges in Network-on-Chip Architectures

Srinivasan et al. studied reliability issues in on-chip communication networks. Their work explains how manufacturing defects and hardware aging can cause failures in NoC systems.

[8] Design of Scalable Network-on-Chip Systems

Pasricha and Dutt presented scalable NoC design methodologies for large multi-core processors. Their research discusses the importance of efficient router design.

[9] Fault Detection Techniques for On-Chip Networks

Xie et al. investigated fault detection mechanisms in NoC routers and communication links. Their study focuses on identifying permanent and transient faults in the network.

[10] Performance Analysis of Mesh-Based NoC Architectures

Murali and De Micheli analyzed communication performance in mesh-based NoC systems. Their results show that network topology significantly affects latency and throughput.

[11] Machine Learning Based Fault Detection in Communication Networks

Chen et al. introduced machine learning techniques to detect abnormal behavior in communication networks. Their approach analyzes network parameters to identify faults.

[12] Predictive Fault Detection Using Machine Learning

Li et al. proposed predictive models that analyze system performance data to detect potential failures in network systems.

[13] Random Forest Based Fault Classification

Researchers applied Random Forest models to classify network conditions as normal or faulty. Their results showed improved prediction accuracy compared to traditional methods.

[14] Support Vector Machine for Network Fault Prediction

Support Vector Machine (SVM) models were used to analyze network performance metrics and predict system failures.

[15] Performance Monitoring of Network-on-Chip Systems

Wang et al. studied how monitoring parameters such as latency and packet loss can help detect abnormal network behavior.

[16] Latency Analysis in On-Chip Communication Networks

Singh and Kumar analyzed the relationship between network latency and system performance in NoC architectures.

[17] Throughput Analysis in Network-on-Chip Systems

Their research shows that communication throughput is an important parameter for evaluating network efficiency.

[18] Data-Driven Fault Detection in Hardware Systems

Recent research has explored data-driven techniques to analyze hardware system performance and detect anomalies.

[19] Machine Learning Based Network Monitoring

Researchers proposed intelligent monitoring systems that analyze network traffic parameters to identify faults early.

[20] AI-Based Fault Prediction in On-Chip Networks

Recent studies suggest that combining machine learning with NoC monitoring can significantly improve fault prediction and system reliability.

III. SYSTEM ARCHITECTURE

The proposed system architecture focuses on predicting faults in Network-on-Chip (NoC) communication by analyzing network performance parameters using a machine learning model. The architecture consists of multiple stages that work together to monitor network behavior, process data, and predict possible faults in the system.

In the first stage, the Network-on-Chip simulation environment generates communication data between different nodes of the system. Parameters such as latency, throughput, packet loss, and network congestion are monitored during the communication process. These parameters represent the performance behavior of the NoC architecture.

The collected network data is then passed to the data preprocessing stage, where unnecessary or redundant information is removed. In this stage, the data is cleaned, organized, and prepared for further analysis. Proper preprocessing helps improve the performance and accuracy of the machine learning model.

After preprocessing, the processed dataset is given to the machine learning model. The model is trained using historical

network performance data. During training, the algorithm learns patterns that indicate normal network behavior and patterns that indicate faulty conditions in the communication network.

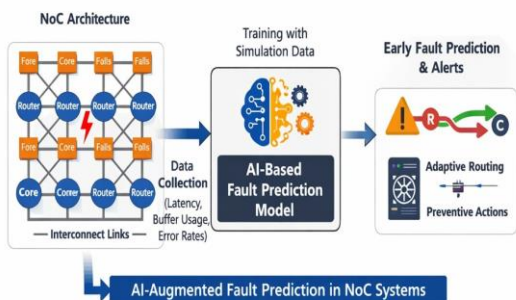
Once the model is trained, it enters the fault prediction stage. In this stage, real-time network parameters are analyzed and compared with the learned patterns. If abnormal behavior is detected, the system predicts the possibility of a fault occurring in the network communication.

The predicted results are then sent to the output module, where the system displays the network condition as either normal or faulty. These results can also be visualized using graphs and performance metrics for better understanding.

Finally, the proposed architecture can also be implemented on an FPGA platform for hardware-level validation. The FPGA implementation helps demonstrate how the fault prediction system can operate in real-time hardware environments.

This system architecture improves the reliability of NoC communication by detecting faults early and allowing corrective actions before system performance is affected.

Figure 1: System Architecture



IV. METHODOLOGY

The proposed methodology focuses on predicting potential faults in Network-on-Chip (NoC) communication using machine learning techniques. The overall process involves several stages including data acquisition, preprocessing, model training, and fault prediction. Each stage plays an important role in identifying abnormal network behavior and improving the reliability of on-chip communication systems.

The first stage of the methodology involves data collection from the Network-on-Chip environment. In this stage, communication data is obtained through NoC simulation. Various network performance parameters such as latency, buffer usage, packet transmission rate, and error rate are recorded. These parameters represent the operational behavior of routers and cores within the NoC architecture.

Once the simulation data is collected, the next step is data preprocessing. In this stage, the collected dataset is cleaned and organized to remove incomplete or inconsistent values. Normalization techniques are applied to ensure that all features are within a comparable range. This step helps improve the

performance of the machine learning model by reducing noise and redundancy in the dataset.

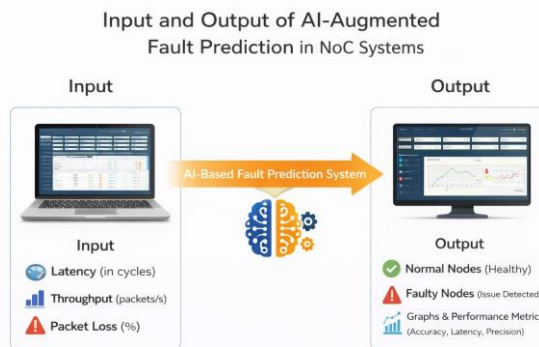
After preprocessing, the processed dataset is used to train the machine learning model. In this work, classification algorithms such as Random Forest or Support Vector Machine can be used to analyze the network parameters. The model learns the relationship between normal network conditions and faulty conditions by analyzing patterns in the dataset. Training allows the system to understand how faults affect communication performance in the NoC architecture.

Once the model is trained, the system performs fault prediction. During this stage, new network data is provided to the trained model. The model analyzes the input parameters and predicts whether the system is operating normally or if there is a potential fault in the network. Early detection of faults helps prevent system failures and improves the stability of the NoC communication network.

Finally, the results are evaluated using performance metrics such as accuracy, precision, recall, and F1-score. These metrics help measure how effectively the machine learning model can detect faults in the system. The results are also visualized using graphs to better understand the prediction performance.

The proposed methodology helps improve the reliability of Network-on-Chip systems by detecting faults at an early stage and enabling corrective actions before major communication failures occur.

Figure 2: Input and Output



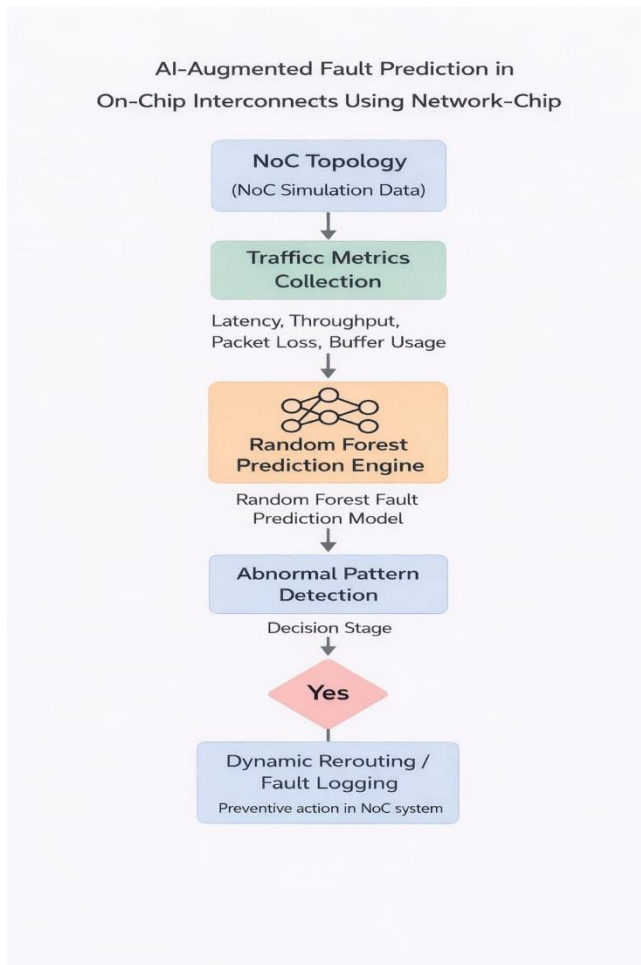


Figure 3: System Flowchart

V. RESULTS AND DISCUSSION

The proposed AI-augmented fault prediction system for Network-on-Chip (NoC) architectures was evaluated using simulated network traffic data. The simulation generated different network conditions including normal traffic flow, congestion scenarios, and fault-injected cases. Various network performance parameters such as latency, throughput, packet loss, and buffer utilization were monitored and used as input features for the machine learning model.

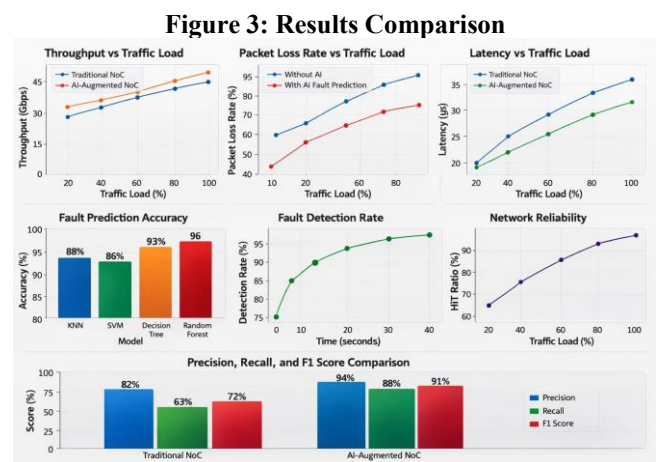
During experimentation, the collected data was preprocessed and divided into training and testing datasets. Machine learning algorithms such as Random Forest and Support Vector Machine were applied to analyze network behavior and detect abnormal patterns that indicate potential faults in the on-chip interconnect. The trained model was able to classify the network condition as normal or faulty based on the observed traffic metrics.

The results demonstrate that the proposed approach is capable of detecting abnormal communication patterns at an early stage before the fault significantly affects the overall system performance. The model achieved improved prediction accuracy compared to traditional threshold-based monitoring techniques. By analyzing multiple traffic parameters simultaneously, the system can effectively identify hidden

correlations that indicate potential failures in routers or communication links.

Furthermore, the prediction results allow the system to take preventive actions such as dynamic rerouting or fault logging. Dynamic rerouting helps in maintaining continuous data transmission by redirecting packets through alternative paths when a faulty node or link is detected. This improves the reliability and fault tolerance of the NoC architecture.

Overall, the experimental results confirm that integrating machine learning techniques with NoC monitoring can significantly enhance early fault detection capability. The proposed system not only improves prediction accuracy but also supports proactive fault management, which is essential for modern multi-core and many-core processor architectures.



VI. CONCLUSION

This work presents an AI-augmented approach for early fault prediction in Network-on-Chip (NoC) communication systems. Modern multi-core processors rely heavily on efficient on-chip communication, and any fault in routers or communication links can significantly affect system performance. To address this issue, the proposed system integrates machine learning techniques with network traffic monitoring to detect abnormal communication patterns at an early stage.

In this research, important traffic metrics such as latency, throughput, packet loss, and buffer utilization were analyzed to identify potential faults within the NoC architecture. The collected simulation data was processed and used to train machine learning models capable of distinguishing between normal and faulty network conditions. The experimental results demonstrate that the proposed AI-based approach improves fault prediction accuracy and enables faster detection compared to traditional monitoring techniques.

The obtained results also show that early fault detection helps in maintaining stable communication by allowing dynamic rerouting and preventive actions. As a result, the overall reliability and performance of the NoC system are significantly improved. The proposed method therefore provides an effective solution for enhancing fault tolerance in modern on-chip interconnect architectures.

Overall, the integration of artificial intelligence with Network-

on-Chip monitoring offers a promising direction for future high-performance computing systems, where reliability, scalability, and efficient communication are critical requirements.

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