Advanced Wireless Communication Technologies for low Power, Reconfigurable Small Satellite Radios

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***Abstract*: Wireless communication plays a significant role in day to day life. Besides communication ,Wireless technology has become an integral part of our daily activities . The Transmission of data or information from one place to another. This provides an exchange of data without any conductor through RF and radio signals. Advances insmart antennas ,coding theory power amplifiers, low power electronics and software defined radios have dramatically impacted terrestrial communications Alsothe shorter life times and higher levels acceptable risk typical of small satellite missions make the utilization of advanced commercial-off-the-shelf(COTS)components feasible. This Paper describes an effort underway to study flexible radio architectures that can rapidly leverage emerging wireless technologies for small satellite communictions. Advances in low power high rate signal conversion and signal processing circuits are also being exploited to boost capabilities while minimizing the associated dissipated power.**

Keywords: Wireless communication, reconfigurable small satellite radios, low power consumption.

I.INTRODUCTION

Large economic markets propel technological innovation. Smaller players can benefit greatly when the developments made by these driving forces also happen to meet their needs. The small satellite community has the opportunity to ride the research-and-development coattails of the mammoth terrestrial wireless communications industry. Due in large part to the efforts of this industry, the performance of low-voltage, low-power circuits is advancing rapidly. Solutions posed to mitigate terrestrial radio-spectrum congestion and improve link performance also have potential to benefit small-satellite systems. Software-defined radios are being used to reduce nonrecurring development costs and time-to-market for new consumer product derivatives. This technology can have similarly positive impacts on small-satellite communications systems.

This paper will discuss an effort underway to study flexible radio architectures that can rapidly leverage emerging wireless technologies for small satellite applications. A modular design approach is emphasized to allow incremental hardware advances to be incorporated into the radio without a complete redesign. It will also make it possible to customize aproduct rapidly to meet demanding specifications that cannot be met by any available radios. Finally, utilizing a software-defined radio paradigm will result in radios that can be rapidly programmed to communicate with a wide range of different networks, use the latest signal processing techniques, and avoid obsolescence with regular software upgrades.

A.Responsive Space Programs

The concept of responsive space emphasizes reduced development time and rapid deployment of an asset to meet a time-critical need. Many of the defining characteristics of a responsive satellite program are important for any small satellite. In many cases, a small, dedicated satellite is chosen to reduce cost and risk. As long as the *a priori* development that is required is not too costly, a communications subsystem that meets the needs of a responsive space program will be inherently beneficial to any small satellite program.

The desired level of responsiveness—the breadth of the range of requirements and the speed with which they can be met—correlates directly to the amount of development that must be done in advance. Being prepared to meet a more diverse collection of possible missions will require a larger budget. This additional cost may be acceptable for the case of the responsive space mission—it is the price paid for the rapid deployment capability—but the business case is less forgiving for traditional small satellites. Programs and vendors can rarely afford to engage in preemptive development, although some are able to leverage extensive collections of heritage designs intended for use on small satellites.

B.Proposed Solution

In a resource-constrained environment with a reasonable amount of development time available, the ideal communications subsystem solution will likely lie somewhere between a highly integrated, well-optimized custom design and a cash-and-carry off-the-shelf radio.Providing a higher degree of customization and integration, while costly, leads to a smaller, lighter, more power-efficient design. Likewise, being responsive to a wider range of possible requirements impacts cost, especially when these requirements are each met with custom designs.

There are some important practical issues that must be considered with respect to licensing a series of derivative products with national and international regulatory agencies. Due to these constraints, general-purpose off-the-shelf radios will always be important to low-cost satellite programs. For programs with communications system requirements that cannot be met with an existing radio, however, a modular approach allows the latest technological advances to be integrated alongside hardware with proven flight heritage.

II. PLATFORM-BASED DESIGN APPROACH

Several groups have proposed or implemented a modular, platform-based approach to designing and building spacecraft[1], small satellites[2,3], and small satellite communications subsystems[4-6]. The potential for cost savings that may be obtained using this approach is discussed in the literature.

A.System-level Design

USU/SDL is currently studying a small satellite platform architecture to look at the merits of this approach.Finally the set of all variants derived from a platform is a product family.Product platforms may actually support a fair amount of customization through the ability to produce large numbers of product variants to target many different market segments and obtain a market advantage.platforms can also substantially reduce manufacturing and development costs and time. Automobile companies routinely use one basic platform across a range of automobile types and product lines.Several factors make satellite designs different than other products. First, small numbers of completed systems are made, compared to the large number of units made for most consumer products. Second, there may be a significant lag time between production of these small number of units such that technology improvements can outpace the next build.

For many in the spacecraft industry, lack of product volume or rate serves as justification to accept higher manufacturing costs. Thus spacecraft remain larger “craftsmen endeavors” rather than applying the latest manufacturing innovations. However, the advanced manufacturing processes could revolutionize custom manufacturing, making even the manufacturing of a small number of units cost-effective. By taking the time to develop an effective manufacturing process plan needed for creating a well-designed small satellite platform, variants on that platform can be easily programmed and fabricated.

USU is currently developing a set architecture of representative future small satellite missions, a platform that encompasses the vast majority of future missions, and the supported family variants to satisfy the requirements of these missions. An architecture-level comparison of the resultant product family with the traditional custom design solutions for each mission type will be completed both technically and economically.

To perform this product family versus custom design comparison, a conceptual systems design model for small satellites is being used. This systems modeling for conceptual satellite design is a well-established approach used by one of the authors as well as many others at The Aerospace Corporation and NASA JPL. Integrating optimization into a conceptual small satellite design and cost model will be explored during this study.

Using this model, a custom individual design will be completed for each of several design reference missions. Then a platform based approach will be taken where design choices for each subsystem are made to decide what will be a part of the common platform and what will be a variant. For example, the type of attitude control may be varied across the mission classes from three-axis to spin stabilized to gravity gradient, but it may be decided that the platform structure should use a common approach and configuration. Various combinations of common and variant features will be explored to try to obtain the product family with the greatest cost savings. This design will be performed manually, but this may be an area where optimization may prove fruitful if time allows. Then at an architecture level the technical merits of the custom designs versus the product family can be compared. Figure 1 illustrates the process just described and reference 8 describes this work at USU further.

B.Communications Subsystem

Caffreyet al.[6] describe a platform of radios developed by AeroAstro to provide S-band and X-band communications. This reference demonstrates the sound business case for such an approach. The AeroAstro downlink transmitters offer programmable data rates and each has an optional external power amplifier to boost the output power, if desired. Their radios also provide optional attachments that allow for redundant interfaces to a range of IEEE-, industry-, and military-standard buses. The modular designs make a variety of options possible, giving them an opportunity to capture a larger market share. Surrey Satellite Technology Limited (SSTL) has successfully applied a similar approach to many of their subsystems for over a decade[3], establishing themselves as a dominant force in the small satellite industry. Also, a number of vendors have introduced software-defined radios intended for use on small satellites[9,10].The goal of this effort is to develop an architecture for a platform of radios that builds on the thesis proposed by Caffrey et al. but extends it further by

- taking the modularity to a lower level,
- incorporating a software-defined radio, and
- utilizing the low-level modules to incorporate additional technology developed for terrestrial wireless communications.

The first phase of this effort focuses on defining segmentation points and standardizing interfaces within the subsystem. This step is critical in that the architecture must allow for the rapid employment of emerging

hardware technologies, especially those for signal processors, low-power signal conversion and analog electronics, and high-efficiency power amplifiers. Next, we are identifying the types of waveforms, modulation and error-correction schemes, network interfaces, and other signal processing algorithms we would like our software-defined radio to support. Finally, we will expand our hardware testbed, designing, building, integrating, and testing many individual customized modules.

Currently, many of the radio components are implemented using laboratory test equipment and COTS hardware. The intent is to develop at least one of each of the following distinct modules:

- a signal processor with a high-precision reference oscillator and a phase-locked loop (PLL) for the master clock,
- an external interface,
- a signal converter, intermediate-frequency (IF) or in-phase and quadrature (I/Q) baseband,
- an optional IF up-/down-converter,
- a buffer/splitter/IF signal distributor,an RF tray interface,
- a low-noise amplifier/RF down-converter,
- an RF up-converter,
- a power amplifier,
- and an antenna interface utilizing a transmit/ receive switch, diplexer, and/or beamforming network.

Since a software-defined radio is able to communicate using a variety of protocols and physical- and data-link-layer standards, we plan to develop a selection of modules that will enable a demonstration of this capability.

III.ARCHITECTURAL CONSIDERATIONS

Practically speaking, a low-power software-defined radio can only take you as far as the intermediate-frequency regime. To operate in a given radio- or microwave -frequency band requires band-specific local oscillators, frequency translators, filters, amplifiers, diplexers, and beamforming networks. If solid-state switches implement a transmit/receive switch in a half-duplex radio or provide cross-strapping in applications requiring redundancy, they are typically band-specific, as well.

A block diagram for an example of a modular software-defined radio is shown in Figure 2. The various colors represent stand-alone modules. The interfaces between each of the modules are standardized, making it possible to update or exchange individual modules with an equivalent variant readily. Ideally, the footprints of each would also be standardized and all baseband and IF modules will be in a single enclosure. The only band-specific modules are the RF trays and a single software-defined radio will be capable of interfacing to several of these trays through the buffered splitter/combiner module.

A.Signal Processor

The signal processor module should be scalable to make the most of the trades between processing capability, power consumption, reliability, radiation tolerance, and cost. In some cases, the optimum solution may be to replace the radio's signal processor with an interface to the satellite's command and data handling (C&DH) processor, consolidating the "brains" of the satellite to a single unit. Whether this module is a tremendously powerful signal processor or merely a feedthrough, the various options should be easily interchangeable to minimize recurring cost and development time.

B.Signal Conversion Methodologies

We are investigating three candidate signal conversion methodologies for the software-defined radio: baseband conversion, standard digital up- and down-conversion, and higher-order Nyquist-zone sampling.

*Baseband.*In-phase and quadrature signals can begenerated and captured at baseband. Quadrature up - and down-converters are then required to get to and from the intermediate frequency. Typically a margin of $\geq 25\%$ is maintained, resulting in a minimum sampling rate that is 2.5 times the bandwidth of the signal of interest.

*Digital IF.*The signal processor performs digital up- and down-conversion, usually at a relatively low intermediate frequency. Further, it eliminates the need to tune the quadrature up-converter for carrier suppression on the transmit side. The primary drawback is the increase in power dissipation in the signal processor and digital-to-analog conversion circuits due to the

C.Redundancy and Fault Tolerance

For low-cost technology demonstration satellites, a single-string communications system lacking even the simplest fault detection mechanisms may be adequate. At the other extreme, satellites performing critical military or commercial functions require high levels of redundancy and thorough fault detection and mitigation capabilities.

Redundancy can be implemented in a modular radio by cross-strapping duplicate modules or strings of modules. For analog hardware, faults tend to come in two flavors, gradual degradation and catastrophic failure. They can be caused by radiation exposure, thermal cycling, or unexpected events such as an electrostatic discharge or being painted by a high-power emitter. Typically the only way to correct an analog fault is to switch to a redundant component, although in some cases recycling the power may be an adequate course of action. An amplifier oscillation set off by thermal conditions is an example of such a situation.

When a software-defined radio is used, digital faults become a particularly serious concern. Radiation-tolerant and radiation-hardened components are statistically less vulnerable, but in high reliability applications triple modular redundancy (TMR) is necessary.

Microprocessors can be used in TMR systems by utilizing three complete processors and voting on their outputs. Rad-hard memory is available for them with built-in TMR functionality. For severe radiation environments, programmable logic devices are often preferred because they allow TMR to be distributed throughout the logic, not just at a single output point. When a fault is detected in a microprocessor, the solution is generally to recycle and resynchronize the entire unit. In field-programmable gate arrays (FPGAs), algorithms and hardware have been developed for detecting and correcting single-eventeffects while the logic in the rest of the circuit runs undisturbed[11]. This reduces the down-time during which fault-correction is unavailable.

Microprocessors tend to be more power-efficient and make it easier to implement software for complex state machines. FPGAs offer advantages in implementing parallel algorithms and allow for low-level TMR. For these reasons, we are investigating signal processing module topologies that employ both microprocessors and programmable logic devices. A third alternative also under consideration is the instantiation of several microprocessors within one or more radiation-tolerant FPGAs. This would leverage standard software libraries and low-level TMR, bringing together the benefits of the two previously distinct options.

IV.RF TRAYS

The purpose of the RF tray is to implement all of the functions necessary to communicate in a given band with at least one and possibly multiple different networks. An example of what an RF tray might look like, with five customizable modules, is shown in Figure 3. Although only one of each module is indicated in the example, it is possible that some modules will have one or more alternate switchable variations in the same tray. The power amplifier, for example, might be switched between a high linearity class A design and a nonlinear, but dramatically more efficient, class E amplifier.

*Power amplifiers.*The power dissipation and thermaldesign of the radio are usually highly dependent on the performance of the power amplifier. This makes the power amplifier module one of the top contenders for customization. Narrowband designs are inherently easier to optimize for power efficiency and linearity. Using a generic power amplifier with significant excess bandwidth will therefore likely mean giving up performance in other areas. Also, for applications that allow for the use of a constant-envelope modulation scheme, or one with a peak-to-average ratio approaching unity, the opportunity to use a high-efficiency, nonlinear power amplifier may arise.

*Antenna interface.*Full-duplex operation is likely torequire a diplexer; the exception would be when separate, well-isolated antennas and robust pre-selection filtering are used for the transmit and receive functions. Two distinct local oscillators are also needed in this case. Half-duplex applications can get by with a transmit/receive switch and a single local oscillator in the RF tray. Full-duplex operation can also be achieved by utilizing two cross-strapped, redundant half-duplex trays.

Mechanical. Ideally, the RF tray is designed as a singlesegmented unit with a fixed footprint. This will simplify the spacecraft design, reduce the number of custom parts required, and ease the burden of integration, assembly, and test. The antenna interface module may vary in size from a single tiny solid-state switch to a bulky diplexer / beamforming network combination full of quarter-wave resonant structures. This complicates the mechanical design considerably. One solution under consideration is to provide a placeholder just large enough to accommodate transmit/receive and cross-strapping switches, then allow for attachment of additional bolt-on hardware as necessary.

*Electromagnetic compatibility.*Even though producingflight hardware is not a priority of this effort, segmented RF tray enclosures will be built and nominal sets of components will be integrated therein. This will provide excellent experience for our student engineers, allow us to experiment with a variety of packaging and assembly techniques, and validate the electromagnetic compatibility (EMC) performance of each.

V. CANDIDATE WIRELESS TECHNOLOGIES

A discussion of some of the wireless technologies that will be integrated into our modular radio testbed follows.

A.High-efficiency and High-linearity Power Amplifiers

For some applications, particularly those requiring high bandwidth efficiency, a highly linear power amplifier is necessary. For example, a 256 -QAM downlink contains 8 information bits per symbol of data, a 4x improvement over a QPSK link. A 256-QAM signal constellation has 32 distinct symbol power levels, corresponding to a peak-to-average power ratio of 4.2 dB if rectangular pulses are assumed. The dynamic range of the signal envelope is 23.5 dB. Amplifier nonlinearities cause symbols associated with small power levels to be amplified with a different (usually larger) gain than symbols associated with higher power levels. A high linearity power amplifier must be used to prevent severe signal distortion (with accompanying spectral regrowth) and degradation of the bit-error rate. Linearity is achieved by employing linearization techniques or by backing off the level of the output signal with respect to the 1 dB gain compression point of the power amplifier.

For the example of 256-QAM, the required backoff margin is typically around 15 dB if no other linearization is applied. Assuming a class A amplifier with an ideal efficiency of 50% as the baseline, a 15 dB backoff implies a *maximum* efficiency of 1.6%. This number is unacceptably low for a small satellite and some form of linearization is necessary for a high-dynamic-range modulation scheme to be feasible. It is also important to note that bandwidth efficiency comes at a cost of bit-error-rate performance. Power consumption therefore increases substantially when the drop in power amplifier efficiency

is combined with the need to deliver more transmit power to maintain a given specified bit-error rate.

For constant-envelope modulation schemes such as Gaussian minimum- shift keying (GMSK), theoretically the peak-to-average power ratio of the waveform approaches unity when it leaves the modulator. As the signal is passed through subsequent components, additional filtering caused by the frequency response of amplifiers, mixers, and filters will impact the signal. The typical increase in peak-to-average ratio is on the order of 1 dB, resulting in a signal envelope with a limited dynamic range that is still well suited for amplification by a high-efficiency nonlinear amplifier.

Due to the sizeable market for low-power wireless handsets and the desire to extend battery life, tremendous investments have been made in developing low-voltage high-efficiency power amplifiers. The majority of the world has adopted the Global System for Mobile Communications (GSM) as their standard for personal wireless communications. Utilizing a GMSK modulation scheme, GSM handsets are well-suited for nonlinear high-efficiency power amplifiers. Significant advances have been made in this arena due to improvements in both semiconductor devices and low-loss lumped elements required to realize these circuits. Small satellite radios can clearly benefit from this technology.In the United States, code-division-multiple-access (CDMA) techniques are prevalent in wireless telephony. CDMA waveforms have high peak-to-average ratios. As a result, large investments have been made in signal processing (e.g. predistortion), feed-forward, and feed-back techniques for amplifier linearization. Linearization is helpful in improving the performance of radios designed to interface with existing ground systems that use common variable-envelope waveforms or multi-carrier signals. These techniques may also make it feasible to use bandwidth-efficient modulation schemes on small satellites, particularly during periods when significant link margin is available such as in the case of a direct overhead pass. The ability to adapt to changing link conditions and spectrum availability is often referred to as cognitive radio[12]. Due to the high cost of licensing radio spectrum, cognitive radio has major market forces pushing for its development.

B.Signal Conversion Circuits

Many familiar electronic devices have “gone digital,” replacing a portion of the bulky and expensive precision analog hardware inside the device with its digital equivalent. This is accomplished by adding or perhaps moving, if the device already contained one, an analog-to-digital converter (ADC) and/or a digital-to -analog converter (DAC). Some of these devices are low-power, battery-operated, and relatively narrowband like wireless handsets and laptop WiFi local-area-network cards. Others, high-frequency test equipment, for example, must handle extremely wideband signals but do not face the challenging size and power limitations imposed on handheld consumer electronics.

Signal conversion circuits are emerging that run at higher sampling rates, offer greater precision, consume less power, and come in smaller packages. ADCs range from the relatively slow but high precision successive approximation and sigma-delta ADCs to the power-hungry flash and time-interleaving circuits that exchange lower resolution for higher conversion rates.An analogous range of DAC circuits are available, as well as direct digital synthesizers and digital up- and down-converters. Many of these components are equipped with a shutdown mode. Maintaining a separate signal conversion module will make it possible to rapidly take advantage of new mixed signal circuits as they enter the market and allow for customization based on the trade between required bandwidth and power dissipation.

C.Digital Signal Processors and FPGAs

CMOS devices are shrinking and the power supply voltages used to bias them are dropping. As a result, the power dissipated by each device is being reduced. Although FPGAs were once considered terribly power-inefficient, improvements such as the ability to effectively power down unused portions of the device are helping to change this image. The high percentage of transistors in an FPGA that are used for routing and configuration functions will always make them less power-efficient than digital signal processors (DSPs), but their power dissipation is low enough to make it feasible to use them in some power-constrained applications.

Both DSPs and FPGAs are becoming more capable and power efficient on a per-operation basis. New circuits offer features such as clock stepping to minimize power consumption when it is feasible to do so. Small satellites will be able to derive more and more signal processing capability from the limited power that is available to them as this evolution continues. It is essential to develop a radio architecture that allows these components to be integrated rapidly.

Smart Antennas

Unlike their larger relatives, small satellites cannot generally afford the luxury of a highly directional, gimballed antenna. As downlink data rates increase, the acceptability of using a low-directivity space segment antenna diminishes rapidly. It is also possible that in the future, the interference environment may preclude the use of a space-segment antenna with an excessively wide beam-width on both the uplink and the downlink.

It is operationally difficult to rely on a spacecraft’s attitude control system to maintain antenna pointing for a fixed-beam antenna. A better solution is to use an array of low-directivity elements and electronically steer the beam. Smart antennas are generally defined as an array of antenna elements combined with signal processing in both space and time. On the receive side, adaptive processing can be used to perform spatial filtering to mitigate interference and improve capacity. This may be particularly beneficial for small satellites tasked with two-way communications

missions. To this end, the Iridium satellites use an antenna array with 48 fixed beams on each satellite[13]. Signal-source geolocation is another capability available to a receiver equipped with a smart antenna.

D.Iterative Error-correction Techniques

Small satellite radios can potentially benefit greatly by employing iterative error-correction techniques. Twocommon iterative error-correction schemes, turbo codes[14,15] and low-density parity-check (LDPC) codes[16,17], both offer relatively low implementation

complexities on the encoding side. Since their decoders require significant computational resources, they are well suited for small-satellite downlinks, leaving the majority of the computational burden to be born by the ground terminal.

With each passing iteration in the decoding process, the error rate converges rapidly on its lower bound. However, each turbo decoder iteration requires substantially more operations than its LDPC counterpart. Both Turbo and LDPC codes

- are typically implemented using rate-1/2 codes,
- need exacting carrier and clock synchronization,
- require block lengths tens of thousands of symbols or longer to be effective, and
- can result in 5 to 9 dB of coding gain (near Shannon-bound capacity), depending on the implementation.

Although rate-1/2 codes are the most commonly discussed in the literature, the code rate is in fact flexible. Also, to achieve capacity near the Shannon bound requires very long block lengths, possibly on the order of one million symbols.

It is tempting to immediately assume that the transmit power can be reduced by the amount of coding gain. Unfortunately, as the signal- to-noise ratio (SNR) of the received signal drops below about 5 dB, traditional phase-locked carrier tracking loops begin to performpoorly and symbol synchronization becomes extremely difficult. Iterative synchronization methods may be employed to counter this effect, but there is a practical limit to how low the received SNR can go. On the positive side: it is possible that an increase in the complexity of the ground-station receiver can be exchanged for *some*reduction in the downlink transmit power while the remaining coding gain is used to reduce the received bit-error rate.

VI. CONCLUSIONS

Due to investment by and research for the wireless telecommunications industry, there are a wide range of emerging technologies which have potential to help mitigate some of the challenges facing small-satellite communications engineers. We are working to develop innovative radio architectures that make it possible to rapidly and economically bring these new technologies to bear. Our modular hardware testbed gives us the capability to evaluate a components such as signal conversion circuits, digital signal processors, FPGAs, and both high-efficiency and high-linearity power amplifiers. Employing the software-defined radio paradigm makes the testbed flexible and provides a means of utilizing advanced signal processing techniques.Developing flight hardware is not an immediate priority, however, some of the related design challenges are being addressed. Graduate research assistants are gaining hands-on experience designing and linearizing power amplifiers, implementing and characterizing modems and microwave radio circuits, and working through challenging EMI/EMC problems. To bring similar practical experience to a wider audience, portions of the testbed will also be utilized in a number of Utah State University microwave engineering and satellite communications courses.

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