

# Advanced Low Power Design of Radix-2 FFT Architecture with Two Channel PISO Butterfly Input

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**Abstract—** In this project multiple independent FFT computation of two independent data stream is introduced. Multipath delay communicator FFT architecture is the basis of proposed architecture. In time FFT and in frequency FFT it has  $N/2$ -point decimation to process the odd and even samples of two data streams separately. The bit reversal operation is performed by the architecture itself is the main feature of the architecture. So without any dedicated bit reversal circuit the outputs are generated in normal order. By interleaving the data the bit reversal operation is performed by the shift registers in the FFT architecture. So high throughput and lower number of register is necessary for the proposed architecture. System throughput is a key factor influencing performance in wireless communication. To increase the transmission rate of the system key research is done.

## I. INTRODUCTION

FFT is most commonly used in wireless communication application. Single path delay feedback and multiple path delay commutator are very popular in a family of pipelined FFT architecture. More than one data stream need to be processed in applications such as image processing, multiple input-multiple output OFDM, and array signal processing and so on. In order to generate the outputs in natural order a dedicated bit reversal circuit and simultaneous multiple FFT operations are required. Multiple independent data streams can be handled by FFT architectures. A single FFT processor has the ability to process all the data streams. Four independent data streams are included], they are processed one by one. At two domains eight data streams are processed. When multiple data streams are processed the output is not achieved as parallel, so more than one FFT processors are used. One to four data streams are processed in wireless area network application by using multiple data path. The proposed architecture is designed to process parallel input data streams continuously with less amount of hardware. The odd and even inputs are in the natural order. The odd samples are processed by  $N/2$  point DIT FFT. The even samples are processed by  $N/2$  point DIF FFT. To generate the outputs of  $N$ -point FFT in natural order, two parallel butterflies processed the outputs of the two  $N/2$  point FFTs

## A. Objectives

FFT has a significant role in the digital signal processing. The FFT computations have high throughput and low latency. High performance FFT circuit must be design to achieve high throughput and latency. System throughput is a key factor influencing performance in wireless communication. To increase the transmission rate of the system key research is done. The proposed architecture is designed to process parallel input data streams continuously with less amount of hardware. The results of different architecture are compared with their area, power and delay.

## B. General Background

FFT is known as an efficient algorithm, used in DET&IDFT. There are different types of FFT algorithms, wide range of mathematics are involved in it. FFT is a special algorithm for speedier implementation DFT. A smaller number of arithmetic operation is required for FFT such as addition & multiplication. FFT has lesser computation time than DFT. In many fields of application in digital signal processing, FFT is an essential analytical tool. It is acting as a special tool in image processing application. For computing the DFT of a finite series FFT is a highly efficient procedure. For this less number of computation is required than that of the direct evaluation of DFT. The computation time of DFT is reduced with the help of the symmetry and periodicity of twiddle factor.

## II. EXISTING SYSTEM

### A. A Normal I/O Order Radix-2 Fft Architecture To Process Twin Data Streams For MIMO

It is designed to process parallel input data streams continuously. The odd and even inputs are in the natural order. The odd samples are processed by  $N/2$  point DIT FFT. The even samples are processed by  $N/2$  point DIF FFT. To generate the outputs of  $N$ -point FFT in natural order, two parallel butterflies processed the outputs of the two  $N/2$  point FFTs.

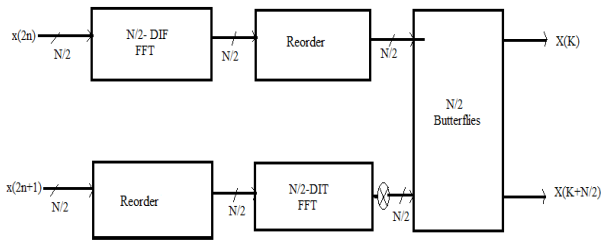


Fig.1. Block Diagram Of Conventional Method

The two  $N/2$ -point FFT operations with additional one stage of butterfly operations for computing an  $N$ -point FFT is shown in Fig.3.1, it provides the methodology but it is not the exact architecture. To process two data streams using two eight-point MDC FFT. The inputs are received by the RSR unit present at the left side of SW1. The last stage RSR is used store eight-point DIF FFT output and bits reverse them. Butterfly operations done by the bit reversed data in the RSR in the last stage and outputs from the eight-point DIT FFT. The first and second data streams generated FFT outputs of in natural order using upper and lower BF2 in the last stage. In last stage the word length is twice due to the two data paths in the last stage is combined.

**B. Operation of the Conventional Architecture**

L1,L2,L3,M1,M2 and M3 are the six levels of FFT architecture in Fig.3.2. In the levels M2 and M1 respectively the eight-point DIF and DIT FFT operations are performed. With the help of SW2 the data from L2 and M2 can be forwarded to L3 and M3 respectively or vice versa.

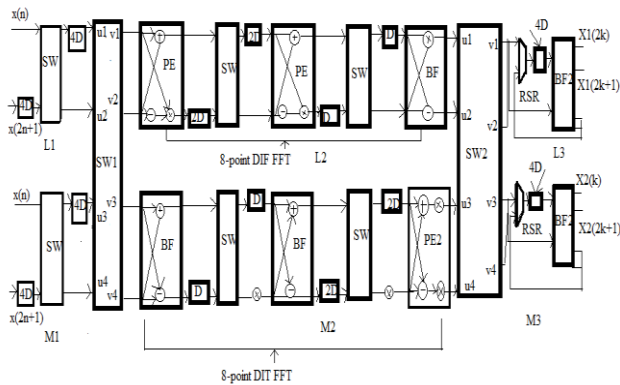


Fig.2: Conventional 16-Point Radix-2 Fft Architecture With Outputs In Natural Order

The partially processed even data is reordered by the RSR registers in the levels L3 and M3 and the odd input data is reordered by the RSR registers in the levels L1 and M1. In the levels L2 and M2 respectively the eight-point DIF and DIT FFT operations are performed. With the help of SW2 the data from L2 and M2 can be forwarded to L3 and M3 respectively or vice versa,  $x(2n)$  and  $x(2n+1)$  are the representation of the two input streams to the FFT processor. In order to swap the data path and propagate the data to different levels SW1 and SW2 have to switches. The switches SW1 or SW2 pass the data at  $u1, u2, u3$  and  $u4$  to  $v3, v4, v1$  and  $v2$  respectively during the swap mode and switches SW1 or SW2 pass the data at  $u1, u2, u3$  and  $u4$  to  $v1, v2, v3$  and  $v4$  respectively during the normal

mode. During  $N/2+1$  to  $NSW1$  is in the normal mode and during the first  $N/2$  clock cycles, SW1 is in the swap mode otherwise during  $N/2+1$  to  $N$  SW2 is in the swap mode and during the first  $N/2$  clock cycle SW2 is in the normal mode. Thus SW1 and SW2 change their modes for every  $N/2$  clock cycles and are indifferent modes at any time. The switches (SW1 or SW2) are in the normal mode, if there is transition of data between  $Ly$  and  $Ly+1$  or  $My$  and  $My+1$  ( $y$  can be 1 or 2). The switches (SW1 or SW2) are in the swap mode, if there is transition of data between  $Ly$  and  $My+1$  or  $My$  and  $Ly+1$ . The control signals of SW1 and SW2 are given as external. This switch helps the signals to swap in the  $N/2$  clock cycle.

**III PROPOSED SYSTEM**

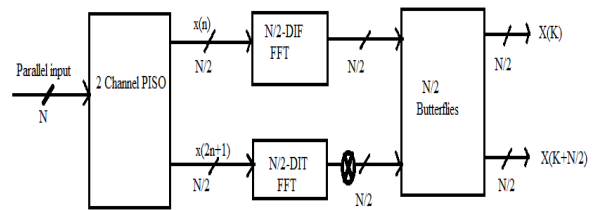


Fig.3 Block Diagram Of Proposed Method

Using two  $N/2$ -point FFT operations with additional one stage of butterfly operations for computing an  $N$ -point FFT is shown in Fig.4.1, it provides the methodology but it is not the exact architecture. To process two data streams using two eight-point MDC FFT. The inputs are received by the PISO unit present at the left side of SW1. The last stage RSR is used store eight-point DIF FFT output and bits reverse them. Butterfly operations done by the bit reversed data in the RSR in the last stage and outputs from the eight-point DIT FFT. The first and second data streams generated FFT outputs of in natural order using upper and lower BF2 in the last stage. In last stage the word length is twice due to the two data paths in the last stage is combined.

**A. Operation of the Proposed Architecture**

To process two data streams using two eight-point MDC FFT. The PISO unit present at the left side of SW1. The inputs are received by the PISO unit. The last stage RSR is used store eight-point DIF FFT output and bits reverse them. Butterfly operations done by the bit reversed data in the RSR in the last stage and outputs from the eight-point DIT FFT. The first and second data streams generated FFT outputs of in natural order using upper and lower BF2 in the last stage. In last stage the word length is twice due to the two data paths in the last stage is combined.

L1, L2, L3, M1 and M2 are the four levels of FFT architecture in Fig.3.4, The partially processed even data is reordered by the RSR registers in the levels L3 and M3 and the odd input data is reordered by the RSR registers in the levels L1 and M1. In the levels L2 and M1 respectively the eight-point DIF and DIT FFT operations are performed. With the help of SW2 the data from L2 and M2 can be forwarded to L3 and

M3 respectively or vice versa. In order to swap the data path and propagate the data to different levels SW1 and SW2 have to switches. The switches SW1 or SW2 pass the data at  $X1, X1$  and  $v1, v2$  respectively during the swap mode and switches SW1 or SW2 pass the data at  $u1, u2, u3$  and  $u4$  to  $v1, v2, v3$  and  $v4$  respectively during the normal mode. During  $N/2+1$  to  $NSW1$  is in the normal mode and during the first  $N/2$  clock cycles, SW1 is in the swap mode otherwise during  $N/2+1$  to  $N$  SW2 is in the swap mode and during the first  $N/2$  clock cycle SW2 is in the normal mode. Thus SW1 and SW2 change their modes for every  $N/2$  clock cycles and are indifferent modes at any time. The switches (SW1 or SW2) are in the normal mode, if there is transition of data between  $Ly$  and  $Ly+1$  or  $My$  and  $My+1$  ( $y$  can be 1 or 2). The switches (SW1 or SW2) are in the swap mode, if there is transition of data between  $Ly$  and  $My+1$  or  $My$  and  $Ly+1$ . The control signals of SW1 and SW2 are given as external. This switch helps the signals to swap in the  $N/2$  clock cycle.  $X1$  and  $X2$  are the representation of the two

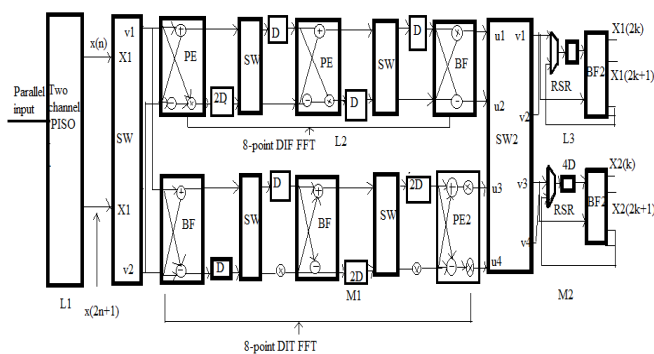


Fig.3.4: Proposed 16-Point Radix-2 FFT Architecture With Outputs In Natural Order

input streams to the FFT processor. The odd even sample in input streams is separated and it is given to two parallel PISO.

- 1) The eight samples of  $X1$  are loaded into the registers in  $L1$ . After eight clock cycles, the switch (SW1) is set in the normal mode and the first eight samples of  $X2$  are loaded into the register  $L1$ . Simultaneously,  $E1(1,1)$  is forwarded to  $L1$  to  $L2$  as  $E1(2,1)$ .
- 2) After eight clock cycles, the positions of the switches SW1 and SW2 are set in the swap mode and the normal mode, respectively. The odd samples ( $O1(1,1)$ ) of  $X1$  are forwarded from  $L1$  to  $M1$  as  $O1(1,1)$  and the even samples ( $E2(1,1)$ ) of  $X2$  is forwarded from  $L1$  to  $L2$  as  $E2(2,1)$ . Simultaneously,  $E1(2,1)$  is forwarded from  $L2$  to  $L3$  as  $E1(3,1)$  and reordering is performed.
- 3) After eight clock cycles, SW1 and SW2 are set in the normal mode and the swap mode, respectively. The odd samples of  $X2$  ( $O2(1,1)$ ) are forwarded from  $L1$  to  $M1$  as  $O2(2,1)$  and  $O1(2,1)$  is forwarded from  $M1$  as  $O1(3,1)$  to  $L3$  where the butterfly operations with  $E1(3,1)$  corresponding to the last stage are performed. In the meantime,  $E2(2,1)$  from  $L2$  is forwarded to  $M2$  as  $E2(2,1)$  and reordering is performed in the RSR.

### A. Bit Reversing

In order to generate the outputs in the natural order a dedicated bit reversal circuit and simultaneous multiple FFT operations are required. For different radices bit reversed circuits are proposed. In variable length similar structure is proposed. The register complexity of it is  $N$ . To bit reverse the data of pipelined FFT of this circuit are suitable.

Table 1 FPGA Implementation Results

N	Registers	LUTs	Latency	Throughput
256[7]	1038	1594	937ns	720MS/s
512[7]	1186	1824	1889ns	720MS/s
256[8]	968	1178	1263ns	380MS/s
512[8]	1126	1497	2568ns	380MS/s
256[1]	1536	2420	505ns	1520MS/s
512[1]	1728	2952	1010ns	1520MS/s
1024[1]	1920	4116	2021ns	1520MS/s
2048[1]	2112	5662	4042ns	1520MS/s

In Table 3.2, shows the FPGA implementation result. In the combinational logic circuits the FPGA is typically implemented by using combinational logic circuits with look up tables. The table output values are just fills, when the FPGA configured it is called look up tables. It is composed of SRAM bits. The time required for one packet of data to reach from one point to another is called latency. When we are observing a system, latency due to the time delay between cause and the physical change of the system. To express how much (information) is reaching from one point to another in data transmission is called network throughput.

### IV CONCLUSION

In this paper, PISO butterfly inputs are used to generate outputs in natural order. The processor can handle two independent data streams simultaneously. The bit reversal circuit present in prior designs is eliminated by using two parallel PISO. The proposed architecture provides throughput higher than the prior architectures and also reduces the complexity of the circuit. Simultaneously two data streams can be processed by the proposed architecture which has two  $N$ -point FFT architectures. So the complexity can be normalized. At present wireless systems have been suddenly developed. To save 30% of the input power consumption, the combination of these techniques has been used.

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