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Advanced Fuzzy Inference Engine

Design of Hardware Circuit for Max – Min Calculator

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Abstract: **The fuzzy logic is successfully applied in various applications in all fields of engineering and science including consumer electronics, control systems, signal and image processing etc. The various fuzzy processing systems have been used by different researchers for development of various applications. The advantage of fuzzy systems is to approximate system behavior where numerical relations do not exist. The basic aim of fuzzy logic system is to develop an imitation of a human intelligent system, with the capability of controlling a given application without any mathematical model. A given a set of input data, the fuzzy inference processor estimate the proposed actions according to their conformance with the knowledge base. A *real-time fuzzy inference* involves processing the knowledge base within constant period of time and with minimum speed of one MFLIPS (Mega fuzzy logic inferences per second).**

Fuzzy inference system requires more time in fuzzy logic due to matching degree calculation. The drawback of high latency of matching degree calculation between the ancient and input membership functions (MF) is avoided by implementing a hardware circuit for max - min calculator circuit to improve the fuzzy inference.
It is common to develop a whole system on a chip with the availability of low cost, large capacity FPGA and advanced computer aided design (CAD) tools. The FPGA reduces die sizes, their cost and greatly reduces the time to market for new consumer products. The proposed architecture calculates the matching degree of trapezoid and triangular together. The architecture is modeled in VHDL and implemented in XILINX.

Keywords: fuzzy logic controller, fuzzy inference processor, linguistic variable, membership function, FPGA.

1. INTRODUCTION

Now-a-days control systems has got priority in various applications; a control system is one which control action depends on one of the parameter in system and it needs numerical calculations for control action, these numerical models are inaccurate and the development of applications using software languages is tough. Here we use a model which can control without any use of numerical values. It can be eliminated by a new logic called fuzzy logic. The idea of fuzzy logic was proposed in the paper by Lotifi A Zadeh of the University of California at Berkeley in 1965. He uses computing with numbers to computing with words and from manipulation of measurements to manipulation of perceptions

The performance of the controller degrades due to the inaccuracy of mathematical modeling, especially for non-linear and complex control systems like PI, PID control systems. Fuzzy logic replaces all conventional control systems Because of the advantages of fuzzy logic systems use in many systems and more researchers are going to use in many applications.

The digital hardware fuzzy inference processor was originally developed by Togai and Watanabe et al [9]. Many variations have been proposed to improve the inferencing performance. Asica, Catania and Russo et. al [8] assume that each membership function is composed of nine segments. They use a binary search algorithm to calculate the matching degree between two membership functions. The main drawback of their fuzzy inference processor [8] is that they use same active rules from the knowledge base when detection. As a result, the inference speed of their fuzzy inference processor depends on the number of active rules. Therefore, their fuzzy inference processor is only suitable for applications that have few active rules. Shih-hsu huang and jian-yuan lai et. al [4] assumes that each membership function is composed of four segments and 64 rules with fuzzified inputs at a speed of 7 MFLIPS. Loan, S.A. and A. M. Murshid et. al [7] assumes that each membership function composed of three segments and 64 active rules but it requires more area compared to Loan, S.A. and A. M. Murshid et. al [5] with four segments and 64 rules. Loan, S.A. and A. M. Murshid et. al [3] assume that each membership function composed of five segments,64 rules and it work for three membership functions: triangular and trapezoidal and Gaussian together. According to Shih-hsu huang and jian-yuan lai et. al [4] eliminates the Gaussian membership function because of its low applications.

In my proposed design assumed that each membership function is composed of four segments, 64 rules and it is combined architecture of Loan, S.A. and A. M. Murshid et. al [7] and et. al [5] because of combined architecture and pipelining usage of LUTs and slice latches are reduced.

II. PRELIMINARIES

In this section we will give you some information on basic terms and fuzzy logic.

Linguistic Variables:

Linguistic variables are defined as the input or output variables of the system whose values are linguistic terms instead of numerical values. A linguistic variable is a set of linguistic terms. Linguistic terms are represented by a simple words or sentence.

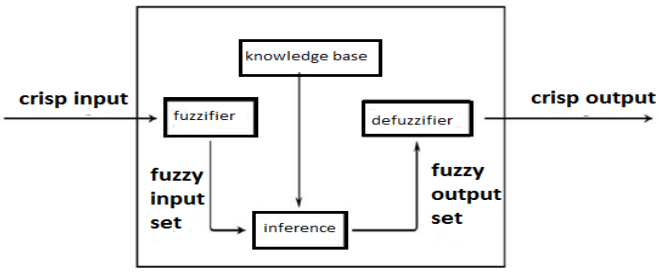

Fig 1: Fuzzy Logic System

Membership Function:

A membership function for a fuzzy set on the universe of discourse set is defined as where each element of universe of discourse set is mapped to a value between 0 and 1. This value, called membership value or matching degree, quantifies the grade of membership of the element in universe of discourse set to the fuzzy set. Membership functions are used in the fuzzification and defuzzification. Membership functions allow us to graphically represent a fuzzy set.

Fuzzy Rules:

In a FLS, a rule base is constructed to control the output variable. A fuzzy rule is a simple IF-THEN rule with a condition and a conclusion.

Fuzzy Logic:

A fuzzy logic system (FLS) relates the crisp input data set to a scalar output data set. Fuzzy logic system consists of four main parts: fuzzification unit, knowledge base, inference engine, and defuzzification unit. These components and the fuzzy logic system architecture are shown in fig 1.

The operation of Fuzzy Logic system is explained as follows; firstly a crisp set of input data is converted into a fuzzy set using fuzzy linguistic variables and membership functions. This step is called as fuzzification. Inference system consists of set of rules which maps the fuzzified membership functions into set of output membership functions. Finally the defuzzifier converts the output membership functions into crisp output.

Various conventional logic systems can be replaced by fuzzy logic systems. The conventional fuzzy system consists of fuzzification and fuzzy inference is an important part of fuzzy processor and its performance measures are area, speed and power. The inference engine performance, particularly the processing speed, is an important measure in case of inference engine. The speed limitation of the inference engine lies in the calculation of the matching degree between the fuzzified input and the antecedent membership functions. The inference processor traverses all the elements in universal disclosure set to obtain the matching degree between the membership functions.

The problem of matching degree calculation between the input and membership functions (MF) is done by implementing a max- min calculator hardware circuit to improve the fuzzy inference speed, the proposed architecture calculates the matching degree between the two types of MF's : trapezoid and triangular together. The architecture will be modeled in VHDL and implemented in XILINX.

III.SYSTEM MODEL AND ASSUMPTIONS

This proposed technique assumed each membership function composed of four segments and each segment represent with one point. This is used for calculating the matching degree to use of a general four point antecedent and fuzzified input functions. For calculating the matching degree the max-min computation is used. This hardware realization, adaptively works for triangular and trapezoidal membership functions. Each membership function is assumed according to HUANG and LAI et. al [4] as minimum value to be '0' and maximum value as '1' and for high performance fuzzy inference matching degree calculates at only crossovers.

IV.DESIGN OF MAX – MIN CALUCLATOR

In this paper a hardware circuit is designed for calculating the Matching degree between antecedent and input using max-min calculator. This proposed paper partitioned the membership function into four discrete point functions for both ancient and input.

For calculating the matching degree between two trapezoidal functions it requires the usage of four mutually exclusive conditions and even triangular functions also require four conditions so, combination of both require six mutually exclusive conditions.

1. If $a3 < x2$ and $x1 < a4$: MD is the graded value of the cross-over point: eq1,shown fig1
2. If x3 < a2 and a1 < x4: MD is the graded value of the cross-over point: eq2 ,shown fig2
3. If a2 < x2 and x1 < a3: MD is the graded value of cross-over point: eq3, shown fig3
4. If $x2 <$ a2 and a1 < $x3$: MD is the graded value of the cross-over point:eq4,shown fig4
5. (a1 = x1 and a2 = x2 and a3 = x3 and a4 = x4) or (a1<=x1 and x1 <= a2) or (x1<=a1 and a1<=x1) : MD = '1'.shown fig 5(a), fig5 (b).

6. If $a4 \leq x1$ and a3<x1 or $x4 \leq a1$ and x3<a1: MD = '0'fig 6

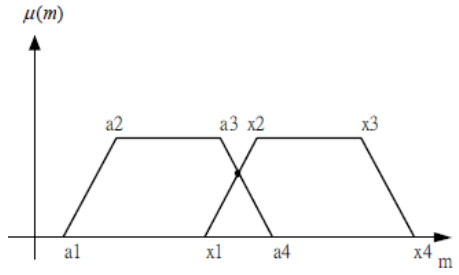

Fig 1

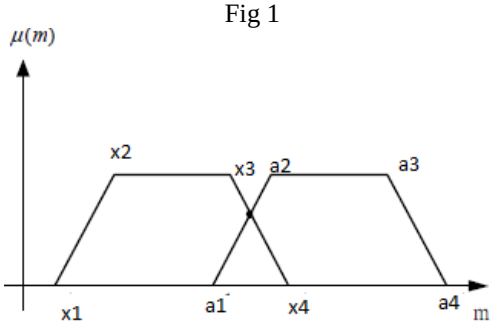

Fig 2

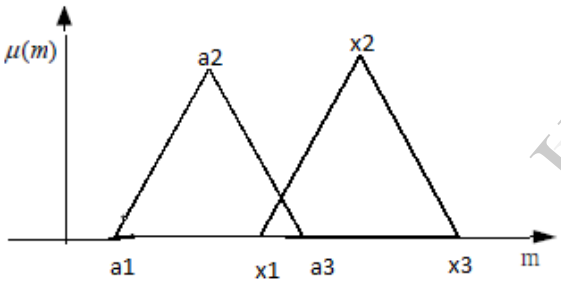

Fig 3

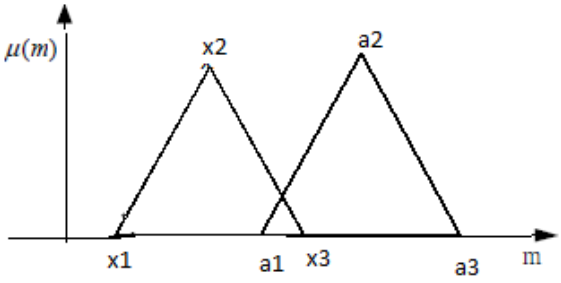

Fig 4

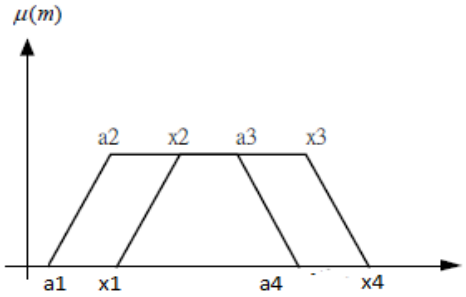

Fig 5(a)

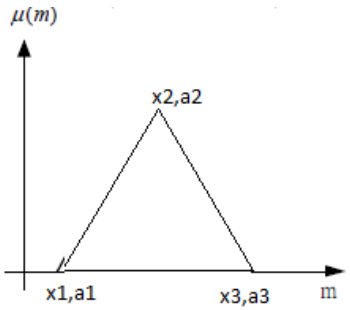

Fig 5(b)

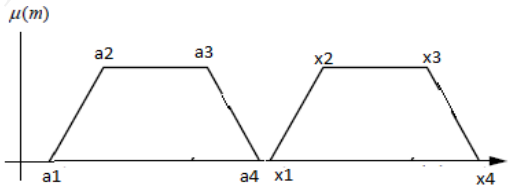

Fig 6

If (a3 < x2 and x1 < a4) Then Matching degree (M.D) given by

$$M.D = 2^{l} - 2^{l} * \frac{(x2 - a3)}{(x2 - a3) + (a4 - x1)} \quad [1]$$

If (x3 < a2 and a1 < x4) Then Matching degree (M.D) given by

$$M.D = 2^{l} - 2^{l} * \frac{(a2 - x3)}{(a2 - x3) + (x4 - a1)} \quad [2]$$

If (a2 < x2 and x1 < a3) Then Matching degree (M.D) given by

$$M.D = 2^{l} - 2^{l} * \frac{(x2 - a2)}{(x2 - a2) + (a3 - x1)} \quad [3]$$

If (x2 < a2 and a1 < x3) Then matching degree (M.D) given by

$$M.D = 2^{l} - 2^{l} * \frac{(a2 - x2)}{(a2 - x2) + (x3 - a1)} \quad [4]$$

Proof: considering the condition for Eq – 2 for assuming segmented points are aligned as a3 < x2 and x1 < a4

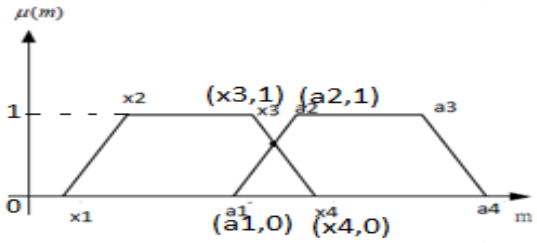

Fig 7

Equation 5 is obtained from a straight line passing through (x3, 1) and(x4, 0) as

$$\mu(m) = \frac{X - x4}{x3 - x4} \qquad [5]$$

Equation 6 is obtained from a straight line passing through (a1, 0) and (a2, 1) as

$$\mu(m) = \frac{X - a1}{a2 - a1} \qquad [6]$$

Equating the equations 5 and 6 we get the following equation 7

$$X = \frac{x4a2 - a1x3}{x4 - x3 + a2 - a1} \qquad [7]$$

Substituting the equation 7 into equation 5 or 6 we get matching degree (M.D)

$$\mu(m) = \frac{a2 - x3}{a2 - x3 + x4 - a1} \qquad [8]$$

Equation 4 is Decimal fraction equivalent of equation 2. Its discrete equal can be obtained by multiply and subtract the decimal fraction from the 2 (segmented points) it is shown in equation 2.

V. RESULTS

Proposed method of matching degree (MD) calculator is done using VHDL (very high speed hardware description language) and is modeled in xillinx13.4 version and implemented on FPGA SPARTAN-3. In this proposed approach a very high speed MD calculator is designed and implemented to improve the speed of fuzzy logic controller.

The Fig 8 shows the simulation results and table-1 shows the comparison of Loan, S.A. and A. M. Murshid [5] and [7] with proposed and combined structure. It gives the matching degree (MD) calculation between the antecedent and fuzzified membership functions. In this implementation, A (a1, a2, a3, a4) represents four segmented points of antecedent membership function and X(x1, x2, x3, x4) represents four segmented points of fuzzified input. These eight signals are applied simultaneously applied as an input to MD calculator and it gives an output as matching degree (h) in the proposed design the number of segmented points are 4,3 for trapezoidal and triangular respectively and corresponding grade value has discrete into 16,8 for trapezoidal and triangular respectively.

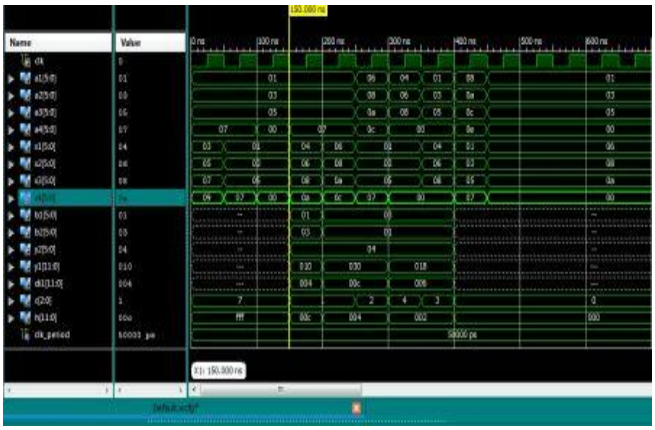

Fig 8

The number of bits used to represent each segment point is 6 bits; it gives the universe of discourse set and the total number of elements in the universe of discourse set is 64 rules.

These results can be easily checked by taking second condition in result i.e. membership function for ancient and fuzzified input values a1, a2, a3, a4 and x1, x2, x3, x4 are 1,3,5,7 and 4,6,7,9 respectively.

The above values are under first condition then use the eq-1 to compute the matching degree and the obtained value is 0.25. This fractional value changed to discrete value by using number of segment points. The above condition under the trapezoidal membership function then it uses four segment points for its representation and the graded value made discrete value into 16 levels i.e. matching degree between the values of 1 to 15. For the above condition matching degree (h) obtained as 000000001100. It is shown in simulation result.

The values of A (1, 3, 5, 7) and X (3, 5, 7, 9) are completely matching and it gives graded value (h) as 1 discrete value of "FFF"h;

The values of A (8, a, c, e) and X (1, 3, 5, 7) are completely mismatching it and it gives graded value as 0 discrete value of"000"h;

VI.COMPARISION

The hardware implementation of MAX-MIN calculator has been implemented in SPARTAN-3 XC3S50 XILLINX FPGA. This FPGA consists of 1536 slices, 1536 4-input LUTs and 124 bonded input/output buffers (IOB). Table-1 gives the comparative analysis of the utilization of resources in implementation of triangular [7], trapezoid [5] and proposed MAX-MIN calculator circuits. This shows the combined structure of both trapezoidal and triangular consumes very less number of FPGA resources. The main feature of combined structure adaptively works for triangular and trapezoidal membership functions together. In table-1 shows the two designs of the trapezoidal, triangular processors consumes 1228 4-input LUTs, on

other hand the proposed advanced max-min calculator uses only 152 LUTs, it shows that it saves the 71% of LUTs usage. And combined structure reduces the 70% usage of slices. Average Fan-out also reduced shown in table-1 and it gives reduction in the power. This FPGA resource utilization shows the proposed architecture efficient in area and power. And the best of our knowledge it has been seen that it operates at speed of 76 MHz (12.46ns). There is a further scope for improvement in the proposed design by using pipelining and use of new methodology to further reduce the area and latency.

Device Utilization Summary

		Triangular		trapezoidal		proposed		%Saving resources
Logic Utilization	available	used	Utilization	used	utilization	used	Utilization	proposed
Number of Slice Latches	1,536	8	1%	2	1%	3	1%	0%
Number of 4 input LUTs	1,536	604	39%	640	41%	152	9%	71%
Number of occupied Slices	768	313	40%	323	42%	83	10%	72%
Number of Slices containing only related logic	83	313	100%	323	100%	83	100%	0%
Number of bonded IOBs	124	48	38%	60	48%	87	70%	17%
Average Fan-out of Non-Clock Nets		3.22		3.14		2.5		

Table-1

VI .CONCLUSION

A new VLSI architecture for a fuzzy inference processor using advanced fuzzy inference processor. Fuzzy inference processor using hardware realization of max-min calculator implemented on SPARTAN-3 FPGA. This hardware realization and comparisons shows that it is power, area and speed efficient compared to existing architectures and also it works for both trapezoidal and triangular together.

REFERENCES

[1] L. A. Zadeh, “Fuzzy logic”, IEEE Computer, vol.1 no. 4, pp. 83–93,1988.
[2] L. A. Zadeh, “Fuzzy sets”, Information and Control, Vol. 8, pp. 338-351, 1965.
[3] Loan, S.A. and A. M. Murshid “A novel VLSI architecture of a multi membership function based MAX-MIN calculator circuit,” Advanced Electronic Systems (ICAES), 2013 International Conference.
[4] S.H.Huang and J.Y.Lai,“A High-Speed VLSI Fuzzy Logic Controller with Pipeline Architecture”, in Proceeding of IEEE International Conference on Fuzzy System, 2001.
[5] Loan, S.A. and A. M. Murshid "A Novel Fuzzy Inference Processor using Trapezoidal-Shaped MF," in proceeding of IEEE International Conference on Open Systems, Malaysia, 25-28 September, 2011.
[6] A. Lukasiewicz,"On three-valued logic,"in polish,pp. 110-128, 1961.
[7] Loan, S.A. and A. M. Murshid “Architectural Design of Fuzzy Inference Processor using Triangular-Shaped Membership Function,” in processing of 2011 IEEE Conference on Open Systems (ICOS2011), September 25 - 28, 2011, Langkawi, Malaysia.
[8] G. Asica, V. Catania, and M. Russo, “VLSI hardware architecture for complex fuzzy systems,” IEEE Transactions on Fuzzy Systems, Vol. 7, 1999, pp. 553-570.
[9] M. Togai and H. Watanabe, “Expert system on a chip: an engine for real-time approximate reasoning,” IEEE Expert Magazine, Vol. 1, 1986, pp. 55-62.