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ADS based Analysis for Wireless Sensor Node

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Abstract— **Wireless Sensor (WS) node design, most critical issue is to minimize power consumption. Power model for Wireless Sensor Network (WSN) incorporates power characteristics of node hardware components and software strategies. WS node design should also consider the power loss due to the RF segment of node. RF segment is designed based on transmission line theory, which if not designed properly may result in losses due to impedance mismatch and unwanted reflections. In this paper we have simulated the microstrip tracks designed for WS node to account for the power loss and in turn optimize the design. Advanced Design Simulation (ADS) software has been used for RF layout simulation. To validate the simulation results the designed layouts were fabricated and tested for RF power received with spectrum analyzer. Simulation and practical observations are discussed in this paper.**

Keywords— ***Wireless, Microstrip, Sensor, RF, Transmission Line, Spectrum, ADS.***

I. Introduction

Wireless Sensor (WS) node is the most important component for the Wireless Senor Networking (WSN). WS node typically includes a *microcontroller*- to execute local data processing and networking operation, a *radio transceiver* – to send/ receive data and *sensor interface* –to sense/ measure system parameters. Generally, WSN deployments consist of large no of WS nodes (dense deployment) in sensing environment and each node transmits sensor data to cluster head/base station. Dense deployment in WSN demands for low transmits power for WS node radio transceivers to reduce interference. Considering this aspect, all the radio transceivers meant for WSN applications, following IEEE 802.15.4 protocol are designed for low (<100mW) transmit power. The RF (100MHz to GHz) output of the radio transceiver has to be fed with no loss or minimum loss to antenna for radiating efficiently and to meet the power criteria [1].

Design of RF interface involves impedance matching and converting differential output of RF IC to single ended for feeding the antenna. Tracks/ interconnects for RF interface have been designed using standard microstrip formula. Performance of the designed layout (i.e. impedance matching and minimum loss) can be estimated through simulation of the layout and can be verified through the practical testing of the boards using vector network analyzer/ signal analyzer. The designed RF layouts have been simulated in Advanced Design System (ADS) [2] software to generate S parameter plots. This paper briefly describes the research work done in RF/microstrip simulation field in section II. Section III summarizes the WS node structure in general. The concept of microstrip design and about RF layout simulation ADS environment has been explained in Section IV and V respectively. Section VI presents the comparative study of simulated and practical observation for RF signal. Section VII concludes the paper.

II. Literature Survey

This work combines the ideas from various WS node design and WSN establishments. In [3]-[7], authors have covered on the aspect of designing industrial grade node and its deployment in Industrial environment. The WS node design discussed in this paper is also Industrial Grade node; but more emphasis has been put on the RF layout design and its analysis. RF related analysis is required to avoid signal attenuation, to minimize adjacent channel interference and to minimize unwanted coupling in nearby tracks.

In [8], author has simulated the microstrip pass band filter in ADS. Same has been used for RF layout analysis by the authors in this paper. Substrate material, simulation frequency, design parameter and analysis done is different from the structure simulated in their paper.

In [9], author has simulated the microstrip antenna, which has to radiate the maximum power. In our design microstrip track has been designed to minimize the RF emissions and to give maximum feed to the external antenna connected to the board.

In all these papers, overall node design for industrial environment and microstrip simulations with ADS has been done. Our paper discuss about the microstrip simulation of RF layout designed for the WS node. Also we have validated the simulated results with the practical observations, i.e. RF signal measurement using spectrum analyzer [10], [1].

III. WS Node Design

WS node design is application dependent. The WS node used for RF layout analysis has been designed for deployment in nuclear plant (i.e., it is industrial grade node). The node consists of CortexM3 based microcontroller with Atmel RF chip based wireless interface and support for 4 sensor connections. The node has been designed with modular approach which consists of microcontroller module, RF module and sensor interface module. Different modules are connected with connectors to make a complete WS node. Developed WS node and RF module have been shown in fig 1. Due to modular approach RF module operating in different frequencies can be connected to microcontroller module. Nuclear reactor present deployments [11] uses 2.4GHz operating WS node but this signal do not have significant strength to penetrate through the 1metre thick reactor containment wall, it is based on test conducted across RCB for different power levels [12]. For, the above mentioned application separate RF board has been designed to operate in 868/915MHz band as RF range increases with reduction in frequency[13].

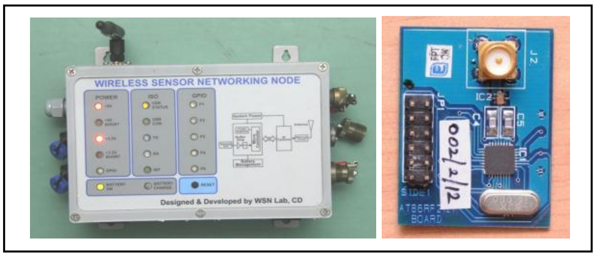


Fig. 1. Developed Wireless Sensor Node and RF Board

IV. MICROSTRIP TRANSMISSION LINE DESIGN FOR THE WS NODE RF LAYOUT

Theoretical relations for microstrip design [14], [15] shows that the characteristic impedance, Zo of microstrip line depends on the following parameters: εr - the relative permittivity of substrate, W - the width of the strip, h - the thickness ("height") of substrate, and t -the thickness of the strip metallization. Fig 2 and 3 shows the characteristic impedance variation with respect to W/h ratio. Substrate type used is FR4, εr-4.5Authors and Affiliations

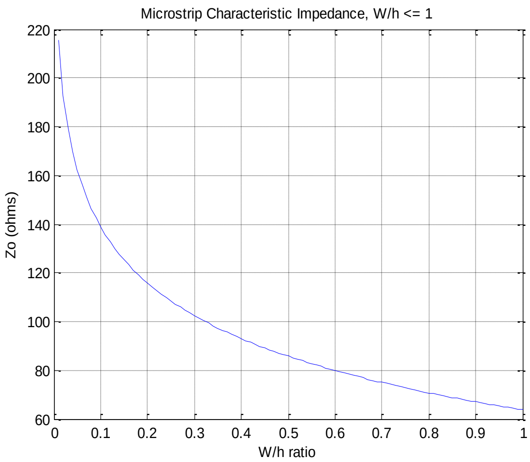


Fig. 2. Microstrip characteristic impedance plot, W/h ≤ 1

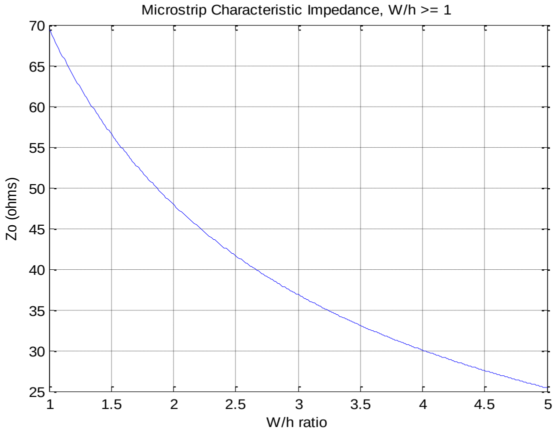


Fig. 3. Microstrip characteristic impedance plot, W/h ≥ 1

For our WS node, RF track/ microstrip has to be designed between RF IC and BALanced to UNbalanced converter (BALUN) for the characteristic impedance of 100Ω (Blue) and BALUN to Antenna centre feed for the characteristic impedance of 50Ω (Green) as shown in fig 4. FR4 type, substrate selected for board design is of 0.8mm height, h. As per the design board specifications, Table 1 gives the track width, W obtained from fig 3 and fig 4 to achieve the characteristic impedance (100Ω and 50Ω) for the RF layout.

TABLE I. W- track width for 0.8mm FR4 substrate for 50 Ω and 100 Ω characteristic impedance

Dielectric Thickness, h	W for 50Ω	W for 100Ω
0.8mm	1.37 mm	0.254 mm

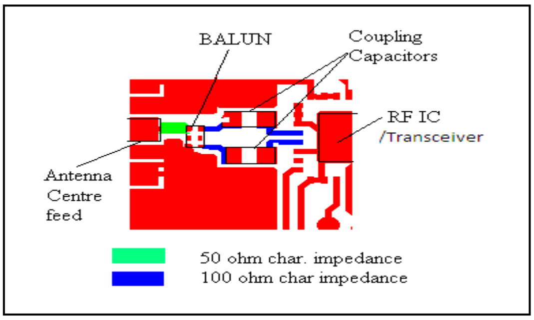


Fig. 4. RF layout: Blue and Green color shows the portion designed using Acknowledgment *(HEADING 5)*

V. MICROSTRIP TRACK SIMULATION IN ADVANCED DESIGN SYSTEM

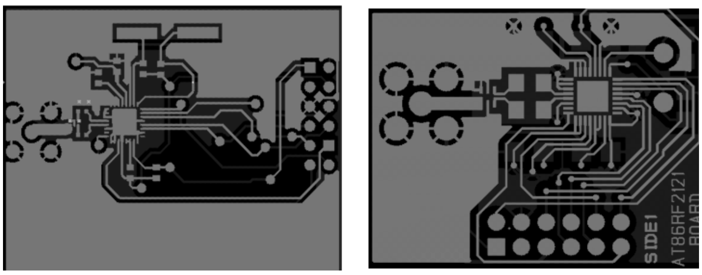
Microstrip track calculations do not incorporate the practical aspects to be followed while making layout. In calculations, it is assumed that the two connecting ports are aligned to each other and connected straight. Practically, the IC/ components packaging is standard. It is rare to have same pin spacing for two different components having different type of package. This mismatch in pin spacing, does not allow us to connect the components with straight tracks. Also, as per the components spacing in the layout, angular turns for tracks are needed. Angle corner have width more than the straight track [16], which results in different characteristic impedance. From EMI aspect, electric fields may get concentrated at angle corners. Considering the different options for connecting RF components (RF IC & BALUN in this paper), two RF layout designs has been made. In Design 1 shown in fig 5 (a), the 100Ω differential tracks are routed in such a way that RF tracks make a 90º angle. In Design 2 as shown in fig 5 (b), the 100Ω differential tracks have been routed in such a way that angle is more than 90º, it is around 120º. Implications of the track routing in Design 1 & 2 will be discussed in section VI.

Losses due to corner/ impedance mismatch can be estimated by simulating the designed microstrip tracks. For simulation ADS has been used. The current design has been made to operate in 868/915MHz. To compute the S-parameters, Momentum part of ADS has been used. Momentum gives us a complete tool set to predict the performance of high-frequency circuit boards, antennas, and ICs.

Full layout simulation will consume more memory and time, so part of layout related to RF is sufficient for simulation to calculate the attenuation losses and solve impedance mismatch issues. Thus segmented simulation improves the efficiency.

Microstrip track simulation has been done by importing the layout in ADS. Ports are assigned to RF track excitation point (PORT1) and signal extraction point (PORT2). S parameters give the idea of signal loss from directly connected ports and also conveys about the unwanted coupling in physically unconnected ports.

Excitation signal fed to these ports is assigned from 860 MHz to 930 MHz and FR4 material is assigned to the substrate. For simulation, the ADS splits the designed structure into segments as per assigned frequency in setup using finite element method.



(a) Design 1 (b) Design 2

Fig. 5. RF layout for 868/915MHz board using AT86RF212

VI. RESULTS: SIMULATION & PRACTICAL OBSERVATION

In simulation results, S parameter for differential PORT1 & PORT2 are observed. S(1,2) shows the amount of signal transferred from PORT 1 to PORT2. There are two plots associated with S parameter; one shows the magnitude/ dB level of the signal and other plot shows the phase change with respect to frequency.

As per fig 6 & 7 the signal at PORT 2 is 63 dB less than signal at PORT 1 and it is around -60º to -90º shifted. The signal strength plot, fig 8 and the phase plot, fig 9 obtained for Design 2, conveys that the signal at PORT2 is approximately of same level as that fed to PORT1 and the maximum phase shift is in the order of -3º which is acceptable.

To validate the simulation results, the boards were fabricated based on the designed layouts. The RF power transferred to the RPSMA connector of antenna through 50Ω impedance track was measured and observed in spectrum analyzer.

For practical measurement, the RF transceiver was configured to transmit at 5dBm power level and the output of RPSMA connector in RF board was fed to signal analyzer. Signal power plot for Design 1, fig 10 shows that signal strength measured is 58 dB less (-53 dBm-5dBm) with respect to signal fed by transceiver. For Design 2, from signal power plot, fig 11, it can be inferred that measured signal is 0.5 dB less (4.5dBm -5dBm) than the input.

A. For Desian1:

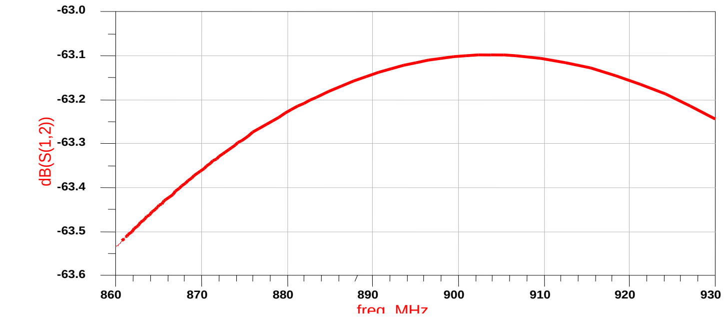


Fig. 6. Design 1, Signal strength transferred to PORT2 from PORT1

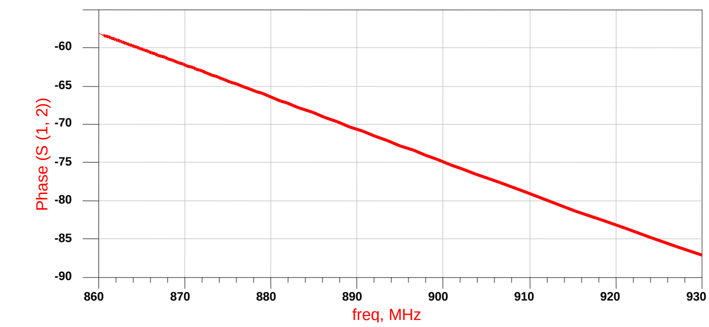


Fig. 7. Design 1, Phase change obtained in signal from PORT1 to PORT2

B. For Design 2:

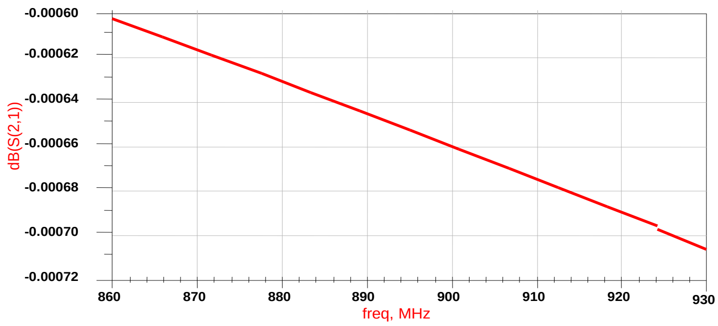


Fig. 8. Design 2, Signal strength transferred to PORT2 from PORT1

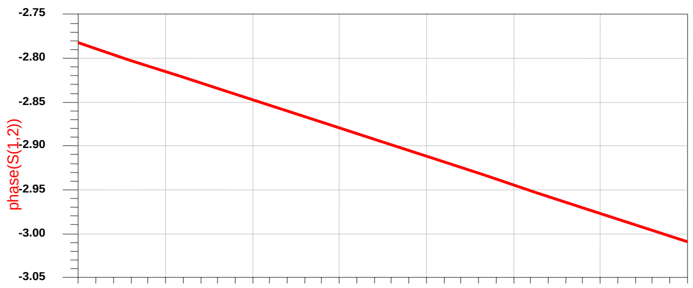


Fig. 9. Design 2, Phase change obtained in signal from PORT1 to PORT2

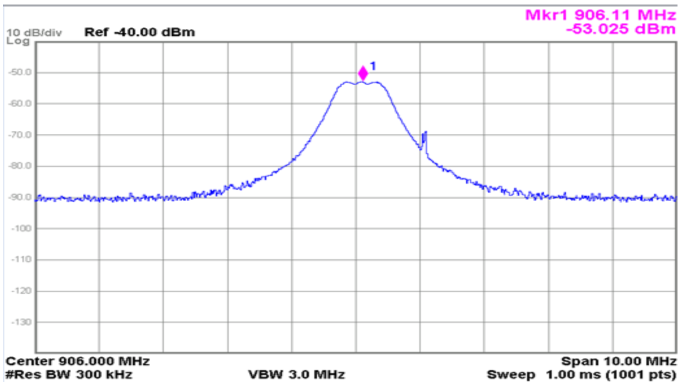


Fig. 10. Peak Power measured for Design 1 using Signal Analyzer, transceiver configured for 5dBm

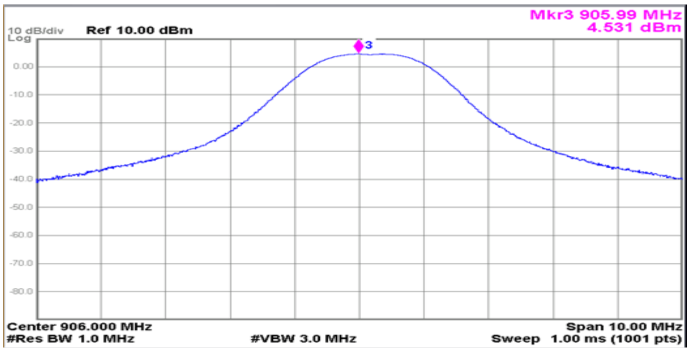


Fig. 11. Peak Power measured for Design 1 using Signal Analyzer, transceiver configured for 5dBm

All the above simulation plots and signal analyzer plots obtained for Design 1 and 2 shows that both the results are in close agreement.

VII. CONCLUSION & FUTURE WORK

In this paper two microstrip based RF layouts designed for WS node were analyzed. Analysis has been done with simulation results obtained through ADS and power spectrum obtained through spectrum analyzer. RF layouts have been designed with same theoretical microstrip track calculations. There is significant RF signal loss for Design 1 due to the 90 degree corners, which results in track width of 1.414times of the actual calculated width, i.e. characteristic impedance changes. Thus, design of microstrip tracks should be as per the calculations, but care needs to be taken in layout design, to avoid unwanted reflections and signal attenuation. The above analysis and comparison gives the confidence that ADS simulation results are close to practical observations. In future any RF design before fabrication can be simulated and optimized in ADS as per requirement. As the required RF functionality is achieved, the designed layouts can be tested in future for radiated emission, to verify that WS node other modules or nearby circuitry functionality is not affected.

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