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Adjustable speed control of PMBLDCM Drive using High Efficiency AC/DC Converter for Power Factor Correction

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Abstract

Harmonic pollution and low power factor in power systems caused by power converters have been of great concern. To overcome these problems several converter topologies using advanced semiconductor devices and control schemes have been proposed. This investigation is to identify a low cost, small size, efficient and reliable ac to dc converter to meet the input performance index of UPS. The performance of single phase and three phase ac to dc converter along with various control techniques are studied and compared. This paper presents a novel ac/dc converter based on a quasi-active power factor correction (PFC) scheme. In the proposed circuit, the power factor is improved by using an auxiliary winding coupled to the transformer of a cascade dc/dc fly back converter. The auxiliary winding is placed between the input rectifier and the low-frequency filter capacitor to serve as a magnetic switch to drive an input inductor. Since the dc/dc converter is operated at high-switching frequency, the auxiliary windings produce a high frequency pulsating source such that the input current conduction angle is significantly lengthened and the input current harmonics is reduced. It eliminates the use of active switch and control circuit for PFC, which results in lower cost and higher efficiency. Finally a Permanent Magnet Brushless DC motor (PMBLDC) load is applied and simulation results are presented.

1. Introduction

Permanent magnet brushless DC motors (PMBLDCMs) are preferred motors for a compressor of an air-conditioning (Air-Con) system due to its features like high efficiency, wide speed range and low maintenance requirements [1-4]. The operation of the compressor with the speed control results in an improved efficiency of the system while maintaining the temperature in the air-conditioned zone at the set reference consistently. Whereas, the existing air conditioners mostly have a single-phase induction motor to drive the compressor in „on/off" control mode. This results in increased losses due to frequent on/off operation with increased mechanical and electrical stresses on the motor, thereby poor efficiency and reduced life of the motor. Moreover, the temperature of the air conditioned zone is regulated in a hysteresis band. Therefore, improved efficiency of the Air-Con system will certainly reduce the cost of living and energy demand to cope-up with ever-increasing power crisis.

A PMBLDCM which is a kind of three-phase synchronous motor with permanent magnets (PMs) on the rotor and trapezoidal back EMF waveform, operates on electronic commutation accomplished by solid state switches. It is powered through a three-phase voltage source inverter (VSI) which is fed from single-phase AC supply using a diode bridge rectifier (DBR) followed by smoothening DC link capacitor. The compressor exerts constant torque (i.e. rated torque) on the PMBLDCM and is operated in speed control mode to improve the efficiency of the Air-Con system.

Since, the back-emf of the PMBLDCM is proportional to the motor speed and the developed torque is proportional to its phase current [1-4], therefore, a constant torque is maintained by a constant current in the stator winding of the PMBLDCM whereas the speed can be controlled by varying the terminal voltage of the motor. Based on this logic, a speed control scheme is proposed in this paper which uses a reference voltage at DC link proportional to the desired speed of the PMBLDC motor.

However, the control of VSI is only for electronic commutation which is based on the rotor position signals of the PMBLDC motor. The PMBLDCM drive, fed from a single-phase AC mains through a diode bridge rectifier (DBR) followed by a DC link capacitor, suffers from power quality (PQ) disturbances such as poor power factor (PF), increased total harmonic distortion (THD) of current at input AC mains and its high crest factor (CF). It is mainly due to uncontrolled charging of the DC link capacitor which results in a pulsed current waveform having a peak value higher than the amplitude of the fundamental input current at AC mains. Moreover, the PQ standards for low power equipments such as IEC 61000-3-2 [5], emphasize on low harmonic contents and near unity power factor current to be

drawn from AC mains by these motors. Therefore, use of a power factor correction (PFC) topology amongst various available topologies [6-14] is almost inevitable for a PMBLDCM drive.

Most of the existing systems use a boost converter for PFC as the front-end converter and an isolated DC-DC converter to produce desired output voltage constituting a two-stage PFC drive [7-8]. The DC-DC converter used in the second stage is usually a flyback or forward converter for low power applications and a full-bridge converter for higher power applications. However, these two stage PFC converters have high cost and complexity in implementing two separate switch-mode converters, therefore a single stage converter combining the PFC and voltage regulation at DC link is more in demand. The single-stage PFC converters operate with only one controller to regulate the DC link voltage along with the power factor correction. The absence of a second controller has a greater impact on the performance of single-stage PFC converters and requires a design to operate over a much wider range of operating conditions.

For the proposed voltage controlled drive, a half-bridge buck DC-DC converter is selected because of its high power handling capacity as compared to the single switch converters. Moreover, it has switching losses comparable to the single switch converters as only one switch is in operation at any instant of time. It can be operated as a single-stage power factor corrected (PFC) converter when connected between the VSI and the DBR fed from single-phase AC mains, besides controlling the voltage at DC link for the desired speed of the Air-Con compressor. A detailed modeling, design and performance evaluation of the proposed drive are presented for an air conditioner compressor driven by a PMBLDC motor of 1.5 kW, 1500 rpm rating.

2. Proposed PMBLDC Motor Speed Control Scheme of Air Conditioners

The proposed speed control scheme (as shown in Fig. 1) controls reference voltage at DC link as an equivalent reference speed, thereby replaces the conventional control of the motor speed and a stator current involving various sensors for voltage and current signals. Moreover, the rotor position signals are used to generate the switching sequence for the VSI as an electronic commutator of the PMBLDC motor. Therefore, rotor-position information is required only at the commutation points, e.g., every 60°electrical in the three- phase [1-4]. The rotor position of PMBLDCM is sensed using Hall effect position sensors and used to generate switching sequence for the VSI as shown in Table-I.

The DC link voltage is controlled by a half-bridge buck DC-DC converter based on the duty ratio (D) of the converter. For a fast and effective control with reduced size of magnetics and filters, a high switching frequency is used; however, the switching frequency (fs) is limited by the switching device used, operating power level and switching losses of the device. Metal oxide field effect transistors (MOSFETs) are used as the switching device for high switching frequency in the proposed PFC converter. However, insulated gate bipolar transistors (IGBTs) are used in VSI bridge feeding PMBLDCM, to reduce the switching stress, as it operates at lower frequency compared to PFC switches.

The PFC control scheme uses a current control loop inside the speed control loop with current multiplier approach which operates in continuous conduction mode (CCM) with average current control. The control loop begins with the comparison of sensed DC link voltage with a voltage equivalent to the reference speed. The resultant voltage error is passed through a proportional-integral (PI) controller to give the modulating current signal. This signal is multiplied with a unit template of input AC voltage and compared with DC current sensed after the DBR. The resultant current error is amplified and compared with saw-tooth carrier wave of fixed frequency (fs) in unipolar scheme (as shown in Fig.2) to generate the PWM pulses for the half-bridge converter. For the current control of the PMBLDCM during step change of the reference voltage due to the change in the reference speed, a voltage gradient less than 800 V/s is introduced for the change of DC link voltage, which ensures the stator current of the PMBLDCM within the specified limits (i.e. double the rated current).

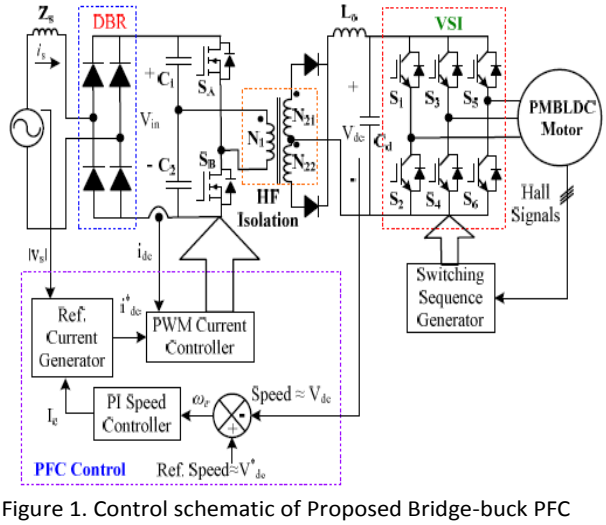

Figure 1. Control schematic of Proposed Bridge-buck PFC converter fed PMBLDCM drive

3. Design of PFC Buck Half-Bridge Converter Based PMBLDC Drive

The proposed PFC buck half-bridge converter is designed for a PMBLDCM drive with main considerations on PQ constraints at AC mains and allowable ripple in DC link voltage. The DC link voltage of the PFC converter is given as,

$$Vdc = 2 (N21/N1) Vin D \text{ and } N21=N22 \quad (1)$$

where N1, N21, N22 are number of turns in primary, secondary upper and lower windings of the high frequency (HF) isolation transformer, respectively**.**

$$Vin = 2\sqrt{2}Vs/\pi \quad (2)$$

To reduce the ripples introduced due to high switching frequency, a suitable ripple filter is designed for constant output voltage of the buck bridge converter. The inductance (Lo) of an output ripple filter restricts the inductor peak to peak ripple current (ΔILo) within a specified range for the given switching frequency (fs), whereas the capacitance (Co) is calculated for a specified ripple in the output voltage (ΔVCo). The output filter inductor and capacitor are given as,

$$Lo= (0.5-D)Vdc/\{fs(\Delta ILo) \} \quad (3)$$

$$Co=Io/(2\omega\Delta VCo) \quad (4)$$

The PMBLDCM considered in this work is rated at 3.75 kW, 1500 rpm. Therefore, the PFC converter is designed at a base DC link voltage of Vdc = 200 V at Vin = 198 V for Vs = 220 Vrms. Other design data include: fs = 40 kHz, Io = 20 A, ΔVCo= 6 V (3% of Vdc), ΔILo= 2.0 A (10% of Io). The design parameters are calculated as Lo=0.6 mH, Co=5000 μF.

The main components of the proposed PMBLDCM drive are the PFC converter and PMBLDCM drive, which are modeled by mathematical equations. The complete PMBLDCM drive is represented as a combination of the individual models of the PFC converter and the VSI-fed PMBLDCM drive. The modeling is discussed in the next section.

4. Modelling of the Proposed PMBLDC Drive

The main components of the proposed PMBLDCM drive are the PFC converter and PMBLDCM drive, which are modeled by mathematical equations and the complete drive is represented as a combination of these models.

4.1 Speed Controller

The speed controller, the prime component of this control scheme, is a proportional-integral (PI) controller that closely tracks the reference speed as an equivalent reference voltage. A voltage gradient less than 800 V/s is introduced for the change of DC link voltage during step change of the reference voltage due to the change in the reference speed, which ensures the stator current of PMBLDCM within the specified limits (i.e., double the rated current). At the kth instance of time, V*dc(k) is the reference DC link voltage, Vdc(k) is the sensed DC link voltage, and the voltage error Ve(k) is calculated as,

$$Ve(k) =V^*dc(k)-Vdc(k) \quad (5)$$

The PI controller gives desired control signals after processing this voltage error. The output of the controller Ic(k) at kth instant is given as,

$$Ic (k) = Ic (k-1) + Kp\{Ve(k) - Ve(k-1)\} + KiVe(k) \quad (6)$$

where Kp and Ki are the proportional and integral gains of the PI controller.

4.2 Reference Current Generator

The reference input current of the buck bridge converter is denoted by idc* and is given as,

$$idc^* = Ic (k) u_{vs} \quad (7)$$

where u_{vs} is the unit template of the voltage at input AC mains calculated as,

$$uvs = vd/Vsm;\ vd = |vs|;\ vs= Vsm \sin \omega t \quad (8)$$

where ω is the frequency in rad/sec at input AC mains.

4.2 PWM Controller

The reference input current of the buck bridge converter (idc*) is compared with the sensed current (idc) to generate the current error Δidc=(idc* - idc). This current error is amplified by gain kdc and compared with fixed frequency (fs) carrier waveforms md [18] as shown in Fig. 2a to get the switching signals for the MOSFETs of the buck bridge PFC converter. Fig 2b shows simplified carrier waveforms md1(t) and md2(t) that are compared with the amplified error

5. Modeling of PMBLDCM Drive

The PMBLDCM drive consists of an electronic commutator, a VSI, and a PMBLDC motor. These components are modeled as given below.

5.1 Electronic Commutator

The electronic commutator uses signals from the Hall effect position sensor to generate signals (Table 1). The switching sequence for the voltage source inverter is generated based on the logic given in Table 2.

5.2 Voltage Source Inverter (VSI)

Fig. 2 shows an equivalent circuit of a VSI-fed PMBLDCM. The output of VSI to be fed to phase 'a' of the PMBLDC motor is given as,

vao = (Vdc/2) for S1 = 1 and S2 = 0 (9)

vao = (-Vdc/2) for S2 = 1 and S1 = 0 (10)

vao = 0 for S1 = 0 and S2 = 0 (11)

van = vao - vno (12)

where 1 and 0 represent the 'on' and 'off' positions of the IGBT switch of the VSI, respectively, and are considered in a similar way for other IGBT switches of VSI i.e., S3- S6. Using similar logic, vbo, vco, vbn, and vcn are generated for two other phases of the VSI feeding PMBLDC motor. The voltages vao, vbo, vco,, and vno are voltages of the threephases and the neutral point (n) with respect to the virtual mid-point of the DC link voltage shown as 'o' in Fig. 3. The voltages van, vbn, and vcn are voltages of three-phases with respect to the neutral point (n); Vdc is the DC link voltage.

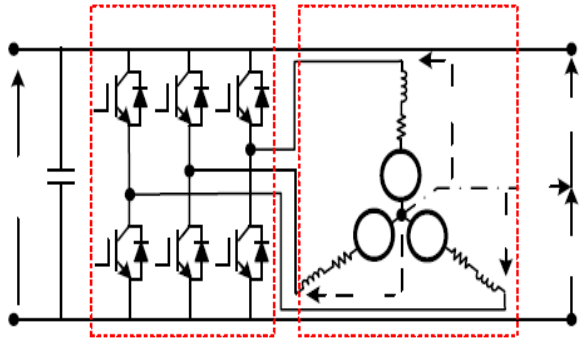

Fig. 2. Equivalent Circuit of a VSI-fed PMBLDCM Drive.

5.2 Voltage Source Inverter (VSI)

The PMBLDCM is modeled in the form of a set of differential equations given as,

van = Ria + pλa +ean (13)
vbn = Rib + pλb +ebn (14)
vcn = Ric + pλc +ecn (15)

In these equations, p represents the differential operator
(d/dt); ia, ib, and ic are current; λa, λb, and λc are flux linkages, and ean, ebn, and ecn are the phase to neutral back EMF of PMBLDCM, in respective phases; R is the resistance of motor windings/phase. Moreover, the flux linkages can be represented as,

λa = Lsia - M (ib + ic) (16)
λb = Lsib - M (ia + ic) (17)
λc = Lsic - M (ib + ia) (18)

where Ls is the self-inductance/phase, M is mutual inductance of the motor winding/phase. PMBLDCM has no neutral connection, therefore,

ia + ib + ic = 0 (19)

From Eqs. (13-22) the voltage (vno) between the neutral point (n) and the mid-point of the DC link (o) is given as,
vno = {vao +vbo + vco - (ean +ebn +ecn)}/3 (20)

From Eqs. (13-19), the flux linkages are given as,

λa = (Ls+M) ia, λb = (Ls+M) ib, λc = (Ls+M) ic (21)

6. Performance Evaluation of the Proposed PMBLDCM Drive

The proposed PMBLDCM drive is modeled in Matlab- Simulink environment and evaluated for an air conditioning compressor load. The compressor behaves as a constant torque load equal to the rated torque with speed control to match air conditioning system requirements. The PMBLDCM rated 3.75 kW is used to drive the compressor load of an air conditioner. Detailed data of the motor and simulation parameters are given in the Appendix. The speed of the motor is controlled effectively by controlling the DC link voltage. The performance evaluation of the proposed topology is carried out on the basis of various parameters such as total harmonic distortion (THDi). The crest factor (CF) of the current at input AC mains, displacement power factor (DPF), power factor (PF), and efficiency of

the complete drive (ηdrive) at different speeds of the motor. Moreover, these parameters are also evaluated for variable input AC voltage at a constant DC link voltage of 245 V, which is equivalent to the 1500 rpm reference speed of the PMBLDCM. The results are shown in Figs. 4- 9 and Tables 3-4 to demonstrate the effectiveness of the proposed PMBLDCM drive in a wide range of speed and input AC voltage. The comparison of results obtained from conventional topology (Figs. 1a and b) and the proposed buck bridge PFC topology (Figs. 7-9) demonstrates improvement of the PQ indices for the same PMBLDCMD under various operating conditions.

6.1 Performance during Starting

The performance of the proposed PMBLDCM drive fed from 220 V AC mains during starting at a rated torque and 1000 rpm speed is shown in Fig. 4a. A voltage rate limiter of 800 V/s is introduced in the reference voltage to limit the starting current of the motor and the charging current of the DC link capacitor. Therefore, the voltage controller closely tracks the reference voltage ramp, and the motor
attains reference speed smoothly within 0.8 sec while keeping the stator current within the desired limits, i.e., double the rated value. The current (is) waveform at input AC mains is in-phase with the supply voltage (vs), demonstrating near unity power factor during the starting period.

6.2 Performance under Speed Control

Figs. 3-5 show the performance of the proposed PMBLDCM drive under speed control at a constant rated torque (23.87 Nm) and 220 V AC mains supply voltage. These results are categorized as performance during transient and steady state conditions.

A.Transient Condition: Figs. 3b-d show the performance of the drive during speed control of the compressor. The reference speed is changed from 1000 rpm to 1500 rpm for the rated load performance of the compressor; from 1000 rpm to 750 rpm for the compressor at half the rated load; and from 750 rpm to 300 rpm for the compressor at light load. Speed control is fast and smooth in either direction, i.e., acceleration or retardation. Moreover, the stator current of PMBLDCM is within the allowed limit (twice the rated current) due to the introduction of a rate limiter in the reference voltage. Moreover, near unity power factor is maintained by the drive during these transient conditions.
B.Steady State Condition: The speed control of the PMBLDCM driven compressor under steady state condition is carried out for different speeds and the results are shown in Figs. 4-5 and Table-II to demonstrate the effectiveness of the proposed drive in wide speed range. Figs.4a-c show voltage (vs) and current (is) waveforms at AC mains, DC link voltage (Vdc), speed of the motor (N), developed electromagnetic torque of the motor (Te), the stator current of the PMBLDC motor for phase „a‟ (Ia), and shaft power output (Po) at 300 rpm, 900 rpm and 1500 rpm speeds. Fig. 5a shows linear relation between motor speed and DC link voltage. Since the reference speed is decided by the reference voltage at DC link, it is observed that the control of the reference DC link voltage controls the speed of the motor instantaneously. Fig. 5b shows the improved efficiency of the drive system (ηdrive) in wide range of the motor speed.

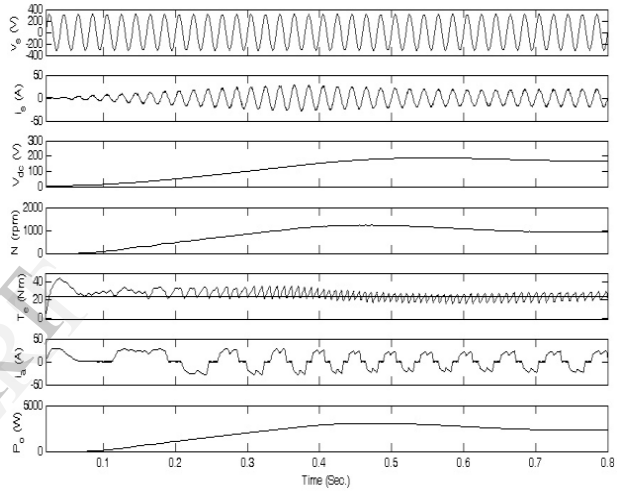

Fig: 3a. Starting performance of the PMBLDCM drive at 1000 rpm

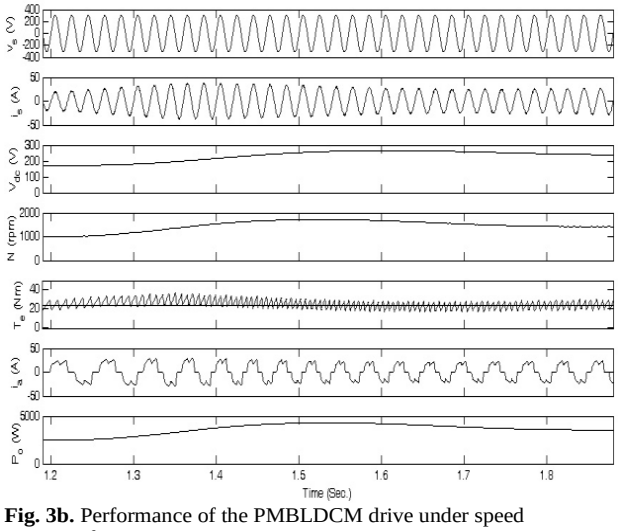

Fig. 3b. Performance of the PMBLDCM drive under speed variation from 1000 rpm to 1500 rpm

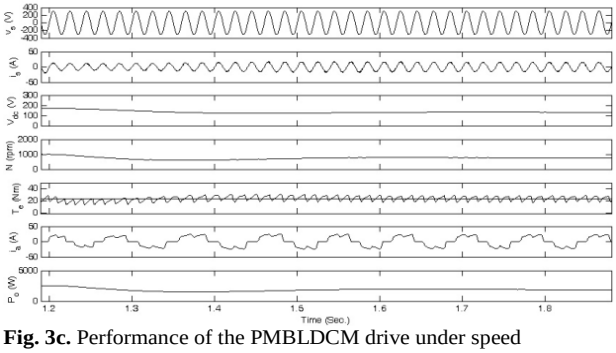

Fig. 3c. Performance of the PMBLDCM drive under speed variation from 1500 rpm to 750 rpm

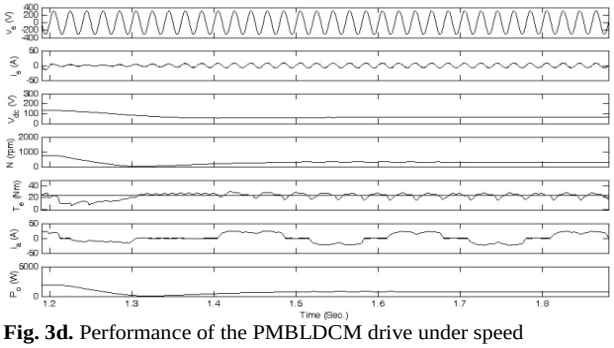

Fig. 3d. Performance of the PMBLDCM drive under speed variation from 750 rpm to 300 rpm

Fig. 3. Performance of the PMBLDCM drive under speed variation at 220 VAC input

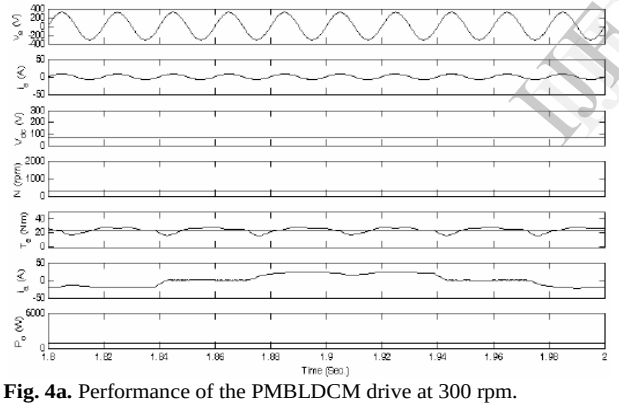

Fig. 4a. Performance of the PMBLDCM drive at 300 rpm.

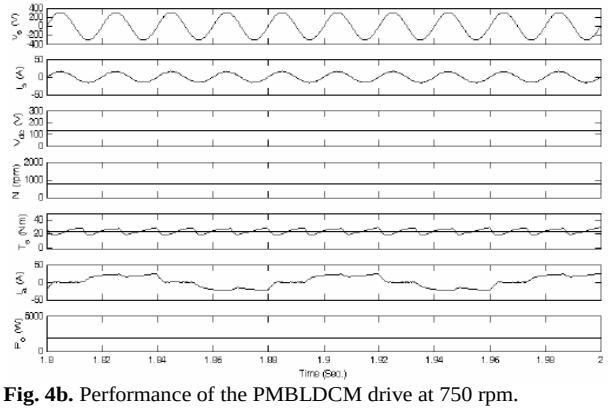

Fig. 4b. Performance of the PMBLDCM drive at 750 rpm.

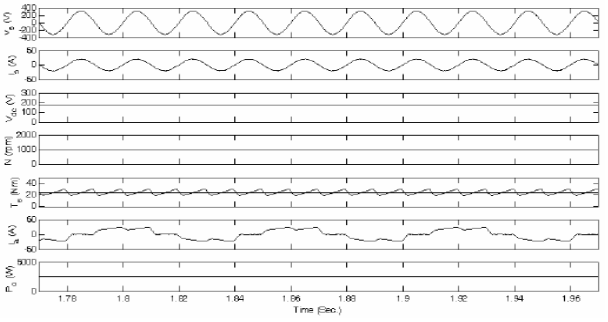

Fig. 4c. Performance of the PMBLDCM drive at 1000 rpm.

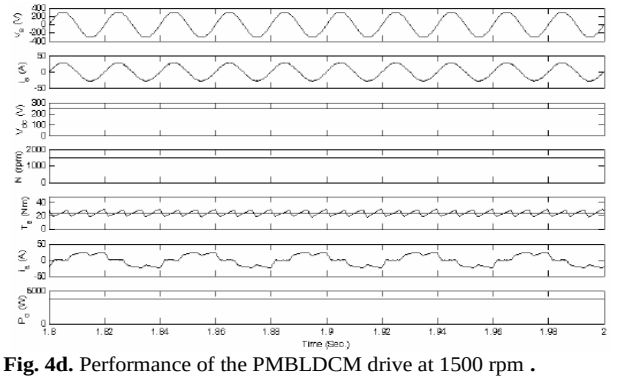

Fig. 4d. Performance of the PMBLDCM drive at 1500 rpm **.**

Fig. 4. Performance of the PMBLDCMD under the steady state condition at 220 VAC input.

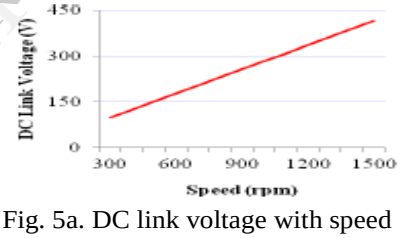

Fig. 5a. DC link voltage with speed

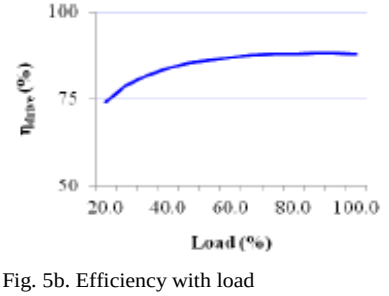

Fig. 5b. Efficiency with load

Figure 5. Performance of the proposed PFC drive under speed control at rated torque and 220 VAC

6.3 Power Quality Performance

The performance of the proposed PMBLDCM drive in terms of various PQ parameters such as THDi, CF, DPF, PF is summarized in Table-II and shown in Figs. 7-8. Nearly unity power factor (PF) and reduced THD of AC mains current are observed in wide speed range of the PMBLDCM as

shown in Figs. 7a-b. The THD of AC mains current remains less than 5% along with nearly unity PF in wide range of speed as well as load as shown in Table-II and Figs. 8a-c.

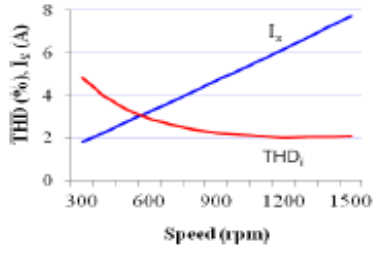

Fig. 6a. THD of current at AC mains

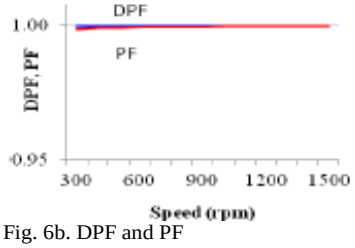

Fig. 6b. DPF and PF

Figure 6. PQ parameters of PMBLDCM drive under speed control at rated torque and 220 VAC input

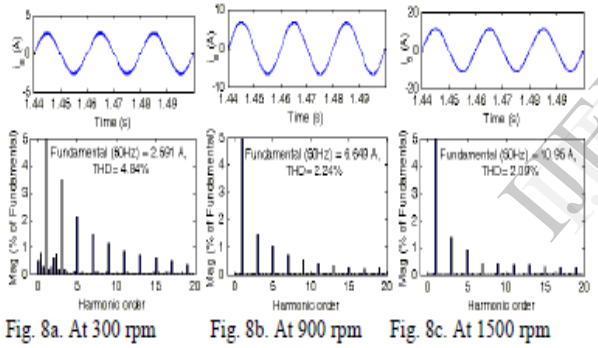

Fig. 8a. At 300 rpm Fig. 8b. At 900 rpm Fig. 8c. At 1500 rpm

Figure 7. Current waveform at AC mains and its harmonic spectra of the PMBLDCM drive under steady state condition at rated torque and 220 VAC

TABLE II
PERFORMANCE OF DRIVE UNDER SPEED CONTROL AT 220 V AC INPUT

Speed (rpm)	V_{DC} (V)	THD_i (%)	DPF	PF	η_{drive} (%)	Load (%)
300	100	4.84	0.9999	0.9987	74.2	20.0
400	126	3.94	0.9999	0.9991	79.1	26.7
500	153	3.33	0.9999	0.9993	81.8	33.3
600	179	2.92	0.9999	0.9995	83.8	40.0
700	205	2.63	0.9999	0.9996	85.3	46.6
800	232	2.40	0.9999	0.9996	86.1	53.3
900	258	2.24	0.9999	0.9996	87.0	60.0
1000	284	2.16	0.9999	0.9997	87.6	66.6
1100	310	2.09	0.9999	0.9997	88.1	73.3
1200	337	2.03	0.9999	0.9997	88.1	80.0
1300	363	2.05	0.9999	0.9997	88.2	86.6
1400	390	2.07	0.9999	0.9997	88.1	93.3
1500	416	2.09	0.9999	0.9997	88.1	100.0

6.4 Performance under Variable Input AC Voltage

Performance evaluation of the proposed PMBLDCM drive is carried out under varying input AC voltage at rated load (i.e. rated torque and rated speed) to demonstrate the operation of proposed PMBLDCM drive for air conditioning system in various practical situations as summarized in Table-III.

TABLE III
VARIATION OF PQ PARAMETERS WITH INPUT AC VOLTAGE (VS) AT 1500 RPM (416 VDC)

V_{AC} (V)	THD_i (%)	DPF	PF	CF	I_s (A)	η_{drive} (%)
170	2.88	0.9999	0.9995	1.41	10.4	84.9
180	2.59	0.9999	0.9996	1.41	9.7	85.8
190	2.40	0.9999	0.9996	1.41	9.2	86.3
200	2.26	0.9999	0.9996	1.41	8.6	87.2
210	2.14	0.9999	0.9997	1.41	8.2	87.6
220	2.09	0.9999	0.9997	1.41	7.7	88.1
230	2.07	0.9999	0.9997	1.41	7.4	88.2
240	2.02	1.0000	0.9998	1.41	7.1	88.4
250	1.99	1.0000	0.9998	1.41	6.8	88.7
260	2.01	1.0000	0.9998	1.41	6.5	88.7
270	2.01	1.0000	0.9998	1.41	6.2	89.0

Figs. 8a-b show variation of input current and its THD at AC mains, DPF and PF with AC input voltage. The THD of current at AC mains is within specified limits of international norms along with nearly unity power factor in wide range of AC input voltage.

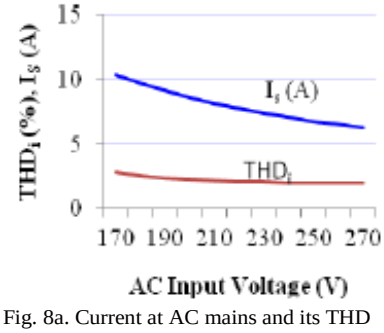

Fig. 8a. Current at AC mains and its THD

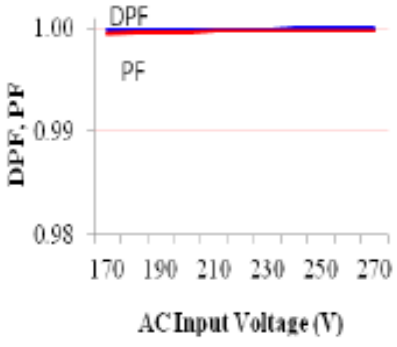

Fig. 8b. DPF and PF

Figure 8. PQ parameters with input AC voltage at 416 VDC (1500 rpm)

7. Conclusion

A new speed control strategy of a PMBLDCM drive is validated for a compressor load of an air conditioner which uses the reference speed as an equivalent reference voltage at DC link. The speed control is directly proportional to the voltage control at DC link. The rate limiter introduced in the reference voltage at DC link effectively limits the motor current within the desired value during the transient condition (starting and speed control). The additional PFC feature to the proposed drive ensures nearly unity PF in wide range of speed and input AC voltage. Moreover, power quality parameters of the proposed PMBLDCM drive are in conformity to an International standard IEC 61000-3-2 [5]. The proposed drive has demonstrated good speed control with energy efficient operation of the drive system in the wide range of speed and input AC voltage. The proposed drive has been found as a promising candidate for a PMBLDCM driving Air-Con load in 1-2 kW power range.

APPENDIX

Rated Power: 1.5 kW, rated speed: 1500 rpm, rated current: 4.0 A, rated torque: 9.55 Nm, number of poles: 4, stator resistance (R): 2.8 Ω/ph., inductance (L+M): 5.21 mH/ph., back EMF constant (Kb): 0.615 Vsec/rad, inertia (J): 0.013 Kg-m2. Source impedance (Zs): 0.03 pu, switching frequency of PFC switch (fs) = 40 kHz, capacitors (C1= C2): 15nF, PI speed controller gains (Kp): 0.145, (Ki): 1.45.

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