Address Generation Based WIMAX Deinterleaver using FPGA

Praveena K
Assistant professor

P. Aparna
Associate Professor

Bhavani V
Assistant professor

Electronics and communication
MVJ CE ,Bangalore

Abstract

The paper reports the implementation of address generator of the 2-D deinterleaver used in wimax transreceiver system using FPGA. The bit streams in channel interleaver and deinterleaver for IEEE 802.16e standard associated with floor function is very difficult to implement on the FPGA kit. But by using this proposed algorithm eliminates the requirement of floor function and it also reduces the complexity in the FPGA implementation. In this paper presents a novel and highly efficient Quadrature Phase Shift Keying(QPSK), 16-QAM, 64-QAM sharing resources and these are novel and highly efficient compared with conventional Look-Up-Table (LUT) based approach.

Index Terms— WiMAX, IEEE 802.16e standard, Wireless system, Look-Up-table, Field Programmable gate Arrays(FPGA).

I. INTRODUCTION

Broadband wireless access (BWA) systems have evolved as the solution for the persistent demand of these multimedia services [1]. It provides enhancement in multimedia data services and quality of service (QoS). It support simultaneous voice, data and multimedia services to a large group of subscribers without the need for digital subscriber line (DSL) or cable modem. WLAN and WiMAX are emerging standards for wireless broadband communication system.

IEEE 802.16 is a solution to broadband wireless access (BWA) commonly known as Worldwide Interoperability for Microwave Access (WiMAX),is a recent wireless broadband standard that has promised high bandwidth over long-range transmission[1]. WiMAX is an emerging industry consortium standard for wireless broadband networking. It is based on wireless metropolitan area networking (WMAN) standards. It offers a rich set of features with a lot of flexibility in terms of deployment options and potential service offerings. The WiMAX physical layer (PHY) is based on orthogonal frequency division multiplexing which offers good resistance to multipath and allows WiMAX to operate in Non Line of Site (NLOS) conditions.

The direct implementation of interleaver/deinterleaver functions in WiMAX is not hardware efficient due to presence of complex functions. Also the conventional method i.e. using memories for storing the permutation tables is silicon consuming. This work presents a 2-D transformation for WiMAX channel interleaver/deinterleaver functions which reduces the overall hardware complexity to compute the deinterleaver addresses and also eliminates the requirement of floor function is proposed[6].

WiMAX implemented on FPGA can easily be upgraded by making necessary changes in the Hardware Description Language (HDL) code. In addition FPGA based circuit is much shorter compared to Application Specific Integrated Circuit (ASIC). Design flexibility is another important advantage of FPGA based implementation.

In this brief, use of FPGA's embedded multiplier provides performance improvement by reducing interconnection delay, efficient resource utilization, and lesser power consumption compared with a configurable logic block-based multiplier. Our work shows betterment over the LUT technique to the tune of approximately 49% in terms of maximum operating frequency.

Section II Describes the related works. Section III explains system description. Section IV, explains the interleaving technique of the WiMAX system. In Section V, a proposed algorithm for 2-D dein-terleaver address generator along with its mathematical back-ground is presented. Transformation of the algorithm into hardware architecture is discussed in Section VI. Section VII, shows the simulation result and Section VIII reports the FPGA implementation result. Finally, this brief is concluded in Section VIII.

II. RELATED WORKS

Very few works related to hardware implementation of the interleaver/deinterleaver used in a WiMAX system is available in the literature. The work in [3] demonstrates the grouping of incoming data streams into the block to reduce the frequency of memory access in a deinterleaver using a conventional look-up table (LUT)-based CMOS address generator for WiMAX. Khater et al.[4] has described a hardware description language (VHDL)- based implementation of address generator for IEEE 802.16e channel interleaver with only a 1/2 code rate. In [5], the authors have described a finite-state machine (FSM)-based address generator of the same interleaver for all permissible code rates and modulation schemes. Both [4] and [5] are tested on the field-programmable gate array (FPGA) plat-form. Asghar and Liu in [6] has made 2-D translation of the functions used in WiMAX channel deinterleaver to claim efficient hardware architecture. However, the derivations in[6] do not clearly explain the design issues, particularly for 64-quadrature-amplitude modulation (QAM).

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Hardware implementation of floor function is very complex and consumes abnormally large amount of resources [6]. Conventional LUT-based technique is found to be unattractive from many aspects such as slowness in operation, consumption of large logic resources leading to inefficiency in resource utilization, etc.

This paper proposes the friendly mathematical expressions[6] and subsequent algorithm for the 16-QAM and 64-QAM compared with the complicated and lengthy expressions.

III. SYSTEM DESCRIPTION

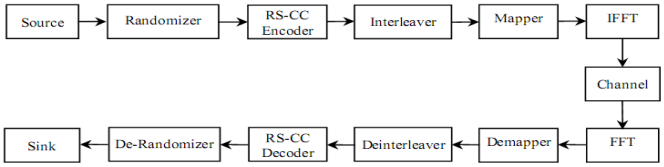

Fig. 1. Block diagram of the WiMAX transreceiver

The system level overview of IEEE 802.16e based WiMAX system is described in Fig.1. In this system, the input binary data stream obtained from a source is randomized to prevent a long sequence of 1s and 0s, which will cause timing recovery problem at the receiver. Psuedo Random Binary Sequence (PRBS) is used in which randomization is done by modulo 2 addition of the data with the output of the PBRS itself [5]. The randomized data bits are there after encoded using Reed Solomon (RS) encoder followed by Convolutional Coder (CC). The former is suitable for correction of burst type of error whereas the later is for random error. After RS-CC encoding all encoded data bits shall be interleaved by a block interleaver. In traditional block interleaver bits received from the encoder are stored row wise in the interleaver's memory. As soon as the memory is completely filled, the bits are read column by column manner [5]. In the block interleaver of WiMAX system, data is written in the memory in a predefined manner based on certain permutation and read in a sequential manner. After interleaving, data passes through the mapper block in which modulation takes place. The resulting data symbols are used to construct one OFDM symbol by performing Inverse Fast Fourier Transform (IFFT). Cyclic Prefix (CP) is used to reduce ISI and ICI.

In the receiver, inverse blocks are applied which perform FFT,de-mapping, deinterleaving, decoding and de-randomizing operations in sequential manner to get back the original data bits.

IV. INTERLEAVING IN WIMAX SYSTEM

Two-dimensional block interleaver/deinterleaver structure, which is used as a channel interleaver/deinterleaver in the WiMAX system, is described in Fig. 2. It has two memory blocks, namely, M-1/2 and an address generator. In The block interleaver/deinterleaver exploits different depths Ncbps to incorporate various code rates and modulation schemes (see Table I) for IEEE 802.16e [7]. The data stream received from the RS-CC encoder is permuted by using the two-step processes described by (1) and (2).

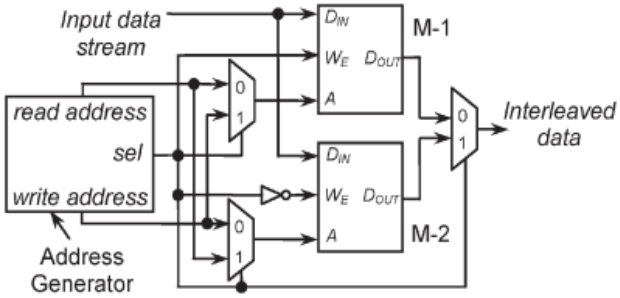

Fig. 2. Block diagram of interleaver/deinterleaver

block interleaving, when one memory block is being written, the other one is read, and vice versa. When sel =1, write-enabled signal WE of M-1 is active. During this period, the input data stream is written in M-1 as it receives the write addresses. Simultaneously, an interleaved data stream is read from M-2 as it is supplied with the read addresses. After the memory blocks are written/read up to the desired location as specified by interleaver depth, the status of sel signal is changed to swap the read/write operation.

TABLE 1
PERMITTED INTERLEAVER / DEINTERLEAVER DEPTH IN IEEE 802.16e FOR ALL CODE RATES AND MODULATION TYPES

Modulation Scheme	QPSK (s=1)		16-QAM (s=2)		64-QAM (s=3)		
Code Rate	½	¾	½	¾	½	⅔	¾
Interleaver Depth, N_{cbps} in bits	96	144	192	288	288	384	432
	192	288	384	576	576	-	-
	288	432	576	-	-	-	-
	384	576	-	-	-	-	-
	480	-	-	-	-	-	-
	576	-	-	-	-	-	-

These steps ensure mapping of coded bits onto nonadjacent subcarriers and alternate less/more significant bits of the modulation constellation ,respectively. Thus,

$$m_k = \left(\frac{N_{\text{cbps}}}{d}\right) \cdot (k \% d) + \left\lfloor \frac{k}{d} \right\rfloor \quad (1)$$

$$j_k = s \cdot \left\lfloor \frac{m_k}{s} \right\rfloor + \left(m_k + N_{\text{cbps}} - \left\lfloor \frac{d.m_k}{N_{\text{cbps}}} \right\rfloor \right) \% s. \quad (2)$$

where % and [ ] signify modulo and floor functions respectively. The deinterleaver, which performs the inverse operation, is also defined by two permutations, i.e., (3) and (4). Let mj and kj define the first and second level of permutations for the deinterleaver, where j is the index of received bits within a block of Ncbps bits. As per [10], (3) and

(4) perform inverse operation of (2) and (1), respectively. Thus the equation becomes,

$$m_j = s \cdot \left\lfloor \frac{j}{s} \right\rfloor + \left(j + \left\lfloor \frac{d.j}{N_{\text{cbps}}} \right\rfloor \right) \% s \quad (3)$$

$$k_j = d.m_j - (N_{\text{cbps}} - 1) \cdot \left\lfloor \frac{d.m_j}{N_{\text{cbps}}} \right\rfloor . \quad (4)$$

V. DE-INTERLEAVING ALGORITHM IN THE WIMAX SYSTEM

The proposed algorithm for address generator of the WiMAX deinterleaver along with its mathematical background has been described. A MATLAB program is developed using (3) and (4) for all modulation schemes and code rates. Due to the presence of a floor function in (3) and (4), their direct implementation on an FPGA chip is not feasible. Table II shows the deinterleaver addresses for the first four rows and five columns of each modulation type. As d =16 is chosen, the number of rows are fixed (= d) for all Ncbps, whereas the number of columns are given by Ncbps/d.

TABLE II
FIRST FOUR ROWS AND FIVE COLUMNS OF DEINTERLEAVER SAMPLE ADDRESSES FOR THREE CODE RATES AND MODULATION TYPES.

N_{cbps}, code rate and modulation type	De-interleaver addresses				
N_{cbps} = 96-bits, ½ code rate, QPSK	0	16	32	48	64
	1	17	33	49	65
	2	18	34	50	66
	3	19	35	51	67
N_{cbps} = 192-bits, ½ code rate, 16-QAM	0	16	32	48	64
	17	1	49	33	81
	2	18	34	50	66
	19	3	51	35	83
N_{cbps} = 576-bits, ¾ code rate, 64-QAM	0	16	32	48	64
	17	33	1	65	81
	34	2	18	82	50
	3	19	35	51	67

A close examination of the addresses in Table II reveals that the correlation between them follows the manner, as shown in Table III. The mathematical foundation of the correlation between the addresses, as derived in this brief, is represented by (5)–(7),
where j =0, 1,...,d-1 and i =0, 1,..., (Ncbps/d) – 1 represent the row and column numbers, respectively, in Table III. In addition, kn represents the deinterleaver addresses.
General validity of (5)–(7) to represent the correlation between addresses of Table III has formally been proven using the algebraic analysis in [6], which lacks the involvement of (5)–(7). The outcome of this analysis using (5)–(7) provides the same result, as shown in Table III. Thus, (5)–(7) play the pivotal role in establishing formal mathematical foundation of our proposed algorithm. From Table III and the mathematical representation by (5)–(7), following three algorithms for the three modulation schemes are proposed. These algorithms eliminate the require-ment of floor function while generating write addresses. These algorithms are also tested on MATLAB. Results obtained are verified with the previous MATLAB program for all code rates and modulation schemes of the WiMAX deinterleaver.

$$k_{n,\text{QPSK}} = \{ d * i + j \quad \text{for } \forall\, j \text{ and } \forall\, i \quad (5)$$

$$k_{n,16\text{-QAM}} = \begin{cases} d*i+j & \text{for } j\%2 = 0 \text{ and for } \forall\, i \\ d*(i+1)+j & \text{for } j\%2 = 1 \text{ and} \\ & \text{for } i\%2 = 0 \\ d*(i-1)+j & \text{for } j\%2 = 1 \text{ and} \\ & \text{for } i\%2 = 1 \end{cases} \quad (6)$$

$$k_{n,64\text{-QAM}} = \begin{cases} d*i+j & \text{for } j\%3 = 0 \text{ and for } \forall\, i \\ d*(i-2)+j & \text{for } j\%3 = 1 \text{ and} \\ & \text{for } i\%3 = 2 \\ d*(i+1)+j & \text{for } j\%3 = 1 \text{ and} \\ & \text{for } i\%3 \neq 2 \\ d*(i+2)+j & \text{for } j\%3 = 2 \text{ and} \\ & \text{for } i\%3 = 0 \\ d*(i-1)+j & \text{for } j\%3 = 2 \text{ and} \\ & \text{for } i\%3 \neq 0 \end{cases} \quad (7)$$

Table III
DETERMINATION OF CORRELATION BETWEEN ADDRESSES

Row no.(j)	Column no. (i) →	0	1	2	3	4
0	N_{cbps} = 96-bits, ½ code rate, QPSK	d.0+0=0	d.1+0=16	d.2+0=32	d.3+0=48	d.4+0=64
1		d.0+1=1	d.1+1=17	d.2+1=33	d.3+1=49	d.4+1=65
2		d.0+2=2	d.1+2=18	d.2+2=34	d.3+2=50	d.4+2=66
3		d.0+3=3	d.1+3=19	d.2+3=35	d.3+3=51	d.4+3=67
0	N_{cbps} = 192-bits, ½ code rate, 16-QAM	d.0+0=0	d.1+0=16	d.2+0=32	d.3+0=48	d.4+0=64
1		d.1+1=17	d.0+1=1	d.3+1=49	d.2+1=33	d.5+1=81
2		d.0+2=2	d.1+2=18	d.2+2=34	d.3+2=50	d.4+2=66
3		d.1+3=19	d.0+3=3	d.3+3=51	d.2+3=35	d.5+3=83
0	N_{cbps} = 576-bits, ¾ code rate, 64-QAM	d.0+0=0	d.1+0=16	d.2+0=32	d.3+0=48	d.4+0=64
1		d.1+1=17	d.2+1=33	d.0+1=1	d.4+1=65	d.5+1=81
2		d.2+2=34	d.0+2=2	d.1+2=18	d.5+2=82	d.3+2=50
3		d.0+3=3	d.1+3=19	d.2+3=35	d.3+3=51	d.4+3=67

VI. ARCHITECTURE OF THE DE-INTERLEAVER ADDRESS GENERATOR

The top-level structure of the deinterleaver address generator is shown in Fig. 3. Logic circuits presented here are QPSK block,16-QAM block, and 64-QAM block,

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respectively. Our design is optimized in the sense that common logic circuits such as multiplier, adder, row counter, and column counter are shared while generating addresses for any modulation type. In addition, the design also shares the incrementer and the decrementer required in 16-QAM and 64-QAM blocks.

Fig 4 represents the simulation results for 64 QAM for the code rate ¾ and Ncbps=576 bits using modelsim XE-III.

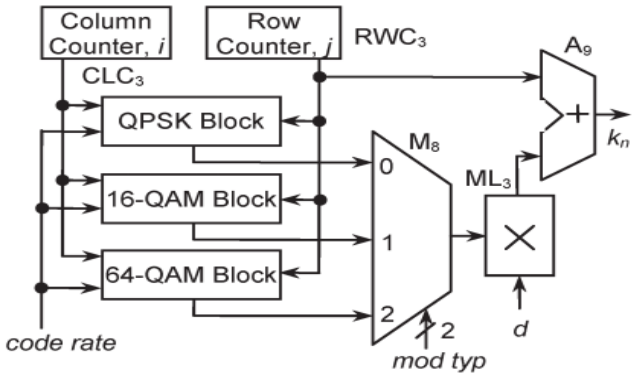

Fig. 3. complete deinterleaver address generator

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VII. CONCLUSION

This brief has proposed a novel algorithm along with its mathematical formulation, including proof for address generation circuitry of the WiMAX channel deinterleaver supporting all possible code rates and modulation patterns as per IEEE 802.16e. The proposed algorithm is converted into an optimized digital hardware circuit. The hardware is implemented on the Xilinx FPGA using VHDL. Comparison of our proposed work with a conventional LUT-based method and also with a recent work show significant improvement on resource utilization and operating frequency.

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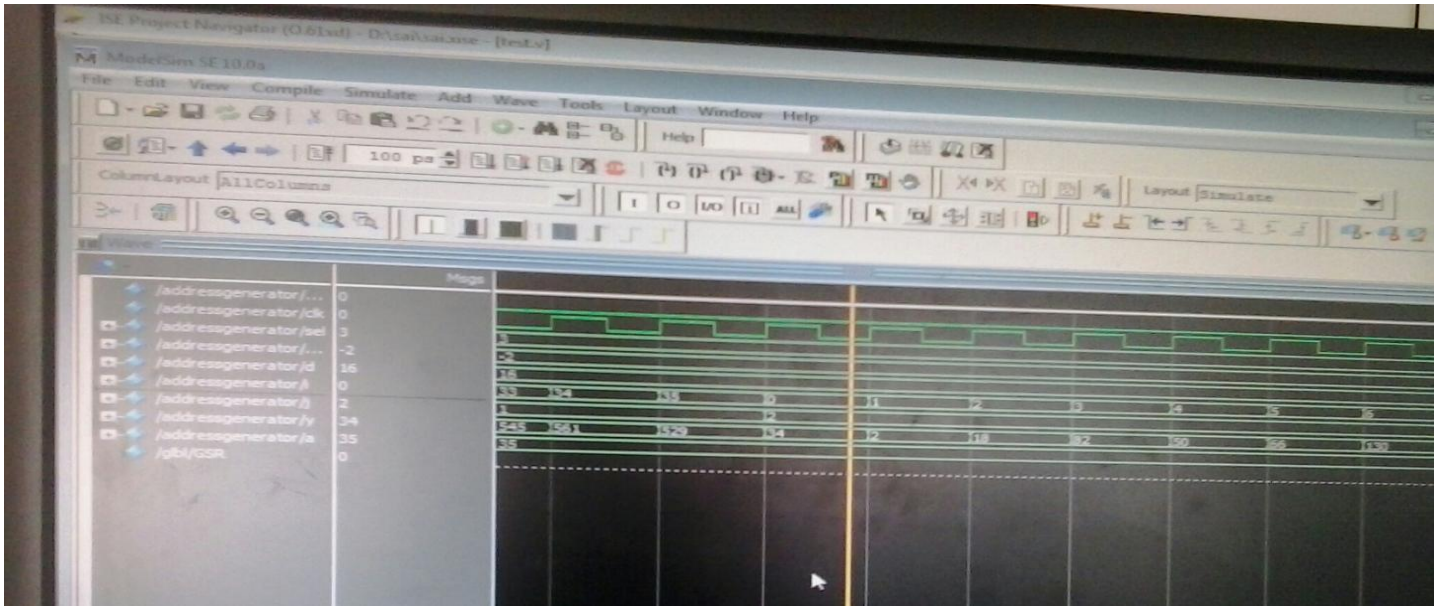

Fig: 4.simulation result 64QAM with Ncbps=576 bits and ¾ code rate

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