Adaptive Thresholding for Image Enhancement : Hardware Approach

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***Abstract*—Objects are extracted from background by thresholding. This needs correct selection of threshold value as single value of threshold will not give proper separation in all the images. Hence adaptive threshold method is chosen.In this work, the threshold value is chosen automatically by using weight updating algorithm. Thresholding leads to binarization of image. This technique is mainly applicable for bimodal images (images which contain two dominant peaks in histogram).It is implemented on FPGA platform using VHDL language and results are presented using simulation and implementation on hardware which are based on fixed point data types and give accurate threshold value.**

***Keywords*-Adaptive Thresholding, FPGA, Hardware design languages, VHDL.**

I. INTRODUCTION

The principal objective of Thresholding is to separate objects from its background in which all gray levels below the threshold value are considered as part of background and mapped into black pixel and those levels above the threshold value are considered as part of object or foreground and mapped into white pixel or vice versa .In this paper threshold value is automatically determined by using adaptive thresholding.[1]

Thresholding techniques can be categorised into three techniques. First is local thresholding, in which threshold value changes over an image, is also known as variable thresholding and threshold value at any point in an image depends on properties of neighbourhood of pixel. Second is Global thresholding, in which threshold value is constant and applicable over entire image. These thresholds an image on basis of information obtained by image histogram and third is optimum thresholding in which threshold value is chosen adaptively on the basis of histogram e.g. Otsu's method[2].

Thresholding is one of the important steps in image processing, as it not only binarizes the image but also reduces the complexity by reducing the image data. For segmentation of image, thresholding is first step in every application [3, 4].

Adaptive Thresholding of bimodal images is very useful in various applications such as document image analysis, counting objects in image, shape recognition and in image segmentation[5].

Forall applications it is not possible to utilize dedicated computer setup and image processing software like MATLAB. It is better to develop independent hardware design to give proper resource utilization and portability.The use of configurable hardware allows direct implementation of image enhancement algorithms with improved performances and reduces the computational and execution time.

The goal of this paper is to propose adaptive technique of thresholding of bimodal images, for easy extraction of features. This algorithm is simulated in Xilinx using ISE simulator and implemented on FPGA. Results of normal thresholding and adaptive thresholding are compared.

The remaining paper is organized as follows. Section II presents the overview of thresholding technique. Section III highlights implementation of proposed algorithm for thresholding. Section IV focused on experimental results. Finally, section V concludes the work.

II. THRESHOLDING TECHNIQUE

1) Threshold operation

Thresholding of image means converting gray level information of image to two-level information.In case the object in the foreground has quite different gray levels than the surrounding background, image thresholding is an effective tool for this separation, or segmentation. Threshold operation is defined using following equation where a_{th} is the threshold value which is useful to separate the pixel values in two classes.

$$F(x,y) = \begin{cases} G_0(x,y) \ for \ G(x,y) < a_{th} \\ G_1(x,y) \ for \ G(x,y) \geq a_{th} \end{cases} \quad (1)$$

By using above equation, values of each pixel from theinput image are replaced by the corresponding pixel in thedestination image using $G_0\ (x,y)$=0 and $G_1\ (x,y)$=1.

2) Adaptive Thresholding

When threshold value selected is different for different images and it is chosen based on some properties of images it is called as adaptive thresholding. A common method used to select threshold value is by analysing the histograms of images. When onlytwo dominant modesand a clear valley are present inhistogram such images are bimodal images as shown in figure no. 1.

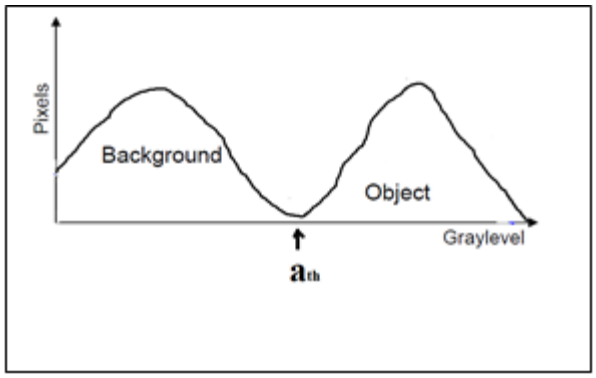


Fig..1: Histogram for Bimodal Image

In this paper the most common technique of adaptive thresholding is presented whichinvolves weight updating unit, for finding appropriate threshold value for bimodal images. Let us consider image of size [M*N] then initially two weights are assigned $\mu_1$and μ_2 then these weights are compared with each pixel values in [M*N] image.The closest weight is selected for updating the weight of every input pixel. The difference between the input pixel and the closest weight is multiply by learning rate β and added to the closest weight.If$\mu_1$is closed to that pixel value then $\mu_1$get updated and if μ_2 is closed to pixel then μ_2 gets updated by using following equation

$$\mu_{new} = \mu_{old} + \beta * (pixel - \mu_{old}) \quad (2)$$

$$where\ \mu = weight$$

$$\beta = learning\ rate$$

$$\beta = \frac{256 - pixel}{256}$$

The updated weights are applied to every pixel of image and at the end average of these two weights are taken as threshold value; it can be defined by following equation

$$a_{th} = \frac{\mu_1 + \mu_2}{2} \quad (3)$$

By using this threshold value, image can be converted into binary form. The pixel range above a_{th} value are consider as object and those are below a_{th} value are consider as background so that object can be discriminated easily. Flow chart for the weight updating process is as in figure no. 2[6,7]

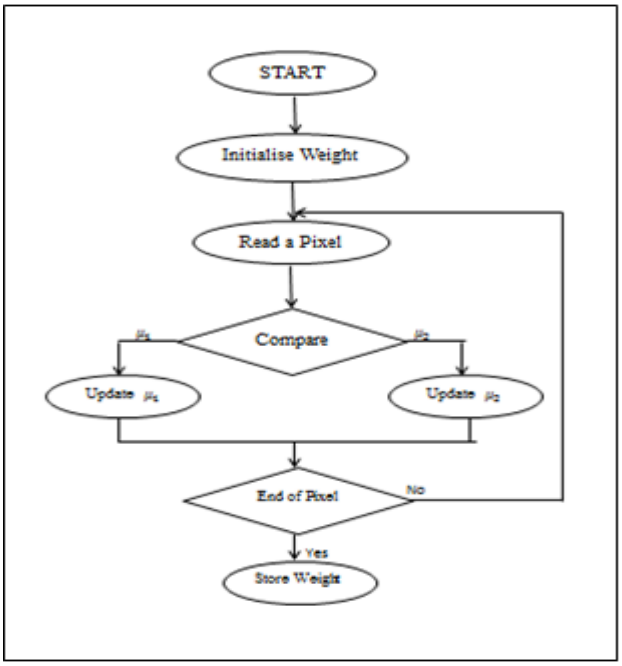


Fig.2: Flow Chart of Weight Updating Process

III. IMPLEMENTATION OF ADAPTIVE THRESHOLDING

The generalised block diagram of a proposed system is as shown in Fig.3. It consists of main three blocks one is ROM memory to store the input image then adaptive thresholding block and third is transmitter to transmit the data serially and then output image can be verified using MATLAB by using serial command.

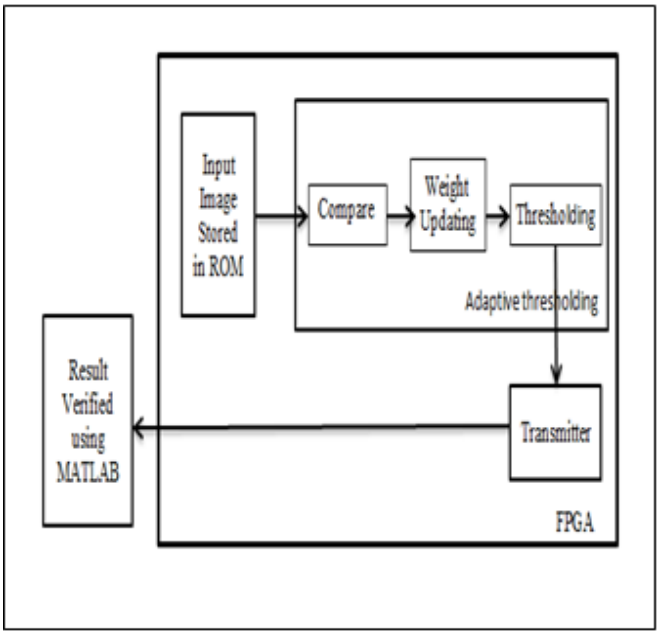


Fig.3: Generalised Block Diagram of Proposed System

1) ROM IP Core (Block Memory Generator)

The IP Core (Intellectual property Core) refers to preconfigured logic functions that can be used in design. Xilinx provides a wide selection of IP that is optimized for Xilinx FPGAs. The CORE Generator System creates customized cores which delivers high levels of performance and area efficiency. In this work , To store the input image block ROM IP core is used, the size of image in this proposed algorithm is 128*128.because of use of this IP core area can be optimized and increase the performance.

2) Adaptive Thresholding Block

This block is designed by VHDL language using fixed point data type for obtaining accurate value of threshold. Two weights are initialized at value 120 and 100 then each pixel value is compare with two weights. For finding the closest weight, absolute difference between pixel value and weights are calculated. Then result of compare unit is given to the weight updating block and closest weight gets updated using weight updating equation. After updating the weights for all pixel values, the average of two weights are calculated which is used as threshold value given to the thresholding block. In threshold block the pixel values above threshold value is assigned as white pixel and those are below threshold value is assigned as black pixel, for differentiating object from the background[6,7].

3) Transmitter Block

Universal asynchronous receiver and transmitter (UART) is common protocol used for the serial communication from external hardware to PC. UART is three main modules:the baud rate generator,receiver module and transmitter module. The baud rate generator is used to set the baud rate to control the UART receive and transmit. The UART receiver module is used to receive the data serially, and convert them into parallel data. The UART transmit module transmits data serially.Ten bits of data is consists of one start bit, 8 bit data bits and one stop bit.The transmission starts with a start bit, which is '0', followed by data bits and an optional parity bit, and ends with stop bits, which are '1'. In this proposed work only baud generator and transmit module is used to transfer the data from FPGA to PC[8].

The complete RTL schematic of presented in fig:3 consists of mainly four blocks, ROM IP block, thresholding block which consists of weight update block and threshold unit, controller for controlling whole operation and transmitter to transmit data serially to the PC.Each block is designed separately using VHDL and all the four blocks arebrought in single top module to work together.

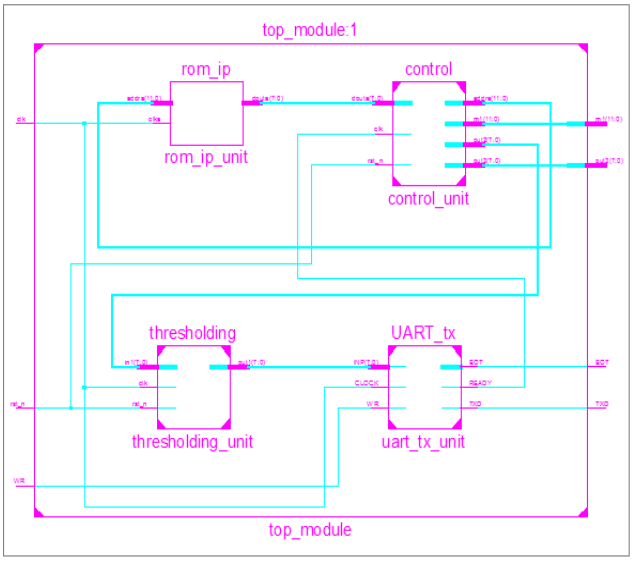


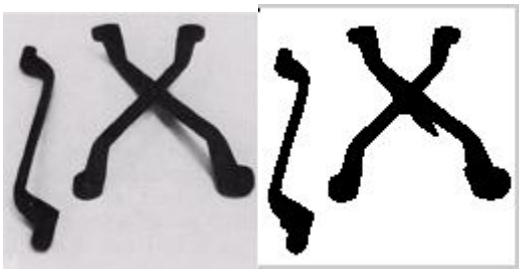
Fig.4:RTL Schematic

III. EXPERIMENTAL RESULTS

For hardware-based implementation Spartan 3E family of FPGAs is used. The software development tool used for developing and verifying the design is the Xilinx's ISE 14.2-version. The image size considered for testing is a 128 x 128 pixel resolution gray-level image. As fixed point data type is used for adaptive thresholding results are more accurate. The proposed algorithm is tested using bimodal images as shown in figure:5.

The Logical consumption in FPGA is given in Table 1 the proposed design is simple and memory efficient as compared to the design in reference no.3 and utilization summary is described in figure 6.

Original Image Result Of Adaptive Thresholding



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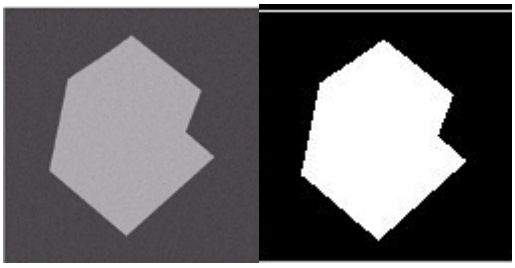

Original Image Result Of Adaptive Thresholding

Fig.5: Result Of Proposed method

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	109	9,312	1%
Number of 4 input LUTs	220	9,312	2%
Number of occupied Slices	158	4,656	3%
Number of Slices containing only related logic	158	158	100%
Number of Slices containing unrelated logic	0	158	0%
Total Number of 4 input LUTs	248	9,312	2%
Number used as logic	210		
Number used as a route-thru	28		
Number used as Shift registers	10		
Number of bonded IOBs	25	232	10%
IOB Flip Flops	8		
Number of RAMB16s	2	20	10%
Number of BUFGMUXs	2	24	8%
Number of MULT18X18SIOs	1	20	5%
Average Fanout of Non-Clock Nets	2.83		

Fig.6-Device Utilization Summary

TABLE 1 : LOGIC CONSUMPTION IN FPGA

Name	Description	Numbers
IOs	----------	27
Registers	Macro	14
Multiplexer	Macro	1
Adders/Subtractors	Macro	10
Comparators	Macro	3
BELS	Cell	465
Flip Flop /Latches	Cell	121
Clock Buffer	Cell	2
IO Buffers	Cell	26

IV. CONCLUSION

The main aim of this proposed work is to implement simple and portablehardware system for adaptive thresholding ofbimodal images, such as fingerprint image.As per figure 6 the proposed design is simple because device utilization is less. Threshold value is calculated accurately as fixed point data type is used which is clearly shown by output images. The proposed design is tested using simulation andall the results are obtained by implementing proposed system onhardware Spartan 3E and resultant images are analysed by using MATLAB.

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