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Adaptive PI controller based Multi Converter Unified Power-Quality Conditioning System (MC-UPQC)

[1]Bora Trinadha Reddy
[1] P.G. Student,
Department of EEE,
AITAM Engineering College,
Andhra Pradesh, India.

[2]Mouliswararao Reddy
[2]Asst. Professor,
Department of EEE,
AITAM Engineering College,
Andhra Pradesh, India.

***Abstract*:- This paper presents a Multiconverter Unified Power Quality Conditioning (MC-UPQC) system in which the voltage and current compensation in multi-bus/feeder systems can be done simultaneously. The configuration consists of one shunt voltage source converter (VSC) and two/more series VSCs. And all connectors are coupled end-to-end on the dc side, sharing a common dc link capacitor. Thus the power transmission occurs from one feeder to adjacent feeders compensating sag, swell and any interruption. In order to compensate for imperfections at supply voltage and load current on the main feeder, the system can be applied to adjacent feeders. This also allows the full compensation of imperfections at supply voltage present on the remaining feeders. The simulation is done using Matlab/Simulink environment that illustrates the performance of MC-UPQC and the control algorithm. The simulation results of two bus/ two feeder system exhibits the efficiency of the proposed configuration.**

Keywords: Power quality improvement, Voltage Source Converter (VSC), Unified Power Quality Conditioner (UPQC).

I. INTRODUCTION

The growing demand in using the renewable energy sources make it desirable to control a huge amount of power that enables the power system for a quick switch between the renewable energy sources and the stand-by power generation. This demands the availability of stand-by power whenever renewable energy is unable to supply the load. Therefore the need for power flow control methods is increased. The system parameters such as line impedance, transmission angle and voltage magnitude are adjusted in order to control the power flow. The Power Flow Controlling Device (PFCD) is a device that tries to change system parameters to control the power flow. The combined Flexible AC Transmission System (FACTS) devices that overlap with the PE PFCDs are the most suitable devices for the power flow control.

Electric Power Quality (EPQ) is normally used as a reference to retain a near sinusoidal waveform of bus voltages and currents of power distribution at rated magnitude and frequency. The issues regarding power quality in the distribution networks are mentioned in the literature [1]-[6] that occur because of the high usage of critical and sensitive equipment like communication network, precise manufacturing processes, process industries etc. This equipment's performance is affected by the issues such as voltage sag, voltage harmonics, voltage swell etc which can be eliminated by FACTS devices.

The application of FACTS concepts in distribution systems has resulted in a new generation of compensating devices. A unified power-quality conditioner (UPQC) [7] is the extension of the unified power-flow controller (UPFC) [8] concept at the distribution level. It consists of combined series and shunt converters for simultaneous compensation of voltage and current imperfections in a supply feeder [9]–[11]. In recent times, multiconverter FACTS devices, such as an interline power-flow controller (IPFC) [12] and the generalized unified power-flow controller (GUPFC) [13] are introduced. An IPFC consists of two series VSCs whose dc capacitors are coupled. This allows active power to circulate between the VSCs. With this configuration, two lines can be controlled simultaneously to optimize the network utilization. The simplest GUPFC consists of three converters—one connected in shunt and the other two in series with two transmission lines in a substation. The basic GUPFC can control total five power system quantities, such as a bus voltage and independent active and reactive power flows of two lines. The aim of these devices is to control the power flow of multilines or a subnetwork rather than control the power flow of a single line as UPFC.

An interline unified power-quality conditioner (IUPQC), which is the extension of the IPFC concept at the distribution level, has been proposed in [14]. The IUPQC consists of one series and one shunt converter. It is connected between two feeders to regulate the bus voltage of one of the feeders, while regulating the voltage across a sensitive load in the other feeder. In this configuration, the voltage regulation in one of the feeders is performed by the shunt-VSC. However, since the source impedance is very low, a high amount of current would be needed to boost the bus voltage in case of a voltage sag/swell which is not feasible. It also has low dynamic performance as there is no regulation of the dc-link capacitor voltage.

In this paper, a new configuration of a UPQC called the MultiConverter Unified Power-Quality Conditioner (MC UPQC) is presented. The system is extended by adding a series-VSC in an adjacent feeder. The proposed topology is capable of simultaneous compensation of voltage and current

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imperfections in both feeders by sharing power compensation capabilities between two adjacent feeders which are not connected. The system can also be used for compensating interruptions without the need for a battery storage system and consequently without storage capacity limitations.

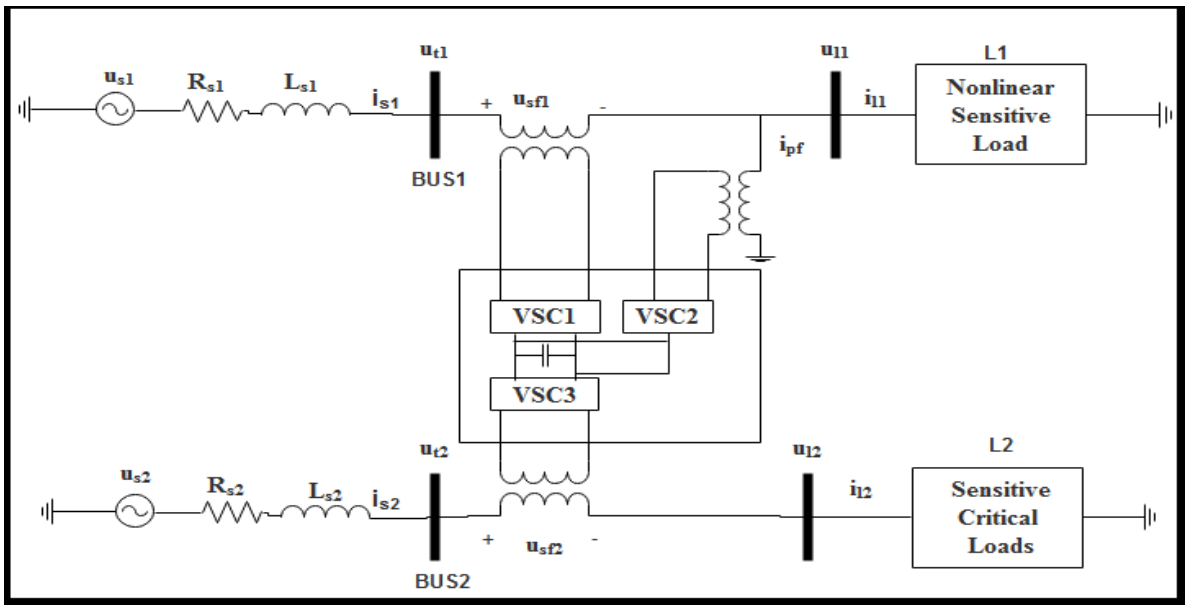

Fig. 1. Typical MC-UPQC used in a distribution system.

II. PROPOSED MC-UPQC SYSTEM

The MC–UPQC system's structure comprises three Voltage source Converters (VSC) named VSC1, VSC2 and VSC3, connected end to end via a common dc-link capacitor. Each of these VSCs is comprehended by a three-phase converter with a commutation reactor (Lf) and high pass output filter (Rf, Cf). The reactor and filter helps in preventing the switching harmonics flow into the power supply. The VSC1 is connected in series with BUS1 and VSC2 is connected in parallel with load L1 at the Feeder1 end. VSC3 is connected in series with BUS2 at the Feeder2 end. The converters are linked to the distribution system via a transformer; the other sides of transformers (series-connected) are connected with buses BUS1 and BUS2 serially whereas the secondary side of the transformer (shunt-connected) is connected with load L1 in parallel.

The regulation of load voltages (ul1 & ul2) against sag/swell, interruption and disturbances in the system to protect the nonlinear/sensitive loads L1 and L2; and the compensation of reactive and harmonic components of non linear load current (il1) are the objectives of the MC-UPQC. In order to achieve these goals, series VSCs (i.e., VSC1 and VSC3) operate as voltage controllers while the shunt VSC (i.e., VSC2) operates as a current controller.

There are two series VSCs and one shunt VSC in the MC-UPQC structure as in Fig. 1 and the controlled strategies used for series and shunt VSCs are sinusoidal pulse width modulation (SPWM) voltage control and hysteresis current control, respectively.

2.1 Series VSCs:

The function of series VSC is to mitigate voltage sag and swell, voltage harmonics and current compensation during interruption. The control algorithm used is based on d-q method. The control block of series VSC is shown in fig.2. It consists of abc to dq0 transformation block which computes the three phase quantities to the direct axes, quadrature axes and zero sequence voltages, in the rotating reference frame using Park's transformation.

$$i_{l\_dq0} = T_{abc}^{dq0} i_{l_{abc}} \quad (1)$$

$$T_{abc}^{dq0} = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & \cos(\omega t - 120^o) & \cos(\omega t + 120^o) \\ -\sin(\omega t) & -\sin(\omega t - 120^o) & -\sin(\omega t + 120^o) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (2)$$

The controlling is based on comparison of a voltage reference and measured terminal voltage ***il-abc***. The PLL block is used to synchronize three phase terminal voltages on a set of frequency. The resultant signals are again transformed back to three phase quantities. This will be a vectorised signal consisting of three phase sinusoidal quantities. These are given to the PWM generator which generates pulses for the converter. The converter produces the three phase voltage signals which is free from distortions and is fed to the non-linear load.

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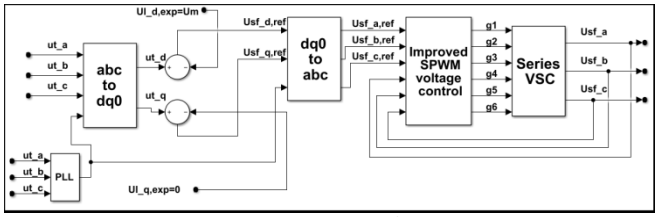

Fig. 2. Control block diagram of the series VSC.

2.2 Shunt VSC:

The function of shunt VSC is to compensate for the reactive and the harmonic components of the load currents of non-linear load. It should also regulate the voltage of common DC-link capacitor. Here the three phase load currents are converted to dq0 quantities and harmonics are eliminated to obtain three phase vectorised currents. These currents are used as carrier signals in the PWM hysteresis current control method to generate pulses for the shunt converter which produces distortions less currents for the load. PI and Adaptive PI controllers are used to maintain the DC-link voltage at the reference value $u_{dc\text{-}ref}$.

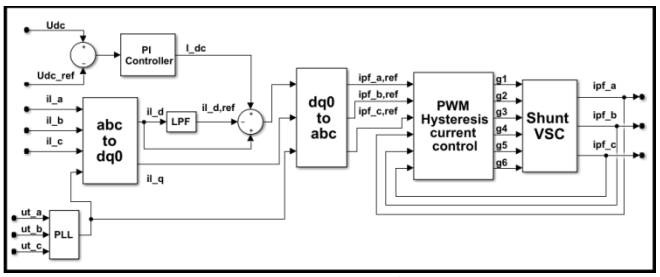

Fig. 3. Control block diagram of the shunt VSC

2.3 Adaptive PI Control For Shunt VSC

The shunt VSC with fixed PI control parameters may not reach the desired and acceptable response in the power system when the power system operating condition (e.g., loads or transmissions) changes. An adaptive PI control method is presented in this section in order to obtain the desired response and to avoid performing trial and error studies to find suitable parameters can be realized. An adaptive PI control block for shunt VSC is shown in Fig.4.

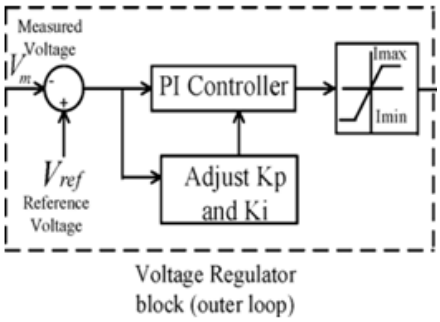

Fig.4 Adaptive PI control block for STATCOM

In Fig.4, the measured voltage Vm(t) and the reference voltage Vref(t), and the q axis reference current and the axis current are in per unit values. The proportional and integral parts of the voltage regulator gains are denoted by KP-v and Ki-V, respectively. In this control system, the allowable voltage error Kd is set to 0. The Kp-v, Ki-V can be set to an arbitrary initial value such as simply 1.0.

The process of the adaptive voltage control method for shunt VSC is described as follows:

1) The bus voltage $V_m(t)$ is measured in real time.

2) When the measured bus voltage over time $V_m(t) \neq V_{ss}$, the target steady-state voltage, which is set to 1.0 per unit (p.u.) in the discussion and examples, $V_m(t)$ is compared with V_{ss}. Based on the desired reference voltage curve, $K_{p\text{-}v}$ and K_{iv} are dynamically adjusted in order to make the measured voltage match the desired reference voltage, and the q-axis reference current I_{qref} can be obtained. Then, a suitable angle can be found eventually the dc voltage in shunt VSC can be modified such that shunt VSC provides the exact amount of reactive power injected in to the system to keep the bus voltage at the desired value.

III. SIMULATION RESULTS

3.1. Sag/Swell and Distortion on the Bus Voltage in Feeder-1

Let us consider that the power system in Fig. 1 consists of two three-phase three-wire 415(v) (RMS, LL), 50-Hz utilities. The BUS1 voltage (ut1) contains the seventh-order harmonic and the fifth order harmonic with a value of 18.27%, and the BUS2 voltage (ut2) contains the fifth order harmonic with a value of 32.46%. The BUS1 voltage contains 25% sag between 0.1s<t<0.2s and 20% swell between 0.2s<t<0.3s. The BUS2 voltage contains 35% sag between 0.15s<t<0.25s and 30% swell between 0.25s<t<0.3s.

The nonlinear sensitive load L1 is a three-phase rectifier load with an RL load of 30Ω and 20mH. And the sensitive critical load L2 contains a balanced RL load of 30Ω and 20mH. The MC–UPQC is switched on at t=0.02s. The BUS1 voltage, the corresponding compensation voltage injected by VSC1, and finally load L1 voltage are shown in Figure 5. Similarly, the BUS2 voltage, the corresponding compensation voltage injected by VSC3, and finally, the load L2 voltage are shown in figure 6.

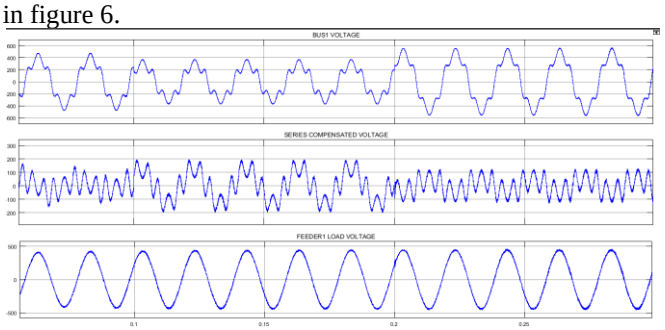

Fig 5. Simulation Result for BUS1 voltage, series compensating voltage, and load voltage in Feeder1.

As shown in these figures, distorted voltages of BUS1 and BUS2 are satisfactorily compensated for across the loads L1 and L2 with very good dynamic response. The nonlinear load current, its corresponding compensation current injected by VSC2, compensated Feeder1 current, and, finally, the dc-link capacitor voltage are shown in Fig. 5. The distorted nonlinear load current is compensated very well, and the total

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harmonic distortion (THD) of the feeder current is reduced to less than 5%.

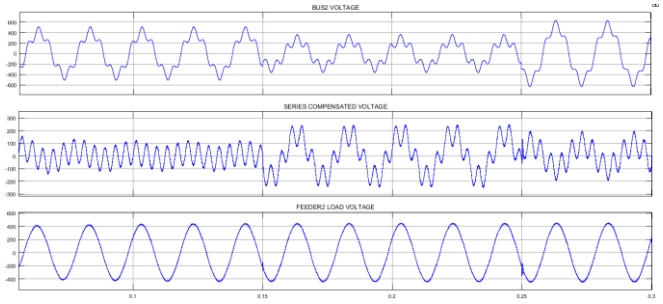

Fig 6.Simulation Result for BUS2 voltage, series compensating voltage, and load voltage in Feeder2**.**

Also, the DC voltage regulation loop has functioned properly under all disturbances, such as sag/swell in both feeders.

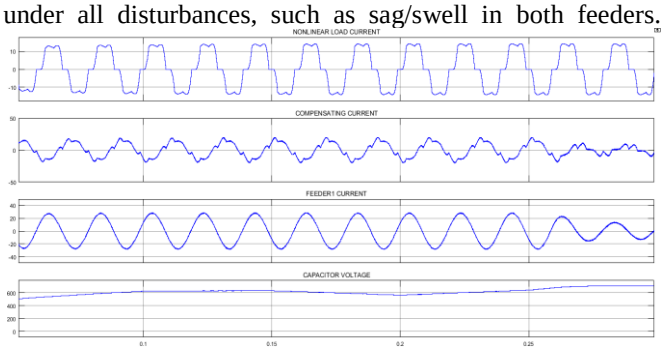

Fig 7.Simulation Result for Nonlinear load current, compensating current, Feeder1 current, and capacitor voltage.

3.2. Upstream Fault on Feeder2

When a fault occurs in Feeder2 (in any form of L-G, L-L-G, and L-L-L-G faults), the voltage across the sensitive/critical load L2 is involved in sag/swell or interruption. This voltage imperfection can be compensated for by VSC2. In this case, the power required by load L2 is supplied through VSC2 and VSC3. This implies that the power semiconductor switches of VSC2 and VSC3 must be rated such that total power transfer is possible. The performance of the MC-UPQC under a fault condition on Feeder2 is tested by applying a three- phase fault to ground on Feeder2 between 0.3s<t<0.4 s. Simulation results are shown in Fig.8.

3.3. Load Change

To evaluate the system behavior during a load change, the nonlinear load L1 is doubled by reducing its resistance to half at 0.5 s. The other load, however, is kept unchanged. In this case load current and source currents are suddenly increased to double and produce distorted load voltages (*Ul1* and U*l2*) as shown in Fig 9.

The simulation results for the three-phase BUS1 voltage, series compensation voltage, and load voltage in feeder 1 are shown in Fig. 10. The simulation results show that the harmonic components and unbalance of BUS1 voltage are compensated for by injecting the proper series voltage. In this figure, the load voltage is a three-phase sinusoidal balance voltage with regulated amplitude.

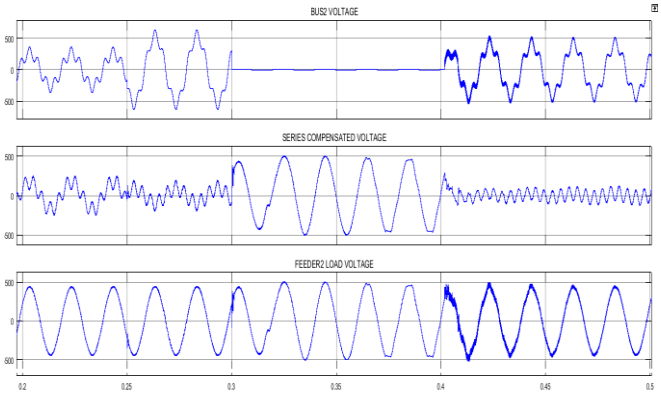

Fig 8.simulation results for an upstream fault on Feeder2:

BUS2 voltage, compensating voltage, and load L2 voltage.

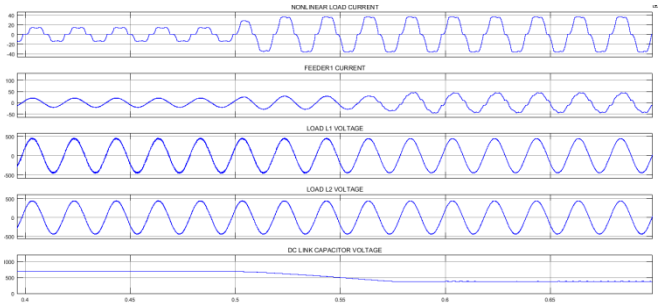

Fig 9.Simulation results for load change: nonlinear load current, Feeder1 current, load L1 voltage, load L2 voltage, and dc-link capacitor voltage

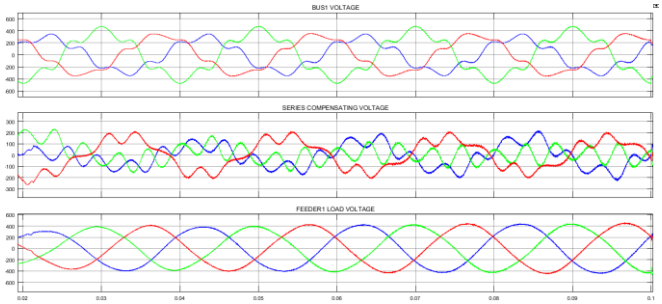

Fig.10 Bus1 voltage, series compensating voltage and load voltage in Feeder1 under unbalanced source voltage

IV. CONCLUSION

In this paper, a new configuration named Multi Converter Unified Power Quality Conditioning (MC-UPQC) system has been proposed which enabled the compensation of both voltage and current simultaneously in adjacent feeders. In this proposed topology, the full protection of critical loads and sensitive loads is done aligned with distortion, sag, swell and interruption compared to the existing UPQC. The proposed MC-UPQC allows the power transfer from one feeder to other to compensate for sag/swell and interruption. The interruptions are compensated without battery storage system and without storage capacity limitation. Also the compensation of sharing power between two adjacent feeders which are not connected is also an advantage of MC-UPQC. The performance of MC-UPQC is evaluated using Matlab/Simulink software under different disturbance conditions.

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