Accuracy-aware self-quantizing hardware architectures for 2-d discrete wavelet transform

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Abstract-This paper design for both digit-serial (DS) bit-parallel (BP) and accuracy-effective execution of the discrete wavelet transform (DWT), with specific consideration set to the force of depth on the common computational precision. These process a multilevel discrete wavelet transform to a given fault tolerance requisite and ensure an energy-smallest execution, which increase the applicability JPEG 2000. Experimental determine of design performance in terms of speed, area and power for 90-nm balancing Metal–oxide semiconductor implementation. Results specify that while BP designs exhibit natural speed benefit, DS plan want considerably fewer hardware reserve with raise precision and DWT level. A four-level DWT with high accuracy, for example,though the BP plan is four timesquicker than the digital-serial design, occupydouble thearea. In addition to the BP and DS designs, the work flexible DWT processor is presented, which carry run-time arrangingDWT parameter.

Index Terms – Discrete wavelet transform, Fixed point arithmetic, image coding, lifting-base, very large scale integration (VLSI)

I.INTRODUCTION

THE JPEG 2000 standard [1] present extensive code efficiency and flexibility benefit above the original block DCT-based JPEG standard, it have however to be commonly adopt for some years because the regularity was completed. The cause for this comprises the great install based of devices and software use the block DCT-based JPEG as fine as the computational weight occupied in performing JPEG 2000 compression. A enter part of JPEG 2000 be the discrete wavelet transform (DWT), which recursively decay an enter picture into sub bands with special spatial frequency and orientation. The large normally used DWT filters in JPEG 2000 are the biorthogonal lossless 5/3 integer and lossy 9/7 floating-point filter banks. We focus on the DWT using 9/7 filter, which provide very excellent compression value but is mainly challenging to implement with high efficiency due to the ridiculous nature of the filter coefficients.

The relatively only some behaviors of this difficulty include the work of Barua, Spiliotopoulosin, Kotteri, and Benkridin. The work in believe the effects of quantizing the lifting coefficients of the 9/7 DWT. The number of canonical signed digit idiom for the coefficients are varied, and their effects on the peak signal-to-noise ratio and hardware area/speed are evaluated. The work in behaviors a like analysis with the fixed-point data path fixed to 12 bits of integer and 12 bits offractional

accuracy, which provides sufficient dynamic choice to compute a six-level DWT with over 50-dB PSNR. The work in check up the effect on PSNR when quantizing filter coefficients for a convolution-based 9/7 DWT, and centers on evaluate dynamic range requirements of the DWT crossways different sub bands and decomposition stages.

II.DWT (Discrete wavelet transform)

A .Lifting-basedApproach

Two-level DWT on an image performing steps illustrates in a Fig.1. The 1-D DWT is first executes on the rows of the image construct low-frequency L1 and high-frequencyH1 components. Later than the stage a 1-D DWT again on the columns of L1 and H1, the first level of decomposition is finished, and LL1, HL1, LH1, and HH1 are achieved. When lifting is used, the 9/7 filter can be expressed using the following steps:

p(z)=

$$\begin{bmatrix} 1 & \alpha(1+Z^{-1}) \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ \beta(1+Z) & 1 \end{bmatrix}\begin{bmatrix} 1 & \gamma(1+Z^{-1}) \\ 0 & 1 \end{bmatrix}$$

$$X\begin{bmatrix} 1 & 0 \\ \delta(1+Z) & 1 \end{bmatrix}\begin{bmatrix} \zeta & 0 \\ 0 & 1/\zeta \end{bmatrix}$$

Where α = 1.586134342, β=0.05298011854,γ=0.8829110762,δ=0.4435068522 and ζ=o.4435068522

Fig.2 illustrates the flipping structure depict by Huangfor the lifting-based 1-D 9/7 DWT. Although the flipping structures divide the similar computational complexity with the traditional lifting scheme, it decreases the critical path significantly by flipping computation units with the inverses of multiplier coefficients. Constants C_0…. C5 are given by

C_0=1/α= - 0.6304636206

C_1=1/ (αβ) =0.7437502472

C_2=1/ (βγ) =-0.668067710

C_3=1/ (γδ) =0.6384438531

C_4=α βδ/ζ=2.065244244

C_5=αβγδζ=2421021152

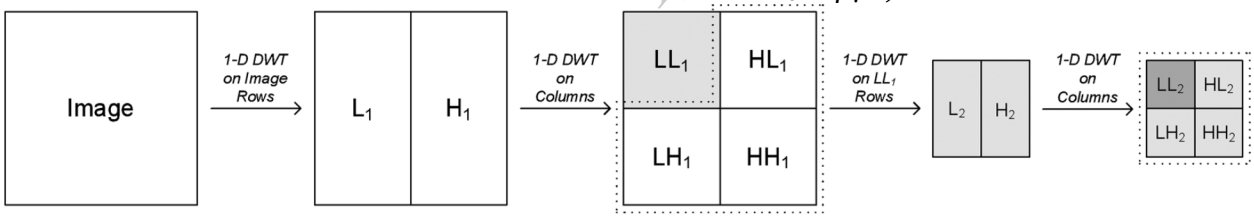

Fig.1. the dotted portions are the final wavelet transformed data**.**

Input, which has been dc level shifted by subtracting,$2^{Bx-1}$is split between even and odd samples, i.e., $d_i^0$and $S_i^{1.}$

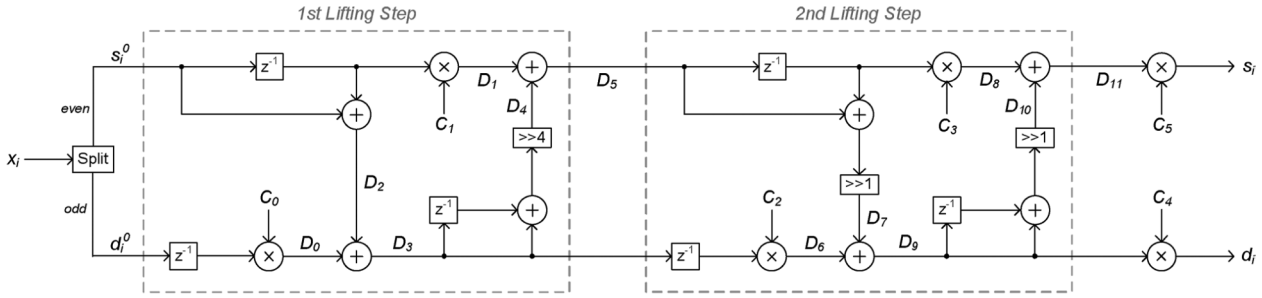

Fig. 2. Flipping structure for the lifting-based 1-D 9/7 DWT

B.Quantization

Quantization is a key element for the lossy 9/7 DWT in governing Achievable compression performance. The JPEG 2000 standard supports uniform dead-zone quantization, as well as Trellis coded quantization.Uniform dead-zone quantizationis preferred in this work due to its plainness and hardware efficiency.

III.BIT-PARALLEL DWT DESIGN

We first judge a BP approach, which is suitable when computing speed is the most important target. Given the lifting frame described before, the design confront lies in formative the appropriate amount of integer and limited bits to use in representing all the signals exploit during the computation. In the planning that pursue, two's complement fixed-point depiction is used for all signals. The amount of integer bits, limited bits, and the whole number of bits of signal are represent by IB,FB , and B=IB+FB.

For IB determination, we use the approach portray in [17], which is based on computing the extraction of the derivatives of every signal.Since the binary position needs to be associatedfor trappings, the two addition operands need to split thesame IB. thus, for the 1-D DWT shown in Fig. 2, the subsequentsignal couple need to divide the same IB, i.e.,(D0,D2) ,(D1,D4), and(D6,D7) . Practically, this implythat the IB should be set to the better IB of the two, e.g., IBD0=IBD2=MAX (IBD0, IBD2).

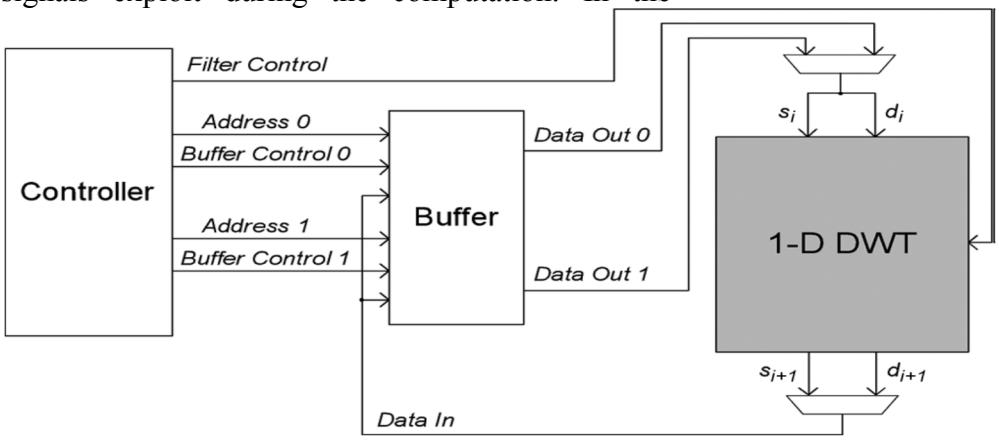

Fig.3. Generic High-Level Architecture of the DWT Designs

A. Integer Bit-Width Determination

For IB determination, we use the approach portray in [17], which is based on computing the extraction of the derivatives of every signal.

B. Fractional Bit-Width Optimization

The fractional bit-width optimization is complete in two steps,i.e., a static step foundation on methodical model to obtain the initial set of bit widths, tag along by a dynamic step based onreplication that extra decrease the bit widths by income of a PSNR deltaentry.

1)Static Optimization:The worst case (maximum absolute error) quantization errors for truncation and round-to-nearest are given by

Truncation:Ez=max (0, 2-FBz -2-FBz') (1)

Round-to-nearest:

$$E_z = \begin{cases} 0, & \text{if } \mathrm{FB}_z \geq \mathrm{FB}_{z'} \\ 2^{-\mathrm{FB}_z - 1}, & \text{otherwise} \end{cases} \quad (2)$$

2) Dynamic Optimization: The systematic optimizationscheme is conventional in the sense that it assumes that theworst case error can concomitantly happen at all nodes, whichis exceptionallylikely to happen in observe.

IV. DIGIT-SERIAL DWT DESIGN

A. Overview

While DS arithmetic has a important benefit over BP interms of circuit area, a enter challenge in DS design involves reducethe number of iterations. For the DS representationsused here, we use a radix-2 SD unneeded number system [19].

B. Integer Width Determination

As in the BP approach, the purpose here is to use the smallest amountnumber of integer digits for every signal while pass up run over.The binarypoint of a digit can be attuned via increasing or decreasingthe numeral of integer digits.

TABLE I
BP APPROACH INTEGER BIT WIDTHS AND FRACTIONAL BIT WIDTHS FOR A TWO-LEVEL DWT

Signal	IB Level 1 Row	IB Level 1 Column	IB Level 2 Row	IB Level 2 Column	FB
C_0	1	1	1	1	15
C_1	1	1	1	1	18
C_2	1	1	1	1	14
C_3	1	1	1	1	19
C_4	3	3	3	3	12
C_5	3	3	3	3	12
x_i / $\hat{x}_i$	0 (0)	1 (1)	2 (1)	3 (2)	8 or 19
D_0	2 (0)	3 (0)	4 (1)	5 (1)	16
D_1	0 (0)	1 (1)	2 (1)	3 (2)	18
D_2	2 (1)	3 (2)	4 (2)	5 (3)	16
D_3	2 (2)	3 (2)	4 (3)	5 (3)	15
D_4	0 (-1)	1 (-1)	2 (0)	3 (0)	18
D_5	1 (1)	2 (1)	3 (2)	4 (2)	18
D_6	1 (1)	2 (2)	3 (2)	4 (3)	18
D_7	1 (1)	2 (1)	3 (2)	4 (2)	18
D_8	0 (0)	1 (0)	2 (1)	3 (1)	16
D_9	0 (0)	1 (0)	2 (1)	3 (1)	15
D_{10}	0 (0)	1 (0)	2 (1)	3 (1)	16
D_{11}	0 (0)	1 (0)	2 (1)	3 (1)	16
s_i / $\hat{s}_i$	1 (1)	2 (1)	3 (2)	4 (2)	19
d_i / $\hat{d}_i$	1 (1)	2 (1)	3 (2)	4 (2)	19

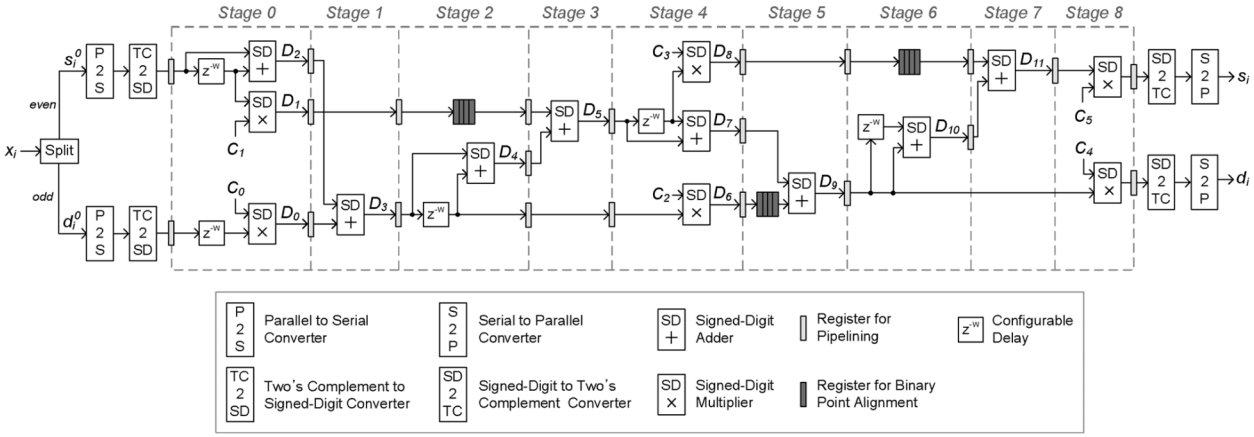

Fig.4 DS 1-D 9/7 DWT data flow

C. Minimizing the Number of DS Iterations

In a DS implementation, raising the number of iterationsgive extra precision but cost more execution time. The objectof iteration optimization is thus to use the smallest amount number ofiterations while discussion the specific error constraint.

$$E_z = E_x + E_y + \max(0, 2^{-\mathrm{FD}_z} - 2^{-\mathrm{FD}_x}) + \max(0, 2^{-\mathrm{FD}_z} - 2^{-\mathrm{FD}_y})$$

Where the previous two terms are quantization error due to using asubset of digits of x and y, which is a purpose of the number ofiterations.

V. RUN-TIME CONFIGURABLE DIGIT SIREAL ARCHITECTURE

The BP and DS architectures discuss in Sections IIIand IV allow optimized multiplication of a single stage of theDWT at a single accuracy constraint.In order to construct the DS approach configurable, the subsequentchange is required.

1) A table contains the number of iterations necessary for each worker for the range of goal combinations of DWT levels and accuracy is generated. The entry of this table is unwavering using the technique described in Section IV.

2) Shift registers that want to delay by aword (such as the configurable delay rudiments in Fig. 4) need to be large enough to support the widest achievable (which will most possible be the uppermost level and accuracy).

VI. IMPLEMENTATION RESULTS

A. Speed

Since BP operator method a word each cycle and DS operator process a word in multiple cycles, DS architectures require extra clock cycles. However, DS operators are fast with no bring propagation. Additionally, the speed of the DS operators is independent of the word size.

B. *Area*

It was absent because memories can be realized in quite a few different ways and since we wanted the results to bring to light the key machinery focused in this paper.

C.*Power*

Power rakishness is resolute by the mixture of static power and dynamic power. Static power principally results from transistor leakage current, whereas dynamic power is mainly due to switching behavior for charging and discharging load capacitance.

OUTPUT EXECUTION

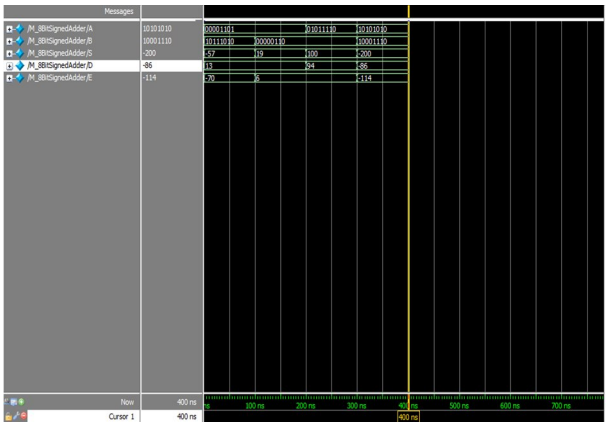

Fig 5. 8-Bit Signed Adder

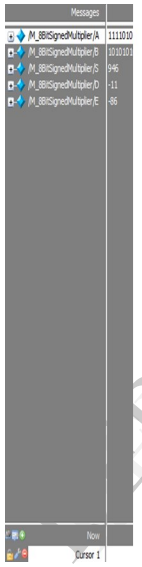

Fig 6. 8-Bit Signed Multiplier

VII.CONCLUSION

We have existing precision-aware approaches and connected hardware implementations for the theater the DWT. Both BP and DS design methodologies and outcomes have been presented. These techniques enable use of an optimal amount of hardware property in the DWT computation. Moreover, these frames enable quantization, which is conventionally executed after the DWT in algorithms such as JPEG 2000, to be specially incorporated into the computation of the DWT itself. We have also presented a highly flexible configurable DWT processor and examine the energy and power tradeoffs between the linked BP and DS designs, in exacting, weight the differing personal roles of static and dynamic power in each. We believe that design technique and architectures such as those presented here play a significant role in the design of energy- and precision-optimized DWT implementations.

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