A VLSI Based Low Power Approach Using Dynamic Voltage Scaling & Voltage Islands for Embedded Processor with Hybrid Parallelism

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Abstract- Today power consumption is the big issue in the world. VLSI design efforts have mainly focused on optimizing speed to realize computationally on real time functions. Therefore, we maximize the run time and minimize the requirements to reduce the power consumption. Network On Chip is an IC approach to design the communication subsystem between IP cores in a SOC. Our approach uses dynamic voltage scaling and voltage islands. This technique of partitioning the core in to multiple voltage and frequency islands aims to reduce the dynamic and leakage power. This paper, demonstrates the optimization at software level, with the compiler support using voltage islands to reduce the power by selectively shutting down the different regions of the chip and running the selected parts of the chip at different voltage & frequency levels. Using this technique where the frequency can be automatically adjusted to conserve the power or to reduce the amount of heat generated by the chip. Our experiments indicate that both data and task parallelism need to be employed as hybrid model in which the speed, area, power utilization can be observed using Xilinx 12.1 tools with multisim. The proposed approach behaves better performance, energy savings and the voltage scaling of memory & execution time.

Index terms-voltage frequency islands, dynamic voltage frequency scaling, energy optimization, network on chip.

1. Introduction

Low power design has become a significant requirement when the CMOS technology entered the nanometer era. VLSI design efforts have mainly focused on optimizing speed to realize computationally on real time functions. So to maximize the run time and minimize the power consumption.

On the one hand, hundreds to millions of transistors can be integrated on the same chip using SOC design methodologies. On the other hand, the shrinking feature sizes and increasing circuit speed cause higher power consumption, which not only shorten the battery life of handheld devices but also lead to thermal and reliability problems.

NOC is an IC approach to design the communication subsystem between IP cores in a SOC. NOC can span synchronous and asynchronous clock domain or use unclocked asynchronous logic.NOC applies networking theory & methods to on chip communication and bring notable improvements over conventional bus and cross bar interconnects NOC improves scalability of SOC. One such hardware approach is voltage frequency islands in which speed, area, power utilization can be observed using Xilinx 12.1 tools. Our goal is mainly to minimize power consumption by exploiting data and task parallelism together and application mapping should be performed carefully. Automated compiler support can be very effective in using the parallelisms and resulting in best energy saving. In addition, our approach combines the use of dynamic frequency scaling link, where frequency is dynamically adjusted to minimize the power dissipation while maintaining the performance demands.

Our results on togetherness of data and task parallelism with compiler support and frequency scaling link show that the energy savings we achieve are consistent across a wide range of values of our major simulation parameters.

2. Related Work

Although today processors are much faster and far more versatile, than their predecessors using high speed circuits and parallel processing, they also consume a lot of power. Hence power consumption and heat dissipation are becoming important issues in chip design, major chip manufacturers, such as IBM [5]and Intel [9],are using voltage islands in their current and future products.

Different approaches are used to adapt in order to overcome the above said issues. For example the voltage islands, frequency islands, dynamic voltage scaling and frequency scaling. Specifically guangyu et al. [2] discuss the methods of channel voltage scaling in which compiler decides the appropriate voltage levels to be used for communication channels in the NOC. Young E.F.Y et al. [3] To minimize the number of level shifters between different voltage islands & to simply the power routing step by placing the islands. IBM [4] manufactures adapting the voltage islands in their products. To manage the power by using two managers are used. One for managing the IC and other for managing one of the power islands. G.De Micheli et al[5] discuss about the comparison of NOCs and SOCs using multiple voltage and frequency islands with 2 dimensional and 3 dimensional analysis. Power and delay are unclear in SOCs. Huaizhi et al[6] shows the voltage assignment to reduce the leakage and dynamic powers using multi supply voltage. Power optimization under constraints are used to assign the supply voltage, gate sizing and placements are discussed by B. Liu, y.cai et al [7]. Hung Ming Chen et al [8] shows the simultaneously assign the voltage islands and the floor plan. In [9], authors propose both voltage and frequency islands are used to assignment, mapping and allocation process are done for getting better performance. Kumar,R [10] present DVFS technique using design level techniques to optimize the maximum energy efficiency. Chia Chen Tsai et al [11] present an appropriate algorithm for power minimization. Rountree.B et al [12] present to describe how we use to leading load cycles to improve the predict performance and avoid the misprediction by DVFS technique. Rajapakse,A et al[13] present an approach for the transient signals generating events as islands and non islanding which is detected in distribution network. In [14] authors propose the power consumption model for distributed applications. In [15] authors used an islanding mode to detect the disconnection in the levels such as voltage and frequency.

3. Block diagram:

The block diagram consists of Network- on -chip, memory, buffer controller and using energy aware of data parallelism, task parallelism. System processing speed, whole chip area and power consumption become the critical design challenges. Network-on-chip designs are also considered to improve system efficiency. It consists of IP core, network interface, router and physical link. IP core represent the processing element.

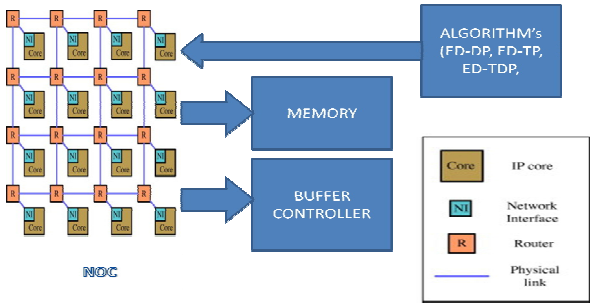

Figure 1: Block diagram

Processing element (PE) is the component that performs custom packet processing. A PE may be fixed-function or programmable. PEs are free to implement their specified functionality in any manner. The implementation of a PE will affect its performance which may have consequences for the performance of the network as a whole. A waypoint may contain more than one PE. A waypoint that contains multiple PEs may offer multiple services, or may offer a single service, utilizing the multiple PEs for scalability or construction of complex services. NOC is an IC approach to designing the common subsystem between IP cores in a Soc. NOC can span synchronous& asynchronous clock domain or use unlocked asynchronous logic. NOC improves scalability of SOCs.NOC links can reduce the complexity of designing wires for predictable speed, reliability etc., Network interface is a system interface between two pieces of equipment or protocol layers in a network. Usually have some form of network address. Its function is to passing message.

Router is a device that forwards data packets between the computer network creating an overlay internetwork. Router is connected to two or more data lines from different network. Ring router is used in this paper. When a data packet comes in one of the lines, the router leads the address information in the packet to determine its ultimate destination. Ring router is an effective algorithm before X-Y routing is used. Ring router is low complex so only it is used. Memory is the process in which information is encoded, stored & retrieved. Encoding represents the receiving, processing

& combination of received. Here RAM memory is used to store the information and it is volatile.

4. ALGORITHM

Our approach uses data parallelism, task parallelism and both data and task parallelism. Data parallelism involves all the processors execute a similar code with works on different parts of array of data. Task parallelism involves select different parts of data to perform different task. Take the plus point of both parallelism and using look up table (LUT).

4.1 Data Parallelism

Data parallelism involves performing a similar computation on many data objects simultaneously. In our approach, group of processors execute a similar code but work on different parts of array data. Using VHDL code to write a program and choose the device in the device properties. In that virtex-6 can be used to verify the Xpower analyzer. The program can be successfully implemented then check the power utilization. Using design summary to determine the area and speed. In the data parallelism has the power utilization of 72.3%.

Steps for Data Parallelism

- Initialize the parameters.
- Evaluate based on fixed voltage according to encoder results.
- Observe the parameter results.
- Estimate the executive time and process status.
- Integration the above steps with applications.
- Estimate the device parameters.

4.2 Task Parallelism

Task parallelism perform different parts of array data and arbitrary sequence of computations. Different loop nest in different processor. Using VHDL code to write a program and choose the device in the device properties. In that virtex-6 can be used to verify the Xpower analyzer. The program can be successfully implemented then check the power utilization. Using design summary to determine the area and speed. The power utilization of task parallelism is 69.4% Compare to the data parallelism the power utilization can be decreased.

Steps for Task Parallelism

- Initialize the parameters.
- Evaluate the table based voltage.
- Observe the parameters results.
- Estimate the execution time and processors status.
- Integrate the above results with applications.
- Estimate the device parameters.

4.3 Data and Task Parallelism

Using both parallelisms used to write a program using VHDL code and choose the device in the device properties. Using Xpower analyzer, the power utilization can be checked. In this parallelism the power utilization of 47.5% and the device summary is used to determine the area and speed. The power utilization can be more decreased compared to using individual parallelism.

Steps for task parallelism

- Initialize the parameters..
- Use both fixed and table based voltage to evaluate.
- Observe the parameter results.
- Estimate the execution time and process status
- Integrate the above steps with applications.
- Estimate the device parameters.

Thus the simulation process can be done by using Xilinx tool. To write a program using VHDL code of data parallelism, task parallelism and both data & task parallelism. Using dynamic voltage scaling technique to determine the voltage of each algorithm. It is a power management technique, where the voltage used in a component is increased or decreased, depending upon circumstances & requirement.

5. RESULTS :

Table 1Power, Speed, Area Consumption of Three Parallelisms

ALGORITHM	POWER	AREA	SPEED
Data parallelism	72.3%	199900 KB	879.275 MHZ
Task parallelism	69.4%	199772 KB	879.275 MHZ
Data & Task Parallelism	47.5%	199772 KB	879.275 MHZ

The graphical representation of power utilization for the three algorithms 1.data parallelism, 2.Task parallelism 3.Hybrid model of data and task parallelism is given below.

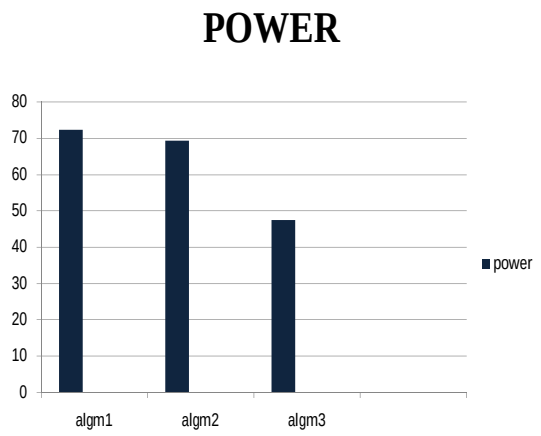

Figure6: Power measurement

The graphical representation of area utilization for the three algorithms 1.data parallelism,2.Task parallelism 3.Hybrid model of data and task parallelism is given below

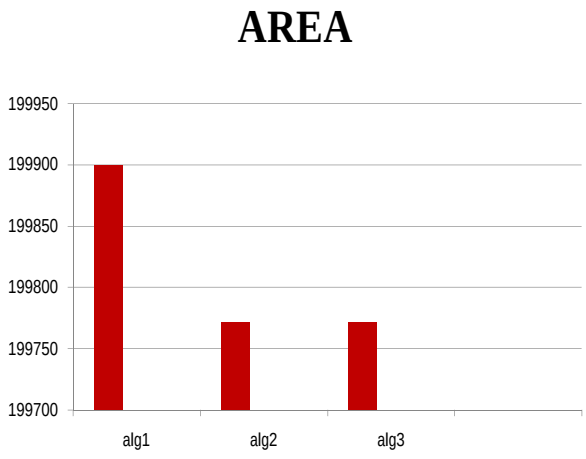

Figure 7: Area measurement

The graphical representation of processor speed for the three algorithms 1.data parallelism, 2.Task parallelism 3.Hybrid model of data and task parallelism is given below

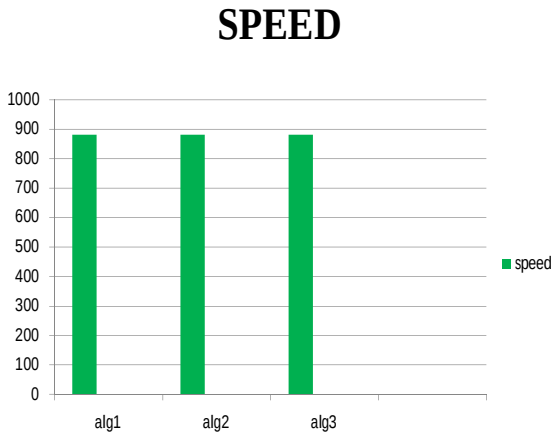

Figure 8: Speed Measurement

Table 2 Execution Time for Three Parallelism

ALGORITHM	EXECUTION TIME
Data Parallelism	3.414ns
Task Parallelism	3.127ns
Hybrid Model	1.310ns

The graphical representation of execution time for the three algorithms 1.data parallelism, 2.Task parallelism 3.Hybrid model of data and task parallelism is given below

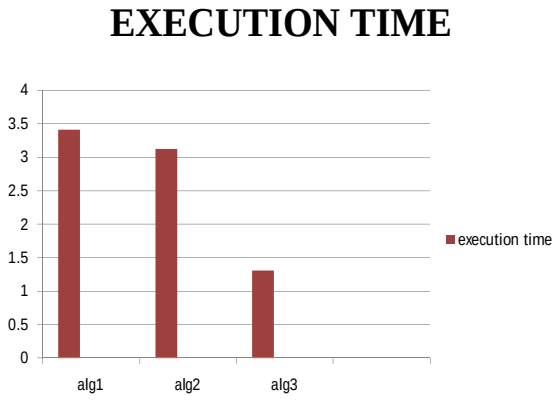

Figure 8: Execution time measurement

Table 3 Voltage Scaling Of Memory

MEMORY	VOLATGE	CURRENT	POWER
1 BIT	2.47 V	2.50 pA	6.181pW
2 BIT	2.97 V	2.00 pA	5.945pW

In the above table the voltage scaling is done in memory and the results of power consumption in the 1 bit and 2 bit memory is furnished**.**

6. CONCLUSION & FUTURE WORK:

The concepts of data parallelism, task parallelism, and hybrid model by the combination of both data and task parallelism has been done and the power consumption and execution time for the same are measured .The results show that hybrid model produces better performance. The concept of voltage scaling is applied to the memory of the NOC .This DVS need to be applied to other units in the block diagram and further analysis can be done.

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