

# A Survey of USB 3.0 with Data Transmission Techniques

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**Abstract**— USB is the dominant interface for external computer peripherals. Peripherals which need very high speed data transfer rate implements all the function of USB interface as dedicated hardware. It is standard for wired connection between two electronic devices (with maximum speed of 5Gbps), including a mobile phone and desktop computer. The connection is made by a cable that has a connector at either end. One end, the one that plugs into the computer, is the same across all USB cables while one that plug into the mobile devices. Different USB standard available till date are USB 1.0,1.1, USB 2.0 and USB 3.0. In these standards the transmission, reception and flow control of packets on the bus is managed by the USB Host Controller. In this paper we investigate the architecture of USB3.0 with different layers and power management.

**Keywords**— USB3.0, Universal Serial Bus, Super Speed USB

## I. INTRODUCTION

The original motivation for the Universal Serial Bus (USB) came from several considerations, two of the most important being:

### • Ease-of-use

The lack of flexibility in reconfiguring the PC had been acknowledged as the Achilles 'heel to its further deployment. The combination of user-friendly graphical interfaces and the hardware and software mechanisms associated with new-generation bus architectures have made computers less confrontational and easier to reconfigure. However, from the end user's point of view, the PC's I/O interfaces, such as serial/parallel ports, keyboard/mouse/joystick interfaces, etc., did not have the attributes of plug-and-play.

### • Port Expansion

The addition of external peripherals continued to be constrained by port availability. The lack of a bidirectional, low-cost, low-to-mid speed peripheral bus held back the creative proliferation of peripherals such as storage devices, answering machines, scanners, PDA's, keyboards, and mice. Existing interconnects were optimized for one or two point products. A search new function or capability was added to the PC, a new interface had been defined to address this need. USB 1.0: Released in January 1996.Specified data rates of 1.5Mbit/s (Low-Bandwidth) and 12Mbit/s (Full Bandwidth). Does not allow for extension cables or pass through monitors

(due to timing and power limitations). Few such devices actually made it to market. USB 1.1: Released in September 1998. Fixed problems identified in 1.0, mostly relating to hubs. Earliest revision to be widely adopted. Initially, USB provided two speeds (12 Mb/s and 1.5 Mb/s) that peripherals could use. As PCs became increasingly powerful and able to process larger amounts of data, users needed to get more and more data into and out of their PCs. This led to the definition of the USB 2.0 specification in 2000 to provide a third transfer rate of 480 Mb/s while retaining backward compatibility. In 2005, with wireless technologies becoming more and more capable, Wireless USB was introduced to provide a new cable free capability to USB.

USB is the most successful PC peripheral interconnect ever defined and it has migrated heavily into the CE and Mobile segments. In 2006 alone over 2 billion USB devices were shipped and there are over 6 billion USB products in the installed base today. End users "know" what USB is. Product developers understand the infrastructure and interfaces necessary to build a successful product.

USB has gone beyond just being a way to connect peripherals to PCs. Printers use USB to interface directly to cameras. PDAs use USB connected keyboards and mice. The USB On-The-Go definition provides a way for two dual role capable devices to be connected and negotiate which one will operate as the "host." USB, as a protocol, is also being picked up and used in many nontraditional applications such as industrial automation.

Now, as technology innovation marches forward, new kinds of devices, media formats, and large inexpensive storage are converging. They require significantly more bus bandwidth to maintain the interactive experience users have come to expect. HD Camcorders will have tens of gigabytes of storage that the user will want to move to their PC for editing, viewing, and archiving. Furthermore existing devices like still image cameras continue to evolve and are increasing their storage capacity to hold even more uncompressed images. Downloading hundreds or even thousands of 10 MB, or larger, raw images from a digital camera will be a time consuming process unless the transfer rate is increased. In addition, user applications demand a higher performance connection between the PC and these increasingly sophisticated

peripherals. USB 3.0 addresses this need by adding an even higher transfer rate to match these new usages and devices. Thus, USB (wired or wireless) continues to be the answer to connectivity for PC, Consumer Electronics, and Mobile architectures. It is a fast, bidirectional, low-cost, dynamically attachable interface that is consistent with the requirements of the PC platforms of today and tomorrow.

## II. INTRODUCTION TO USB 3.0

The Universal Serial Bus 3.0 Specification Revision 1.0 was released in November 2008, with the first USB 3.0 device-controller hardware expected to follow about a year later. Windows will likely support USB 3.0 sometime after the release of Windows 7, the successor to Windows Vista.

USB 3.0 defines new dual-bus architecture (Figure-1) with two physical buses that operate in parallel. USB 3.0 provides a pair of wires for USB 2.0 traffic and additional wires to support the new Super Speed bus at 5 Gbps. Super Speed offers a more than 10 time increase over USB 2.0's high speed. Plus, unlike USB 2.0, Super Speed has a pair of wires for each direction and can transfer data in both directions at the same time. USB 3.0 also increases the amount of bus current devices can draw and defines protocols for more aggressive power saving and more efficient transfers.

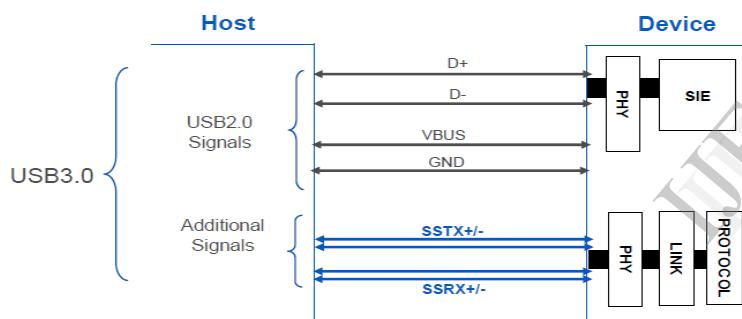


Figure: 1 USB3.0 Bus Communication Architecture

## III. USB3.0 SYSTEM DESCRIPTION

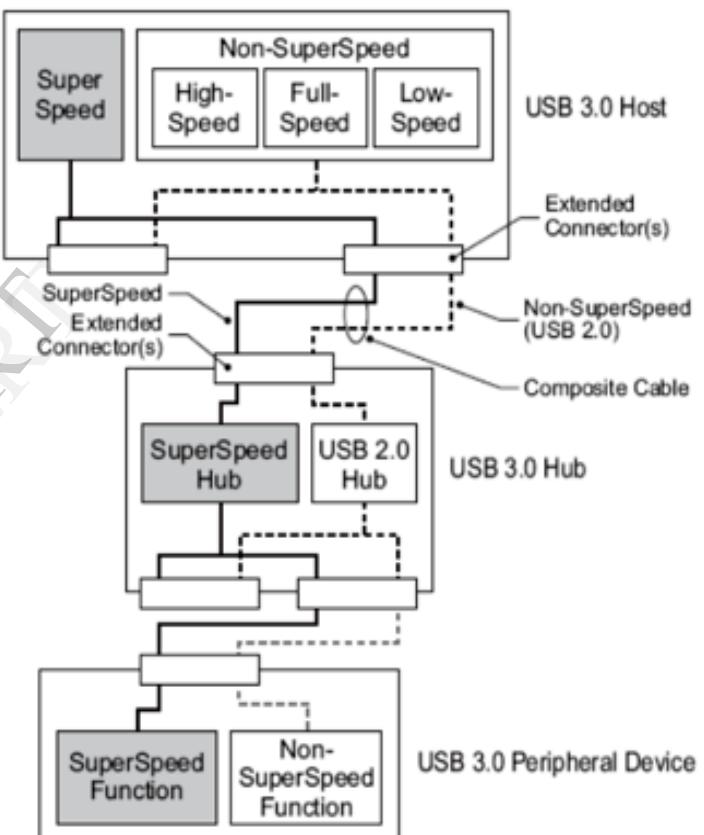
USB 3.0 is a physical SuperSpeed bus combined in parallel with a physical USB 2.0 bus (Figure 2). It has similar architectural components as USB 2.0, namely:

- USB 3.0 interconnect
- USB 3.0 devices
- USB 3.0 host

The USB 3.0 interconnect is the manner in which USB 3.0 and USB 2.0 devices connect to and communicate with the USB 3.0 host. The USB 3.0 interconnect inherits core architectural elements from USB 2.0, although several are augmented to accommodate the dual bus architecture.

The baseline structural topology is the same as USB 2.0. It consists of a tiered star topology with a single host at tier 1 and hubs at lower tiers to provide bus connectivity to devices.

The USB 3.0 connection model accommodates backwards and forward compatibility for connecting USB 3.0 or USB 2.0 devices into a USB 3.0 bus. Similarly, USB 3.0 devices can be attached to a USB 2.0 bus. The mechanical and electrical backward/forwards compatibility For USB 3.0 is accomplished via a composite cable and associated connector assemblies that form the dual-bus architecture. USB 3.0 devices accomplish backward compatibility by including both Super Speed and non-Super Speed bus interfaces. USB 3.0 hosts also include both Super Speed and non-Super Speed bus interfaces, which are essentially parallel buses that may be active simultaneously.



Note: Simultaneous operation of SuperSpeed and non-SuperSpeed modes is not allowed for peripheral devices.

Figure-2 USB 3.0 Dual Bus Architecture  
IV. SUPERSPEED ARCHITECTURE

The SuperSpeed bus is a layered communications architecture that is comprised of the following elements:

- **SuperSpeed Interconnect.** The SuperSpeed interconnect is the manner in which devices are connected to and communicate with the host over the SuperSpeed bus. This includes the topology of devices connected to the bus, the communications layers, the relationships between them and how they interact to accomplish information exchanges between the host and devices.

- **Devices.** SuperSpeed devices are sources or sinks of information exchanges. They implement the required device-end, SuperSpeed communications layers to accomplish information exchanges between a driver on the host and a logical function on the device.

- **Host.** A SuperSpeed host is a source or sink of information. It implements the required host-end, SuperSpeed communications layers to accomplish information exchanges over the bus. It owns the SuperSpeed data activity schedule and management of the SuperSpeed bus and all devices connected to it.

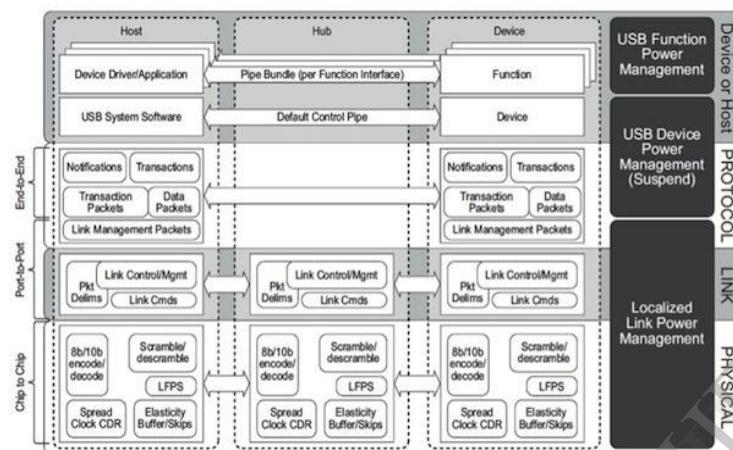


Figure-3 USB3.0 Communications Layers and Power Management Elements

### Physical Layer

The physical layer specifications for SuperSpeed defines the PHY portion of a port and the physical connection between a downstream facing port (on a host or hub) and the upstream facing port on a device. The SuperSpeed physical connection is comprised of two differential data pairs, one transmit path and one receive path. The nominal signaling data rate is 5 Gbps.

### Link Layer

The Link Layer specifications for SuperSpeed is a logical and physical connection of two ports. The connected ports are called link partners. The link layer defines the logical portion of a port and the communications between link partners.

### Protocol Layer

The Protocol Layer specifications for SuperSpeed define the end-to-end communications rules between a host and device. All protocol layer communications are accomplished via the exchange of packets. Packets are sequences of data bytes with specific control sequences which serve as delimiters managed

by the link layer. Host transmitted protocol packets are routed through intervening hubs directly to a peripheral device. Device Transmitted protocol packets simply flow upstream through hubs to the host.

## V. USB 3.0 POWER MANAGEMENT OVERVIEW

The SuperSpeed architecture has been defined with platform power efficiency as a primary objective. Some of the key power efficiency enhancements include:

- Elimination of continuous device polling.
- Elimination of broadcast packet transmission through hubs.
- Introduction of link power management states enabling aggressive power savings when idle.
- Host and device initiated transition to low power states.
- Device and individual Function level suspend capabilities enabling devices to remove power from all, or only those portions of their circuitry that are not in use.

### Link Power Management

Link power management enables a link to be placed into a lower power state when the link partners are idle. The longer a pair of link partners remain idle, the deeper the power savings that can be achieved by progressing from U0 (link active) to U1 (link standby with fast exit), to U2 (link standby with slower exit), and finally to U3 (suspend).

After being configured by software, the U1 and U2 link states are entered and exited via hardware autonomous control. Hardware autonomous transitions for the U1 and U2 link states enable faster response times. This, in turn, translates to better power savings when entering a power saving state, and less impact on the operational state when exiting. The U3 link state however is entered only under software control, typically after a software inactivity timeout, and is exited either by software (host initiated exit) or hardware (remote wakeup). The U3 link state is directly coupled to the device's suspend state.

## VI. CONCLUSION & FUTURE SCOPE

Through this paper we understand the concept of USB 3.0 and serial data communication. In this paper we also understand backward compatibility of USB 3.0. We understand the SuperSpeed features of USB 3.0. We also understand different layers in SuperSpeed USB. Along with SuperSpeed USB 3.0 also provide power management and data integrity through LTSSM and CRC. In future we can see due to data bursting capability USB 3.0 provide far more speed than USB 2.0 as device does not have to wait for the hub's acknowledgment. And also error free data transmission with high throughput.

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