Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 5 Issue 06, June-2016

A Study on Compressor Adders for Fast Multipliers

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***Abstract*—In this paper, different compressor adders are analyzed and compared with conventional adders. Architectures of 5-3, 10-4, 15-4 and 20-5 compressor units are compared with conventional adders. The compressor adders decrease the critical delay compared to conventional adders and can be used in multiplier architectures. Analysis is done by coding the designs in Verilog and synthesized with Xilinx ISE 14.6 using Virtex6 series of FPGA. Optimized architectures are synthesized using Encounter RTL Compiler Tool in Cadence and obtained the reports on power, area. The results indicate the better speed performance and overall efficiency of compressor adders. It can be used in multipliers and applied on Multiply Accumulate Units for Digital Signal Processing applications.**

Keywords—MAC unit, compressor

I. INTRODUCTION

Device level to architectural levels of ideas were already proposed the fundamental problems regarding power consumption. However, there is no universal way to avoid tradeoffs between power, delay and area. So the techniques chosen by a designer for a particular target must satisfy the application and needs.

Multiplier is one of the critical components dictating the overall circuit performance as long as constrained by power consumption and computation speed. In multiplication process, the reduction of partial products contributes most to the overall delay, power and area. Compressors are employed to reduce the latency of this step. Hence compressors are a critical component of the multiplier circuit that greatly influences the overall multiplier speed. For high speed applications, a huge number of compressors are to be used in multiplications to perform the partial product addition. Thus the studies related to the field of multipliers and adders are endless and still significant. Therefore, it is of great interest to develop high speed and low power compressors with minimum number of transistors. Conventionally, partial product reduction has been carried out through the use of carry save adders consisting of rows of 3:2 counters, otherwise known as full adders. To increase the speed of multiplication higher order reduction schemes have been adopted. As the compressors are used repeatedly in larger systems, improved design with lowest transistor count and reduced delay will contribute a lot towards overall system performance.

In the case of area occupied, as the compressor has reduced number of gates as compared to a full adder and half adder based circuit, the area also had reduced equivalently. The compressor based multiplier has occupied reduction with respect to the modified booth methodology. Even though the compressor based architecture occupies area more than that of the booths method, considering the speed of circuit which is the major concern, case of area can be ignored [11].

In this paper, section II briefly reviews the compressor adder architecture and concepts. Simulation results with schematic diagrams and waveforms of each design are coming under chapter III. The section IV deals with the results and comparisons of compressors. Finally, section V concludes the report.

II. COMPRESSOR ADDERS

A compressor adder provides reduced delay over conventional adders using full adders and half adders. It is represented as N-r, where N represents the number of bits and r represents the total count of 1s present in N bits. It is termed as compressor so that it reduces the gate count and delay compared to other adder circuits. Studies are taken place to improve circuits of lower order compressors [2]. The compressor circuits which can be used for multiplication process such as 5-3, 10-4, 15-4 and 20-5 are explained in next subsection.

The Fig. 1 shows the schematic view of 5-3 compressor adder. In this compressor adder maximum of five bits can be added and a result of three bit is obtained. Maximum possible value obtained is 101, which is the three bit binary of decimal 5. In the figure n2, n3 and n4 are 4:1 multiplexers which allow only one output to be high in an instant, which results in lowering the delay and consumes low power.

In Fig. 2 schematic view of 10-4 compressor adder obtained using incisive simulator in cadence is showed. In this compressor adder maximum of ten bits can be added and a result of four bit is obtained. Maximum possible value obtained is 1010, which is the four bit binary of decimal 10. In the Fig. 2, a1 and a2 are 5-3 compressor units, a3 and a5 are full adders and a4 is a half adder. As it is making use of compressor adders inside the circuitry, it results in further reduction of the delay.

In Fig. 3 schematic view of 15-4 compressor adder obtained using incisive simulator in cadence is showed, which adds maximum of fifteen bits and a result of four bit is obtained. Maximum possible value obtained is 1111, which is the four bit binary of decimal 15. In the Fig. 3, u0 to u4 are full adders, it uses two 5-3 compressor units (u5 and u6) and a 4 bit parallel adder denoted as u7. Similarly in 20-5 compressor adder, it adds maximum of twenty bits at a time and a result of five bit is obtained. Maximum possible value obtained is 10100, which is the four bit binary of decimal 20.

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In Fig. 4, u8 is 15-4 compressor adder and u9 denotes 5-3 compressor adder. Other blocks are full adder and half adder modules [2].

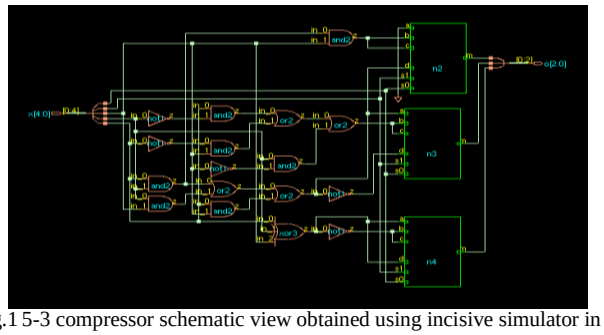

Fig.1 5-3 compressor schematic view obtained using incisive simulator in Cadence

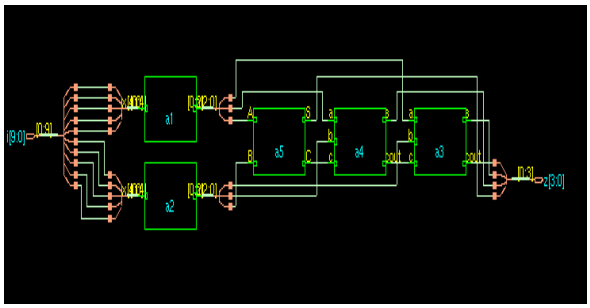

Fig.2 10-4 compressor schematic view obtained using incisive simulator in Cadence.

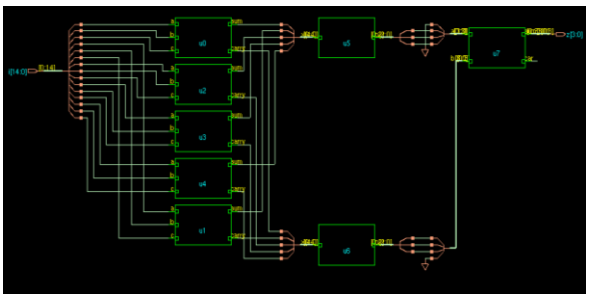

Fig.3 15-4 compressor schematic view obtained using incisive simulator in Cadence

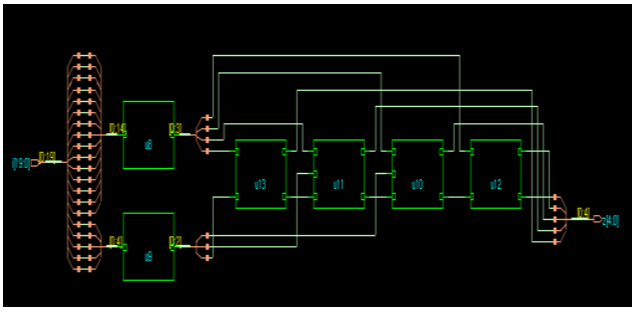

Fig.4 20-5 compressor schematic view obtained using incisive simulator in Cadence

III. SIMULATION RESULTS

The architectures of 5-2, 10-4, 15-4 and 20-5 compressors are coded in Verilog and logic synthesis and delay reports are taken using Xilinx ISE 14.6 simulator. Target device is Virtex 6: xc6vcx75t-2ff484, speed grade -2. Comparison in terms of delay among enhanced compressors and conventional ones are given in table 1. For input bits 5, 10, 15 and 20 compressor adders is having delay less than conventional ones.The results and inferences obtained from the simulation results were explained in this section with the help of tabular and graphical comparisons.

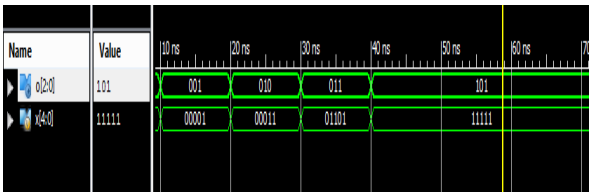

Fig.5 Simulated waveform of 5-3 compressor

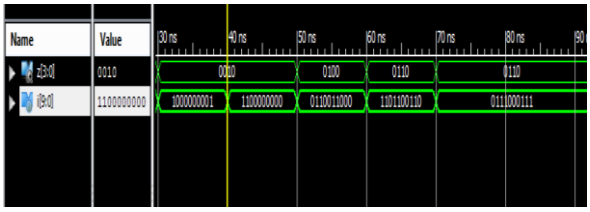

Fig.6 Simulated waveform of 10-4 compressor

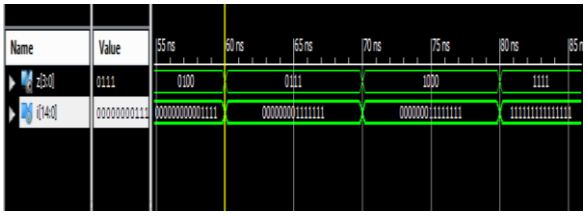

Fig.7 Simulated waveform of 15-4compressor

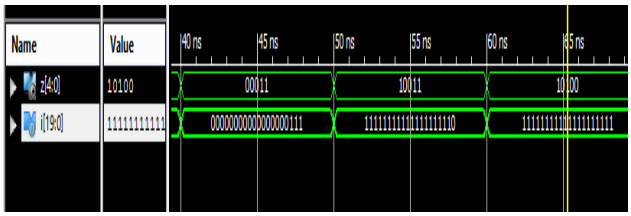

Fig.8 Simulated waveform of 20-5 compressor

IV. RESULTS AND COMPARISONS

In table 1, Compressor adders with 5, 10, 15 and 20 inputs are compared with conventional adders in terms of combinational delay. The code is simulated and synthesized using Xilinx ISE 14.6. The result shows there is considerable amount of improvement in compressor adders than the conventional adders. The comparison of 5 inputs, 10 inputs, 15 inputs and 20 inputs conventional adders and compressor adders are plotted in a graph, which is shown in Fig. 9. The use of enhanced version of Virtex also provides good results. It is well suited for applications such as DSP, where these compressors can make use for MAC units etc. Table 2 explains about the synthesized reports on power, area, gate reports on each compressor adders which is obtained from Cadence Encounter RTL complier tool.

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TABLE I. COMPARISON TABLE OF CONVENTIONAL AND COMPRESSOR ADDERS

Number of inputs	Combinational Delay	
	Conventional Adder	Compressor Adder
5 bit	1.611	1.184
10 bit	3.10	1.880
15 bit	3.843	2.940
20 bit	5.126	3.078

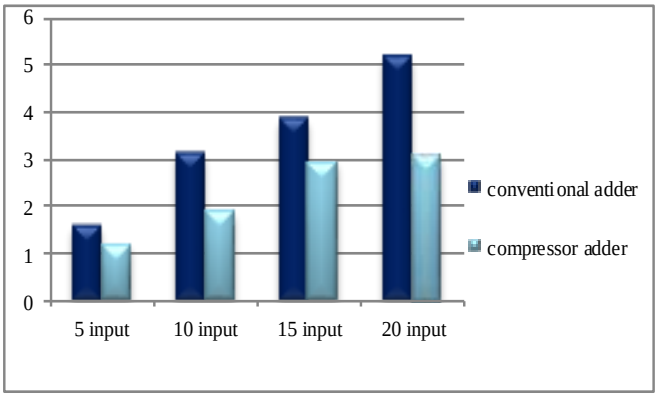

Fig.9 Graph showing comparison of delay

TABLE II. REPORTS OBTAINED ON COMPRESSOR ADDERS USING CADENCE ENCOUNTER RTL COMPLIER TOOL

Type of compressor	Leakage power (nW)	Dynamic power (nW)	Total power (nW)	Total cell area (μm^2)	Total gate area
5-3	276.26	2183.09	2459.35	75	75.499
10-4	992.01	12182.1	13174.2	112	112.468
15-4	1129.2	11141.8	12271.1	274	274.478
20-5	1657.2	17241.1	18898.4	406	406.426

V. CONCLUSION

In this work, 5-2, 10-4, 15-4 and 20-5 compressors are compared with conventional ones and delays are compared with conventional architectures by coding the designs in Verilog and synthesized with Xilinx ISE 14.6 using Virtex 6 series of FPGA. Optimized architectures are synthesized using Encounter RTL Compiler Tool in Cadence and obtained the reports on power, total cell area and gate area. The results indicate the better speed performance and overall efficiency of compressor adders over conventional adders. That is, by optimizing the design the efficiency can be improved without much area overhead and compressor adders reduce the delay up to a great extent than conventional adders. As a future work these compressors can be used in multipliers which can be used in MAC units for high speed applications.

V. ACKNOWLEGMENT

The authors would like to acknowledge all of our professors and assistant professors of ECE department, RSET, Rajagiri valley, Kerala and many others in VLSI and Embedded system branch students who have contributed to the work.

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