A Study on Adiabatic Logic Circuits for Low Power Applications

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Abstract- **Adiabatic logic circuits are widely employed in Low power VLSI circuits to achieve power efficient system. To limit the power dissipation adiabatic operation promises large power reduction because it reused the energy rather than dissipation. In this paper adiabatic logic principle is discussed for CMOS based low power VLSI design followed by adiabatic logic. In this paper different adiabatic logic families has been discussed, which can be classified as partially and fully adiabatic.**

I. INTRODUCTION.

1.1 Brief of Electronics

The history of electronics is a story of twentieth century and the three key components- the vacuum tube, the transistor and the integrated circuit. In 1883, Thomas Alva Edison discovered that electrons will flow from one metal conductor to another through a vacuum. This discovery of conduction became known as the Edison effect. In 1904, John Fleming applied the Edison effect in inventing a two-element electron tube called a diode, and Lee De Forest followed in 1906 with the three-element tube, the triode. These vacuum tubes were the devices that made manipulation of electrical energy possible so it could be amplified and transmitted [1]. In 1947, the transistor was invented by a team of engineers from Bell Laboratories. John Bardeen, Walter Brattain, and William Shockley received a Nobel prize for their creation, but few could envision how quickly and dramatically the transistor would change the world. The transistor functions like the vacuum tube, but it is tiny by comparison, weighs less, consumes less power, is much more reliable, and is cheaper to manufacture with its combination of metal contacts and semiconductor materials[1].

Digital CMOS (Complementary Metal oxide Semiconductor) integrated circuits have been the driving force behind very large scale integration (VLSI) for high performance computing and other scientific and engineering applications. The demand for digital CMOS ICs will be continually strong due to silent features such as low power, reliable performance, circuit techniques for high speed such as using dynamic circuits, and ongoing improvements in processing technology.

It is now projected that the minimum feature size in CMOS ICs can decrease to 35nm within a decade [2]. With such a technology, the level of integration in a single chip can be in the order of several tens of billions of transistors for logic chips or even higher in the case of memory chips.

1.2 Need for Low Power CMOS Logic Circuits

The increasing prominence of portable systems and the need to limit power consumption in very high density ULSI chips have led to rapid and innovative developments in low power design during the recent years. The driving forces behind these developments are portable device applications requiring low power dissipation and high throughput, such as notebook computers, portable communication devices, and personal digital assistants (PDAs). In most of these cases, the requirements for low power consumption must be met along with equally demanding goals of high chip density and high throughput. Hence, low power design of digital integrated circuits has emerged as a very active and rapidly developing field. The limited battery lifetime typically imposes very strict demand on the overall power consumption of the portable system. Reducing the power dissipation of integrated circuits through design improvement is major challenge in portable system design. ULSI reliability is yet another concern which points to the need for low-power design. Therefore, the reduction of power consumption is also crucial for reliability enhancement [2].The methodologies which are used to achieve low power consumption in digital systems span a wide range, from device/process level to algorithm level. Device characteristics, device geometries, and interconnect properties are significant factors in lowering the power consumption. Circuit level measures such as the proper choice of circuit design styles, reduction of the voltage swing and clocking strategies can be used to reduce power dissipation at the transistor level. In this report we will be discussing the concept of adiabatic logic and its techniques. Since, it emerges as an effective means for reducing the power consumption.

II. OVERVIEW OF POWER CONSUMPTION

There are mainly three types of power dissipation in a CMOS based circuit:

1. Static power dissipation
2. Dynamic power dissipation
3. Short circuit dissipation

2.1 Static Power Dissipation

It is related to the logical states of the circuit rather than switching activities. In CMOS logic, *leakage current* is the only source of static power dissipation.

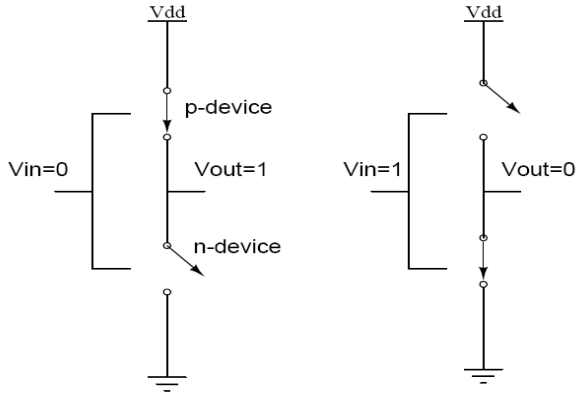


Figure 2 CMOS inverter model for static power dissipation [3]

When the input = '0', the associated n-device is off and the p-device is on. The output voltage is V_{dd} or logic '1'. When the input = '1', the associated n-device is on and the p device is off. The output voltage is '0'volts or V_{ss}. From figure 2 it can be seen that one of the transistors is always off when the gate is in either of these logic states. Since no current flows into the gate terminal, and there is no Dc path from V_{dd} to V_{ss} the resultant steady state current and the power P_s is zero [3].

The static power components become important when the circuits are at rest, i.e. when there is no activity in the circuits and they are all biased to a specific state of circuit. The static power dissipation mainly includes sub threshold and reversed-biased diode leakage currents. Due to the necessary but harmful (in a leakage- power sense) down – scaling of threshold voltages, the sub threshold leakage is becoming more and more pronounced. Below the threshold voltage, in weak inversion, the transistors are not completely off. The sub threshold current has a strong dependence on the threshold voltage. Sub threshold Current: Sub-threshold current that arises from the inversion charges that exists at the gate voltages below the threshold voltage. Tunneling Current: There is a finite probability for carrier being passed through the gate oxide which results in tunneling current thorough the gate oxide. Reverse-biased Diode Leakage: Reverse bias current in the parasitic diodes [4].

2.2 Dynamic Power Dissipation

In Figure 3, During switching from '0' to '1' or '1' to '0' , both n- and p-transistors are on for short period of time. This results in short current pulse from V_{dd} to V_{ss}. Current is also required to charge and discharge the output capacitive load. The current pulse from V_{dd} to V_{ss} results in '*short circuit dissipation'* that is dependent on the input rise/fall time, the load capacitance and gate design.

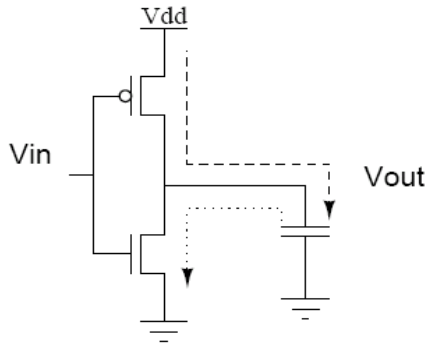


Fig 3. Power dissipation due to charging and discharging of capacitor [3]

Dynamic power dissipation can be further subdivided into three major categories: switched power dissipation, short circuit dissipation, and glitch power dissipation. All of them more or less depend on the signal, load capacitance, and supply voltage of the electronic circuit. The continuous charging and discharging of the load capacitance is necessary to transmit information in CMOS circuits [4].

2.3 Short circuit power dissipation

This type of power dissipation takes place due to large rise and fall time of the signal. This component of power dissipation occurs when pull up and pull down network both turns ON simultaneously. This can be minimizes by reducing the rise and fall time and keeping symmetrical both.

III. VLSI CIRCUIT DESIGN TECHNIQUE FOR LOW POWER CMOS LOGIC CIRCUIT

3.1 Adiabatic Circuits

Adiabatic Logic is the term given to low-power electronic circuits that implement reversible logic. The term comes from the fact that an adiabatic process is one in which the total heat or energy in the system remains constant. Research in this area has mainly been fueled by the fact that as circuits get smaller and faster, their energy dissipation greatly increases, a problem that adiabatic circuits promises to solves [5].Most research has focused on building adiabatic logic out of CMOS. However, current CMOS technology, though fairly energy efficient compared to similar technologies, dissipate energy as heat, mostly when switching.In order to solve this problem there are two fundamental rules CMOS adiabatic circuits must follow [5].

1. Never to turn on a transistor when there is a voltage difference between the drain and source.
2. The second says never to turn off a transistor that has current flowing through it.

Adiabatic logic works with the concept of switching activities which reduces the power by giving stored energy back to the supply. Thus, the term adiabatic logic is used in low-power VLSI circuits which implements reversible logic. In this, the main design changes are focused in power clock which plays the vital role in the principle of operation. Each phase of the power clock gives user to achieve the two major design rules for the adiabatic circuit design [6]. During the recovery phase energy will be restored to the power clock, resulting in considerable energy saving. Adiabatic logic offers a way to

reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy. By properly mixing the ideas derived for adiabatic and static CMOS circuits one can achieve low power dissipation in the circuit.

Adiabatic technique plays a vital role in portable devices that are inherently available with constraint in battery life. Long battery operating life requirement of portable devices can be addressed by investigating adiabatic logic. Compared with the conventional low power approaches, power dissipation can be significantly reduced by using the adiabatic computation. Over the years different low power adiabatic logic circuits are proposed. Though, CMOS technology provides circuits with very low static power dissipation, during the switching operation currents are generated, due to the discharge of load capacitances that cause a power dissipation which increases with the clock frequency. The adiabatic technique prevents such losses. The charge does not flow from the load capacitance to ground, but it flows back to a trapezoidal or sinusoidal supply voltage and can be reused. Power losses due to the resistance of the switches needed for the logic operation still occur. In order to keep these losses small, the clock frequency has to be much lower than the technological limit.

3.2 Adiabatic logic circuit principal

Adiabatic switching is used to minimize energy loss during charging/discharging [7]. During adiabatic switching all nodes are charged or discharged at a constant current in order to minimize power dissipation. This is accomplished by using ac power supplies to initially charge the circuit during specific adiabatic phases and then discharge the circuit to recover the supplied charge. The principle of adiabatic switching can be best explained by comparing it with the conventional switching technique.

3.3 Conventional and Adiabatic Switching

3.3.1 Conventional Logic Switching

In conventional CMOS level-restoring logic which uses the constant voltage source V_{dd} , the switching event of circuits with rail-to-rail output voltage swing causes an energy transfer from the power supply to the output node or from the output node to the ground the power dissipation have mainly 3 sources: dynamic, short circuit and leakage power dissipation. Among all, dynamic power dissipation is main component [8]. The equation of the power dissipation is given by.

$$Power = \alpha C_L V^2_{dd} f_{clk} + I_{sc} V_{dd} + I_{leakage} V_{dd} \quad (1)$$

First term in equation (1) represents the dynamic power, where α is the switching activity, CL is the loading capacitance, fclk is the clock frequency and V_{dd} supply voltage. The second term represents short circuit current Isc which arises when both the NMOS and PMOS transistors are simultaneously active, resulting into conducting current directly from supply to ground. Last is leakage current leakage which can arise from substrate injection and sub threshold effects is primarily determined by fabrication technology considerations [8].

3.3.2 Adiabatic Switching

Adiabatic switching can be achieved by charging the capacitor from a time-varying voltage source. Here, R is the "on" resistance of the PMOS network. Initially, the capacitance voltage V_C is zero, the variation of the voltage as a function of time can be,

$$V_{C(t)} = I_s * T / C \quad (2)$$

So the charging current can be expressed as

$$Is = C * Vc(t) / T \quad (3)$$

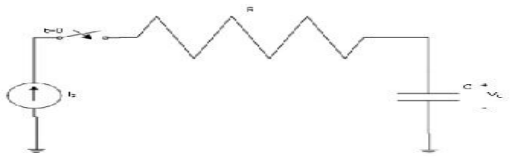


Figure4. Schematic for adiabatic charging process

The amount of energy dissipated in the resistor R from t = 0 to t = T

$$E_{Dissipated} = R * C/T * C * V_{CC}^2 \quad (4)$$

From (4) we can say that the dissipated energy is small if the charging time T>>2RC so it can be made small by increasing the charging time [8].

3.4 A Simple Adiabatic Logic Gate

A general circuit topology for the conventional CMOS gates and adiabatic counterparts is

shown in Figure 5. To convert a conventional CMOS logic gate into an adiabatic gate, the pull-up transistor and the pull-down transistor networks must be replaced with complementary transmission-gate (T-gate). The T-gate network implementing the pull-up function is used to drive the true output of the adiabatic gate, while the T-gate network implementing the pull-down function drives the complementary output node [7].

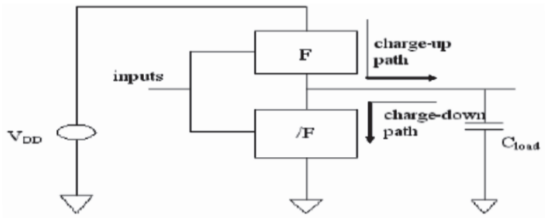


Fig 5. A Simple Adiabatic Logic Gate

Both the pull-up and pull-down networks in the adiabatic logic circuit are used for charging as well as discharging the output node capacitance, which ensures that the energy stored at the output node can be retrieved by the power supply, at the end of each cycle shown in Figure 6. To allow adiabatic operation, the DC voltage source of the original circuit must be replaced by a varying power supply with the ramped voltage output.

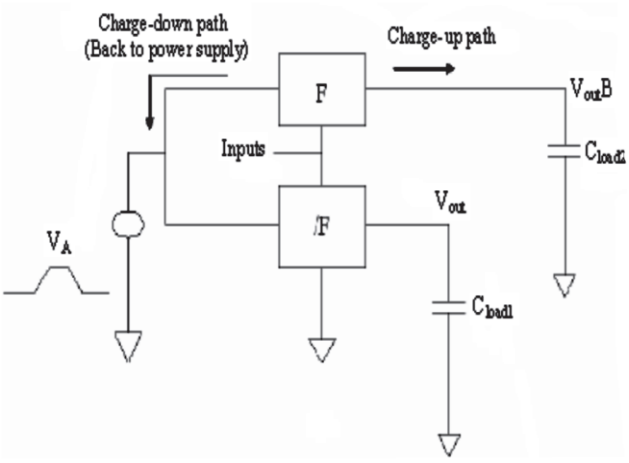


Fig. 6. Adiabatic Logic Gate showing charging and discharging path [7]

3.5 Steps of Adiabatic Circuit Design

General rules or steps to be followed for adiabatic circuit design are as follows:

- Replace each of the PMOS and NMOS devices in the pull-up and pull-down networks with T-gates.
- Use expanded pull-up network to drive the true output.
- Use expanded pull-down network to drive the complementary output.
- The Pull up network is given the input whereas the pull down network is feed will inverted input.
- Both networks in the transformed circuit are used both to charge and discharge the load capacitance.
- Replace DC V_{dd} by a pulsed power supply (Vpwr) with varying voltage to allow adiabatic operation

3.6 Adiabatic Logic Families

Adiabatic logic circuits are one that are based on adiabatic switching principal. Adiabatic logic circuits are classified into 2 types:

- Partially/Quasi Adiabatic Circuits
- Fully Adiabatic circuits

3.6.1 Partially/Quasi Adiabatic Circuits

Quasi adiabatic circuits have simple architecture and power clock system. The adiabatic loss occurs when current flows through non-ideal switch, which is proportional to the frequency of the power-clock [9].

Popular Partially Adiabatic families include the following:

I. Efficient Charge Recovery Logic (ECRL).
II. 2N-2N2P Adiabatic Logic.
III. Positive Feedback Adiabatic Logic (PFAL).
IV. NMOS Energy Recovery Logic (NERL).
V. Clocked Adiabatic Logic (CAL).
VI. True Single-Phase Adiabatic Logic (TSEL).
VII. Source-coupled Adiabatic Logic (SCAL).

Among these logic families two of them are chosen ECRL and PFAL, which shows the good improvement in power dissipation and mostly used as reference in new logic families for less power dissipation.

(i) Efficient Charge – Recovery Logic (ECRL)

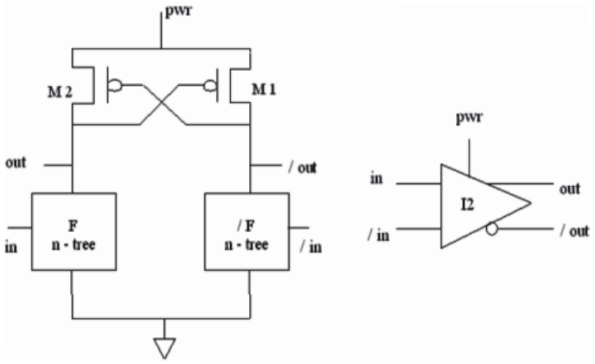


Fig. 7. Efficient Charge – Recovery logic (ECRL) purposed by Moon and Jeong [10]

Efficient Charge – Recovery Logic (ECRL) proposed by Moon and Jeong [10], shown in Figure 7, uses cross-coupled PMOS transistors. It has the structure similar to Cascode Voltage Switch Logic (CVSL) with differential signaling. It consists of two cross-coupled transistors M1 and M2 and two NMOS transistors in the N-functional blocks for the ECRL adiabatic logic block [10]. An AC power supply *pwr* is used for ECRL gates, so as to recover and reuse the supplied energy. Both out and /out are generated so that the power clock generator can always drive a constant load capacitance independent of the input signal. Full output swing is obtained because of the cross-coupled PMOS transistors in both precharge and recovers phases. But due to the threshold voltage of the PMOS transistors, the circuits suffer from the non-adiabatic loss both in the precharge and recover phases. That is, to say, ECRL always pumps charge on the output with a full swing. However, as the voltage on the supply clock approaches to |Vtp|, the PMOS transistor gets turned off. So the recovery path to the supply clock is disconnected, thus, resulting in incomplete recovery. *Vtp* is the threshold voltage of PMOS transistor. The amount of loss is given as:

$$E_{ECRL}=C\,|Vtp|^2/2 \qquad (5)$$

Thus, from equation (5), it can be inferred that the non-adiabatic energy loss is dependent on the load capacitance and independent of the frequency of operation. The ECRL circuits are operated in a pipelining style with the four-phase supply clocks. When the output is directly connected to the input of the next stage (which is a combinational logic), only one phase is enough for a logic value to propagate. However, when the output of a gate is fed back to the input, the supply clocks should be in phase. A latch is one of the simplest cases which have a feedback path. The input signals propagate to the next stage in a single phase, and the input values are stored in four phases (1-clock) safely. Let us assume in is at high and inb is at low. At the beginning of a cycle, when the supply clock 'pwr' rises from zero to V_{dd}, out remains at a ground level, because in turns on Ftree (NMOS logic tree). /out follows pwr through M1. When pwr reaches V_{dd}, the

outputs hold valid logic levels. These values are maintained during the hold phase and used as inputs for the evaluation of the next stage. After the hold phase, pwr falls down to a ground level, out node returns its energy to pwr so that the delivered charge is recovered. Thus, the clock pwr acts as both a clock and power supply. A major disadvantage of this circuit is the existence of the coupling effects, because the two outputs are connected by the PMOS latch and the two complementary outputs can interfere each other [7].

(ii) 2N-2P Adiabatic Logic Family

The schematic of the 2N-2P inverter gate is shown in Figure 8. Initially, input 'in' is high and input '/in' is low. When power clock (pclk) rises from zero to VDD, since F is on so output 'out' remains ground level. Output '/out' follows the pclk. When pclk reaches at VDD, outputs 'out' and '/out' hold logic value zero and VDD respectively. This output values can be used for the next stage as an inputs. Now pclk falls from VDD to zero, '/out' returns its energy to pclk hence delivered charge is recovered. ECRL uses four phase clocking rule to efficiently recover the charge delivered by pclk.

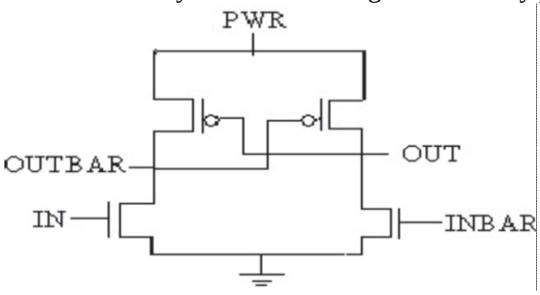


Figure 8. Schematic of 2N-2P inverter gate

(iii) 2N-2N2P Adiabatic Logic

The 2N-2N2P logic family was derived from 2N-2P in order to reduce the coupling effect. The major difference with respect to 2N-2P is that the latch is made by two p-MOSFETs and twon-MOSFETs, rather than by only two p-MOSFETs as in 2N- 2P. The additional cross-coupled n-MOSFET switches lead to non-floating outputs for a large part of the recovery phase.

(iv) Positive Feedback Adiabatic Logic (PFAL)

The partial energy recovery circuit structure named Positive Feedback Adiabatic Logic (PFAL) [11] has been used, since it shows the lowest energy consumption if compared to other similar families, and a good robustness against technological parameter variations. It is a dual-rail circuit with partial energy recovery. The general schematic of the PFAL gate is shown in Figure 9. The core of all the PFAL gates is an adiabatic amplifier, a latch made by the two PMOS M1-M2 and two NMOS M3-M4 that avoids a logic level degradation on the output nodes out and/out. This logic family also generates both positive and negative outputs.

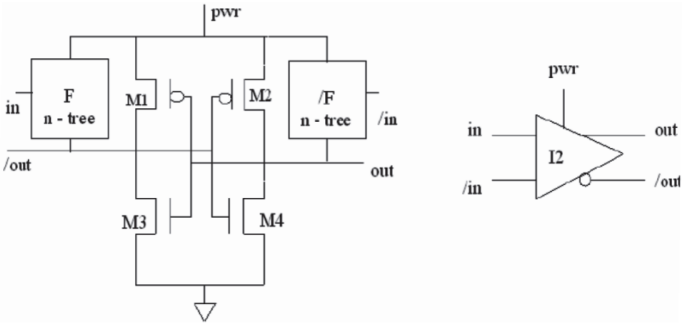


Fig. 9. The general schematic of PFAL Gate

PFAL consist of a latch formed by two cross-coupled inverters to store the output state when input signal are ramped down. The two n-trees connected in parallel of PMOS realize the logic functions. The PMOSFET of the adiabatic amplifier is in parallel to the functional block and form a transmission gate [7]. The two major differences with respect to ECRL are that the latch is made by two PMOSFETs and two NMOSFETS, rather than by only two PMOSFETs as in ECRL logic, and that the functional blocks are in parallel with the transmission PMOSFETs. Thus the equivalent resistance is smaller when the capacitance needs to be charged.

(v) Clocked Adiabatic Logic (CAL)

CAL is a dual-rail logic that operates from a single-phase AC power-clock supply [12]. In the adiabatic mode, the power clock supply waveform is generated using an on-chip switching transistor and a small external inductor between the chip and a low-voltage dc supply.

The basic CAL gate, the inverter, is shown in Figure 10. Cross-coupled CMOS inverters, transistors M1 – M4, provide memory function. In order to realize an adiabatic inverter and other logic functions with a single power clock, an auxiliary timing control clock signal CX has been introduced, as shown in Figure 10. This signal controls the transistors that are in series with the logic trees represented by the functional blocks F and /F. The CX-enabled devices allow operation with a single power clock pwr.

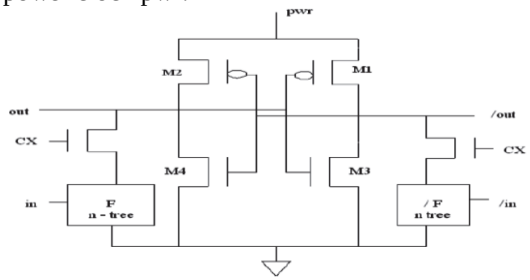


Figure 10. Basic CAL gate inverter

(vi) NMOS Energy Recovery Logic (NERL)

NMOS energy recovery logic (NERL), which uses NMOS transistors only and a simpler 6-phase clocked power. Its area overhead and energy consumption are smaller, compared with the other fully adiabatic logics. NERL is more suitable than the other adiabatic logic circuits for the applications that do not require high performance but low energy consumption. Schematic of NERL is shown in Figure 11.

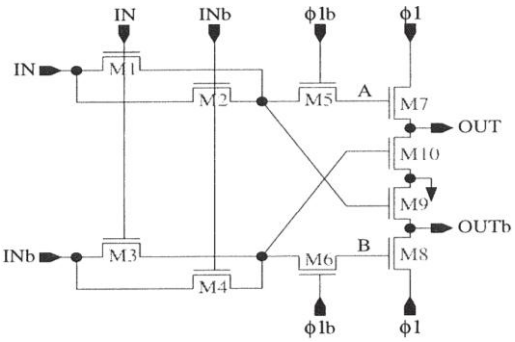
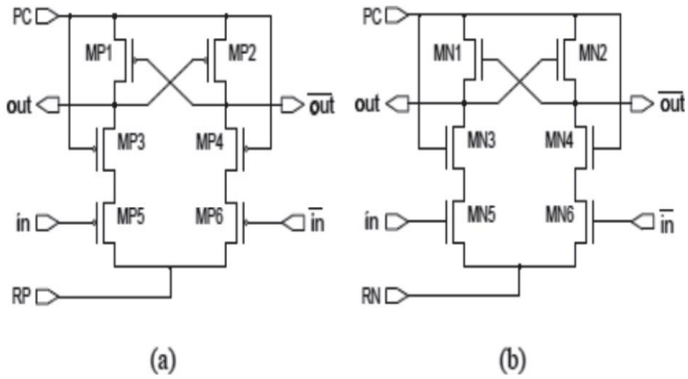


Figure 11.NMOS energy recovery logic gate

(vii) True Single-Phase Adiabatic Logic (TSEL)

TSEL is a partially adiabatic circuit family related to 2N2P, 2N- 2N2P, and CAL. Power is supplied to TSEL gates by a single phase sinusoidal power-clock. Cascades are composed of alternating PMOS and NMOS gates. Two DC reference voltages ensure high-speed and high-efficiency operation. They also enable the cascading of TSEL gates in an NP-domino style. In comparison with corresponding adders in Alternative logic styles and minimum possible supply voltages, TSEL is more energy efficient across a broad range of operating frequencies. Specifically for clock frequencies ranging from 10MHz To 200MHz. TSEL is the first energy-recovering logic family that operates with a single-phase sinusoidal clocking scheme. Both TSEL and SCAL gates are dual-rail and always present a balanced load to the clock generator, regardless of the particular data computed [7].Schematic of TSEL is shown in Figure 12.



(viii) Source-Coupled Adiabatic Logic (SCAL)

SCAL is, a partially adiabatic, dynamic logic family. SCAL retains all of TSEL's positive features, including single-phase power-clock operation. Moreover, it achieves energy efficient operation across a broad range of operating frequencies by using an individually tunable current source at each gate. SCAL achieves increased energy efficiency by using a tunable current source to control the rate of charge flow into or out of each gate. Our adiabatic circuitry avoids a number of problems associated with multiple power-clock schemes, including increased energy dissipation, layout complexity in clock distribution, clock skew, and multiple power-clock generators. Schematic of SCAL is shown in Figure 13 [7].

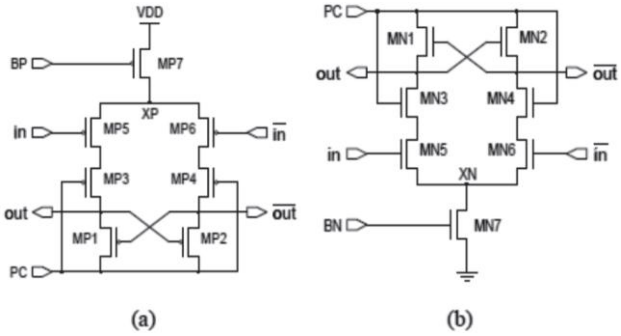


Figure 13.(a) Source-Coupled adiabatic logic using PMOS(b) Source-Coupled adiabatic logic using NMOS

3.6.2 Full Adiabatic Logic Circuits

Full-adiabatic circuits have no non-adiabatic loss, but they are much more complex than quasi-adiabatic circuits. All the charge on the load capacitance is recovered by the power supply. Fully adiabatic circuits face a lot of problems with respect to the operating speed and the inputs power clock synchronization [7].

Some Fully adiabatic logic families include:

(i) Pass Transistor Adiabatic Logic (PAL).

(ii) Split- Rail Charge Recovery Logic (SCRL)

(i) Pass Transistor Adiabatic Logic (PAL)

PAL is a dual-rail adiabatic logic with a relatively low gate complexity that operates with a two-phase power clock. A PAL gate consists of true and complementary pass transistor NMOS functional blocks (f, /f), and a cross coupled PMOS latch (M p l, Mp2), as illustrated by the example of Figure 14, which shows the implementation of an AND-OR gate: Q = A.B + C. The power is supplied through a sinusoidal power-clock (PC). When PC starts rising from low, input states make a conduction path from the power clock (PC) through one of the functional blocks to the corresponding output node and allow it to follow the power clock. The other node will be tri-state and kept close to OV by its load capacitance. This in turn causes one of the PMOS transistors to conduct and charge the node that should go to one state, up to the peak of PC. The output state is valid at around the top of the power clock.

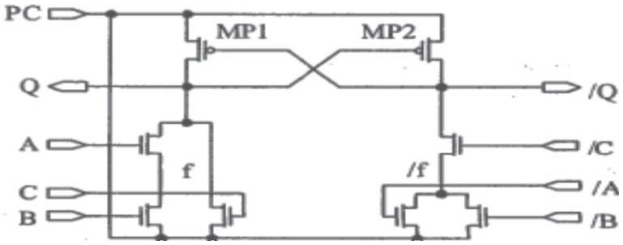


Figure 14. A PAL gate consists of true and complementary pass transistor NMOS functional blocks and a cross coupled PMOS latch

The power clock will then ramp down toward zero, recovering the energy stored on the output node capacitance. Pass Transistor adiabatic logic (PAL) family exhibits considerable improvements in terms of energy savings and switching noise characteristics, it has the disadvantages of higher supply voltage and lower speed of operation.

(ii) Split Charge Recovery Logic (SCRL)

Split Charge Recovery Logic (SCRL), within which the transfer of charge between the nodes occurs quasi statically. Operating quasi statically, these logic families have an energy dissipation that drops linearly with operating frequency, i.e., their power consumption drops quadratically with operating frequency as opposed to the linear drop of conventional CMOS. The circuit techniques in these new families rely on constructing an explicitly reversible pipelined logic gate, where the information necessary to recover the energy used to compute a value is provided by computing its logical inverse. Information necessary to uncompute the inverse is available from the subsequent inverse logic stage.

4. CONCLUSION

This paper reveals the truth that there is a need of low power CMOS devices to reduce the energy dissipation. Adiabatic circuits provide a method of decreasing the energy dissipation when compared to conventional logic switching. In this paper various techniques of adiabatic logic to reduce the power dissipation have studied and explored thoroughly. Among them fully adiabatic circuits reduces the power consumption significantly but they are very complex to design , although among partially adiabatic circuits ECRL and PFAL shows the good improvement in power dissipation among other partially adiabatic logic techniques.

REFERENCES

[1] Retrieved from website: "http://science.jrank.org/pages/2376/Electronics-History.
[2] Sung-Mo Kang , Yusuf Leblebici. “Introduction” in *CMOS digital circuits: analysis and design*,3rd ed., New york: McGraw –Hill, 2003, pp.1-3.
[3] Lecture 26.Class lecture, Topic: “Power dissipation in CMOS circuits”.
[4] Amit Singh Gaur and Jyoti Budakoti. “Energy efficient advanced low power CMOS design to reduce power consumption in deep submicron technologies in CMOS circuit for VLSI design”, International Journal of Advanced Research in Computer and Communication Engineering Vol. 3, Issue 6, June 2014.
[5] Gojman, B,(August 8,2014*).Adiabatic Logic*.
[6] R.Sivakumar and D.jothhi, “Recent trends in low power design”, International journal of computer and electrical engineering”, November 2014.
[7] Deepti Shinghal, Amit Saxena and Arti Noor, “MIT International Journal of Electronics and Communication Engineering”, Vol. 3, No. 2, August 2013, pp. 108–114.
[8] Bhakti patel and Poonam Kadam, “Comparative analysis of Adiabatic logic Techniques”, International Conference on Computer Technology (ICCT), 2015.
[9] Ashmeet Kaur Bakshi, Manoj Sharma, Design of Basic Gates using ECRL and PFAL, IEEE, 2013.
[10] Sung-Mo Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits—Analysis and Design, McGraw-Hill, 2003.
[11] T. Gabara, “Pulsed Power Supply CMOS,” Technical Digest IEEE Symposium Low Power Electronics, San Diego, pp. 98- 99, October 1994
[12] W.C. Athas, J.G. Koller, L. Svensson, “An Energy- Efficient CMOS Line Driver using Adiabatic Switching,” Fourth Great Lakes symposium on VLSI, California, March 2005.
[13] Minakshi Sanadhya and M.Vinoth Kumar, “Recent development in efficient adiabatic logic circuits and power analysis with CMOS logic”, 3rd International Conference on Recent Trends in Computing 2015 (ICRTC-2015).
[14] Arpan chaudhari, Mamia saha,Moumita Bhowmik, Sambhu Nath Pradhan,Subhrajit Das , “Implementaion of circuit in different Adiabatic Logic”, presented at Ieee 2nd International Conference On Electronics and Communication System , 2015.
[15] Yasmine Badr, “Adiabatic Logic”.
[16] Munish Mittal and Anil khatak, “Design and Analysis of Energy Recovery Logic for Low Power Circuit Design” International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 National Conference on Advances in Engineering and Technology (AET- 29th March 2014*)*.