A Strategy of High Voltage Gain Switched – Capacitor DC-DC Converter with Reduced Component Rating and Count Fed DC Drive system

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Abstract- *This paper presents a strategy of bidirectional switched-capacitor dc-dc converter with high voltage gain for industrial applications. In contrast to the conventional flying capacitor dc-dc converter and multilevel modular capacitor clamped dc-dc converter, the proposed converter is completely modular with low component power rating, small switching device count, low output capacitance requirement and simpler gate drive. Therefore, a small and light weight converter with high voltage gain and high efficiency can be achieved. This paper discusses the construction and operation of new converter along with the comparison of conventional converters. Finally, proposed converter is fed to dc motor to verify its performance characteristics. Simulation results are presented to validate the concept proposed.*

Keywords- *Dc–dc power conversion, switched-capacitor, efficiency, modular, voltage gain.*

I. INTRODUCTION

Now-a-days, power converters plays a vital role in industrial applications and the new kind of converters was developing to achieve good performance with reduced loss and high efficiency. Switched-capacitor dc-dc converters have become popular due to their attractive features such as magnetic-less structure and high efficiency. Since they can be easily integrated without bulky magnetic components, the power density of dc–dc converters can be significantly boosted.

The flying capacitor dc-dc converter [1][4] has some potential features to be used in automotive applications such as hybrid electric vehicles to manage power transfer between different voltage level buses. A bidirectional 3X (i.e., the voltage gain, V_{out}/V_{in} is 3) dc-dc converter is shown in Fig.1. However with proper PWM control, it can have three voltage ratios instead of fixed 3:1 ratio. But, for convenience the dc-dc boost conversion for 3X is presented.

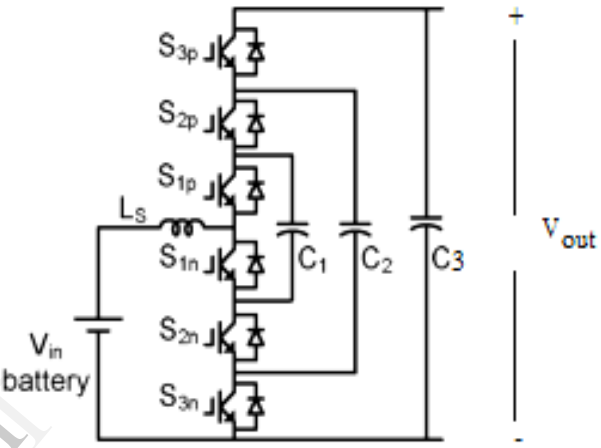


Fig.1. Flying capacitor dc-dc converter with voltage conversion ratio of three.

In construction, flying capacitor (FC) dc-dc converter requires 2N switching devices and N capacitors in incremental order of range for a voltage conversion ratio of N times (NX). From Fig.1. of 3X voltage ratio, the converter circuit requires 6 switching devices and 3 capacitors. A phase leg of complimentary switches S_{jp} and S_{jn} are connected to connect a capacitor across it for each conversion ratio. The voltage source or battery is connected at the midpoint of switching devices S_{jp} and $S_{jn.}$

The operation of FC when the desired ratio is 3X, the converter circulates from switching states I, II to III as shown in Figs.2. (a), (b) and (c) with 1/3 duty ratio per state. In State I, C_1 is connected the battery/voltage source V_{in} then $V_{c1} = V_{in.}$ In state II, the charged capacitor C_1 is in series with the battery V_{in} and connected to C_2 then $V_{c2}=V_{c1}+V_{in.}$ In State III, the charged capacitor C_2 is in series with the battery V_{in} and connected to C_3 then $V_{c3}=V_{c2}+V_{in}$. After these three states, the capacitor voltages will be balanced automatically. As a result, the output

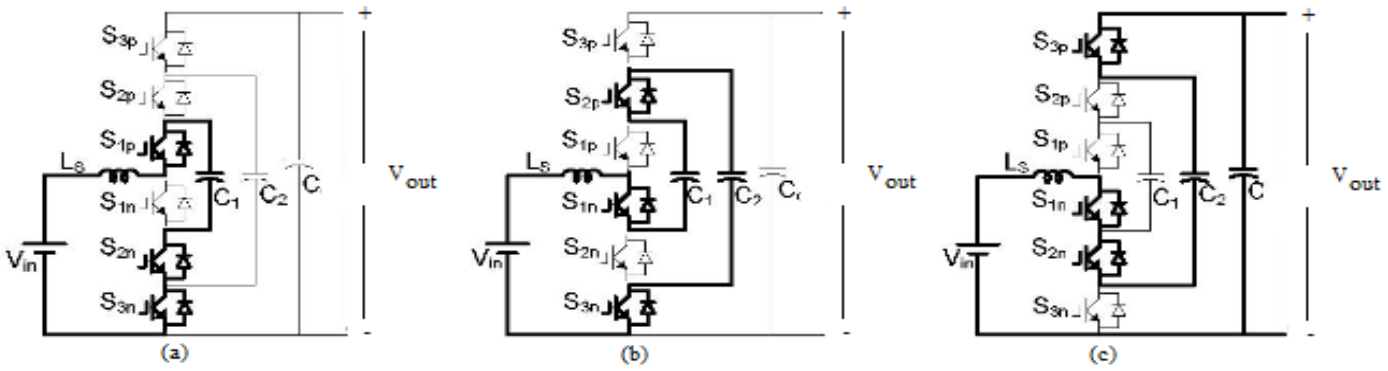


Fig.2. Switching Patterns for 3X mode: (a) Switching State I, (b) Switching state II, (c) Switching State III.

voltage is three times the input voltage. The corresponding switching states are summarized in Table1.

Table 1: Sequential conduction of switches and capacitors of FC.

Switching States	Sequential Conducting Switches			Operations or Capacitor Charge
I	S_{1p}	**S_{2n}**	**S_{3n}**	Vin↓ → C1↑
II	**S_{1n}**	S_{2p}	**S_{3n}**	Vin↓ + C1↓ → C2↑
III	**S_{1n}**	**S_{2n}**	S_{3p}	Vin↓ + C2↓ → C3↑

The Pulses Should be generated as per above sequence. It is clear that, S_{1p} as to conduct with 33% pulse width and start at 0 Sec phase delay. S_{2p} as to conduct with 33% pulse width and start at 33% Sec phase delay. S_{3p} as to conduct with 33% pulse width and start at 66% Sec phase delay. S_{1n} as to conduct with 66% pulse width and start at 0 Sec phase delay. S_{2n} as to conduct with 33% pulse width at 0 Sec phase delay and again at 66% Sec phase delay with 33% pulse width. S_{3n} as to conduct with 66% pulse width and start at 66% Sec phase delay.

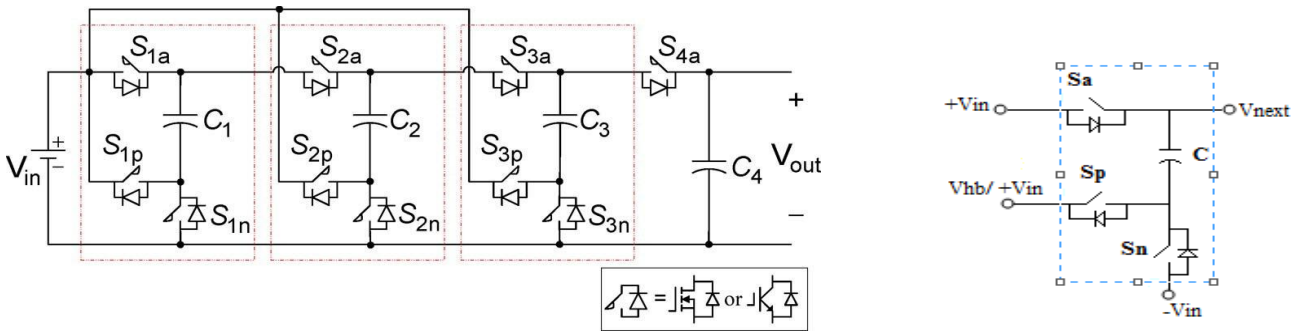
This topology is not suitable of high voltage gain since switching scheme is complicated and is not sufficient as the conversion ratio increase i.e., switching states are equal to conversion ratio N. Thus the operating frequency is limited to low when conversion ratio is high or its operation is difficulty at high frequency. The conducting switches in each sub-interval are N thus lead to excessive voltage drop across the switches/diodes. Then the dynamic switching loss is also high.

In contrast to the conventional flying capacitor multilevel dc-dc converter (FCMDC), Multilevel Modular capacitor clamped dc-dc converter topology [5]-[8] is completely modular and requires a simpler gate drive circuit. The MMCCC as shown in Fig.3.(a) is composed of three cells plus a switch S_{4a} and a capacitor C_4 connected to the output. In boost mode, it steps up the voltage from the low voltage input (defined as V_{in}) to the high voltage output (defined as V_{out}). A basic modular block is shown in Fig.3.(b).

In construction, the switch S_{ja} (j = 1, 2, 3, 4) creates a path for charging the capacitor C_j in one of two alternate switching states. The capacitor C_1 is charged by the input, V_{in}, and the other capacitor C_j (j = 2, 3) is charged via the addition of C_{j-1} and V_{in}. A phase leg of complementary switches S_{jp} and S_{jn} (j = 1, 2, 3) from each basic cell is in parallel with the input source V_{in}, in order that C_j can be directly connected to the positive (or negative) terminal of the input through just one switch S_{jp} (or S_{jn}). The switching states are reduced from four to two, since the current path becomes independent. The above review explains why the MMCCC has shorter current paths and lower current stress than the FC converter as shown in Fig.1. From another point of view, the MMCCC can be reverted to the similar form as the FC circuit and can be redrawn as in Fig.4.

In operation, interestingly, the MMCCC will perform the entire operation only in two sub-intervals. In the first sub-interval, the capacitor C_1 is charged by voltage source or battery V_{in} directly and at the same time the capacitor C_3 is charged through the series combination of battery V_{in} and capacitor C_2. Similarly in the second sub-interval, the capacitor C_2 is charged with the series combination of battery V_{in} and capacitor C_1 and also the capacitor C_4 is charged by series combination of battery V_{in} and capacitor C_3 with the proper selection of switches to be switched in the circuit. The corresponding switching states are summarized in Table 2.

The Pulses generation is as per switching sequence given in table1. It is clear that, S_{1a}, S_{1n} and S_{2p}, S_{3a}, S_{3n} has to be conduct with 50% pulse width with a



(a) (b)

Fig.3. (a) Original MMCCC with a voltage conversion ratio of four. (b) Basic Model.

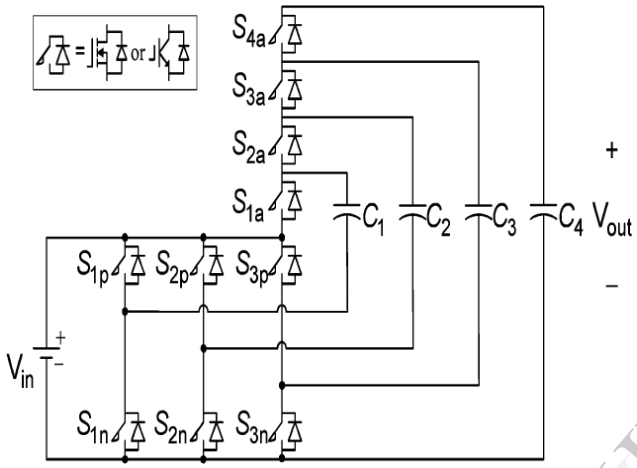


Fig.4. MMCCC in the similar form as the flying-capacitor circuit.

Table 2: Sequential conduction of switches and capacitors of MMCCC.

Switching States	Sequential Conducting Switches			Operations or Capacitor Charges
I	S_{1a}		S_{1n}	Vin↓ → C1↑
	S_{2p}	S_{3a}	S_{3n}	Vin↓ + C2↓ → C3↑
II	S_{1p}	S_{2a}	S_{2n}	Vin↓ + C1↓ → C2↑
	S_{3p}		S_{4a}	Vin↓ + C3↓ → C4↑

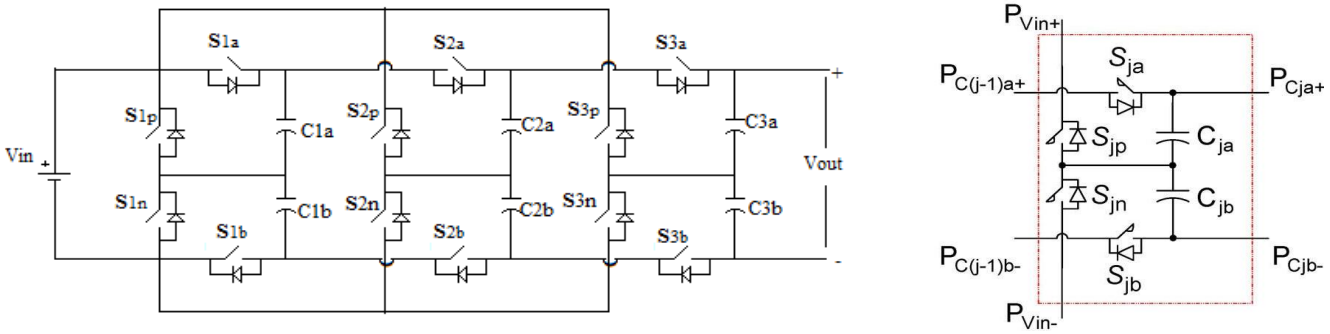
phase delay of 0 Sec. $S_{1p,}$ $S_{2a,}$ S_{2n} and $S_{3p,}$ S_{4a} has to be conduct for remaining 50% pulse width with a phase delay of 50% Sec.

The MMCCC topology has many advantageous features such as high frequency operation capability, low input/output current ripple, lower on-state voltage drop and bi-directional power flow management. Even though it suffers from such as the MMCCC require extra N-2 switching devices compared with FC dc-dc converter. The MMCCC have 3N-2 switching devices rather than 2N in conventional FC structure. Both MMCCC and FC require increased capacitor voltage with increment of the voltage conversion ratio. The different voltage rating requirement and maximum voltage rating of the capacitors pose challenges on component selection, size and efficiency when a high voltage gain is desired.

II. PROPOSED CONVERTER

The proposed switched – capacitor dc-dc converter [9] has overcome the limitations made in the both flying capacitor (FC) dc-dc converter and multilevel modular capacitor clamped dc-dc converter (MMCCC) with low switching device and capacitor power rating, small switching device count same as the FC converter, and low output capacitance requirement with the same switching scheme followed for MMCCC, thus proposed converter is most suitable for high voltage gain.

Fig.5.(a) shows the proposed switched-capacitor dc–dc converter with a voltage conversion ratio of six (named 6X). It can also function as a buck when the energy flows in the opposite direction. It is composed of three cells. In boost mode, it steps up the voltage from the low voltage input (defined as V_{in}) to the high voltage output (defined as V_{out}). The new converter can also viewed in another way as shown in Fig.6. Inside each module, a phase leg of complimentary switches S_{jp} and S_{jn} (j=1,2,3) and a pair of capacitors C_{ja} and C_{jb} are connected together at their respective mid points. Externally, another phase leg S_{ja} and S_{jb} is in parallel with the input voltage. The capacitor C_{ja} is connected through the switches S_{ja} and S_{jn} during charging along with necessary combination switches. Similarly capacitor C_{jb} is connected through the switches S_{jb} and S_{jp} during charging respectively.



(a) (b)

Fig.5. (a) Proposed 6X switched-capacitor dc–dc converter. (b) Basic Model

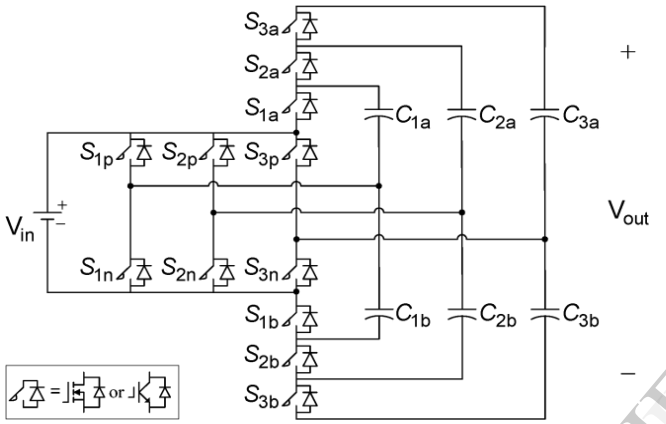


Fig.6. Another view of Proposed 6X switched-capacitor dc–dc converter.

Fig.5.(b) shows the basic model of proposed converter. Each modular block has two equal voltage rating capacitors and three switching devices for a conversion ratio of two. The terminal P_{+Vin} and P_{-Vin} are connected to the positive and negative polarities of the voltage source or battery respectively. The terminals $P_{C(j-1)a+}$ and $P_{C(j-1)b-}$ are connected to the positive and negative terminal of previous capacitors output voltage respectively. The P_{Cja+} and P_{Cjb-} are the present capacitors output voltage connected to next module switching device terminals.

This converter alternates between two switching states with 50% duty ratio for each state. The switching devices marked in solid line are on-state devices and current paths, the remaining devices in dashed lines are off-state devices. The corresponding equivalent circuits are shown in Fig.8.

In the switching state I as shown in Fig.7.(a), in the upper path, the capacitor C_{1a} is charged to V_{in} by the input through devices S_{1a} and S_{1n}, as simplified into an equivalent circuit in Fig.8.(a). The capacitor C_{2a} is in series with the input to charge the capacitor C_{3a} through the switches S_{2p}, S_{3a} and S_{3n}, as simplified in Fig.8.(b). In the lower path, the capacitor C_{1b} is in series with the input to charge the capacitor C_{2b} through the switches S_{1n}, S_{2p} and S_{2b}, as simplified in Fig.8.(c). During this time C_{3b} is discharged by the load current.

In the similar way the switching state II as shown in Fig.7.(b), the complementary switches are gated on so that the capacitors C_{2a}, C_{1b}, C_{3b} that are discharged in the first switching state become charged in the second switching state, while the capacitors C_{1a}, C_{3a}, C_{2b} become discharged. In the lower path, the capacitor C_{1b} is charged to V_{in} by the input through devices S_{1b} and S_{1b}, as simplified into an equivalent circuit in Fig.8.(d). The capacitor C_{2b} is in series with the input to charge the capacitor C_{3b} through the switches S_{2n}, S_{3b} and S_{3p}, as simplified in Fig.8.(e). In the upper path, the capacitor C_{1a} is in series with the input to charge the capacitor C_{2a} through the switches S_{1p}, S_{2n} and S_{2a}, as simplified in Fig.8.(f). During this time C_{3a} is discharged by the load current. The corresponding switching states are summarized in Table 3.

Table 3: Sequential conduction of switches and capacitors of proposed converter.

Switching States	Sequential Conducting Switches			Operations or Capacitor Charges
I	S_{1a}	S_{1n}		Vin↓ → C1a↑
	S_{2p}	S_{3a}	S_{3n}	Vin↓ + C2a↓ → C3a↑
	S_{2p}	S_{2b}	S_{1n}	Vin↓ + C1b↓ → C2b↑
II	S_{1p}	S_{1b}		Vin↓ → C1b↑
	S_{3p}	S_{3b}	S_{2n}	Vin↓ + C2b↓ → C3b↑
	S_{1p}	S_{2a}	S_{2n}	Vin↓ + C1a↓ → C2a↑

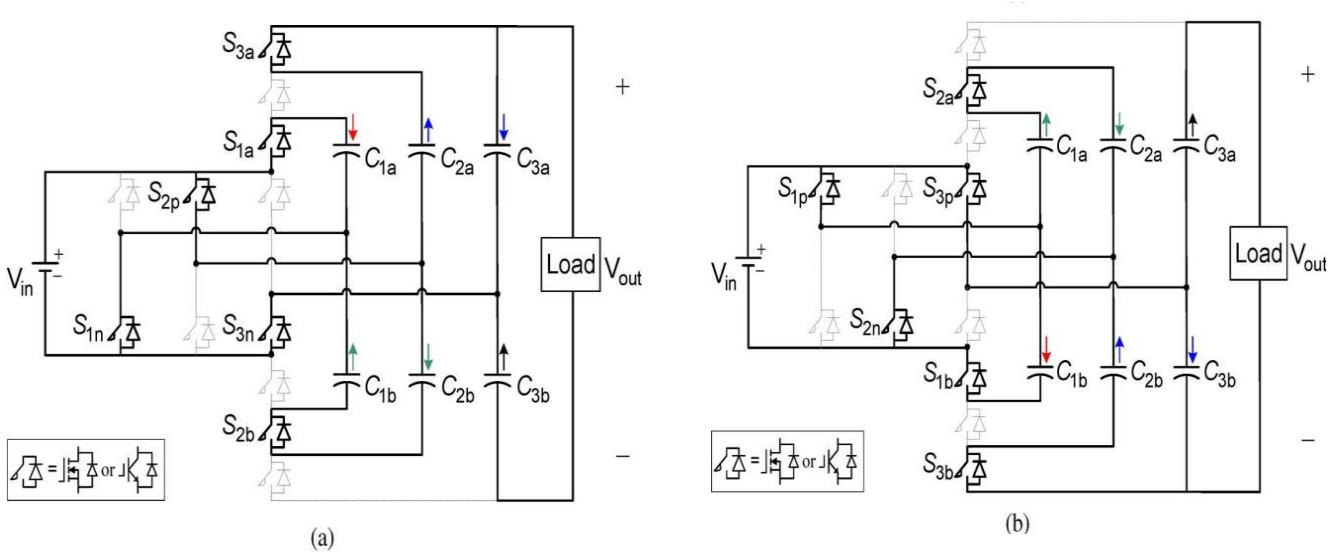


Fig.7. (a) Switching state I. (b) Switching State II.

The Pulses Should be generated as per above sequence given in table 3. From the above, it is clear that, S_{1a}, S_{1n}, S_{2p}, S_{3a}, S_{3n} and S_{2b} has to be conduct with 50% pulse width with a phase delay of 0 Sec. S_{1p}, S_{1b}, S_{3p}, S_{3b}, S_{2n} and S_{2a} has to be conduct for remaining 50% pulse width with a phase delay of 50% Sec.

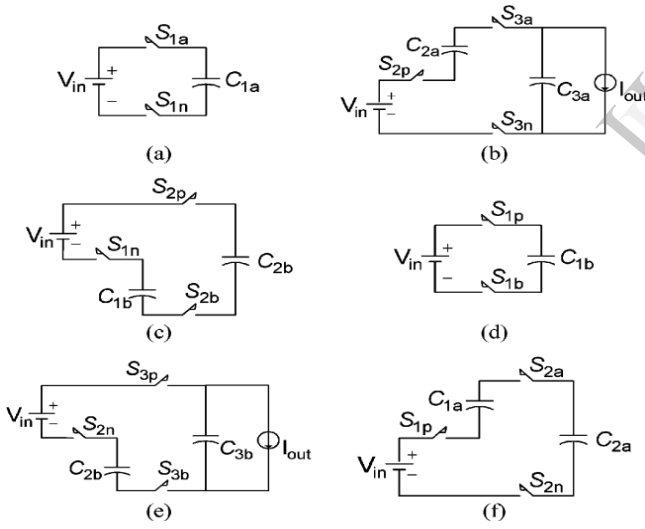


Fig.8. Equivalent circuits for two switching states. (a) Charging C_{1a}. (b) Charging C_{3a}. (c) Charging C_{2b}. (d) Charging C_{1b}. (e) Charging C_{3b}. (f) Charging C_{2a}.

Combining the voltage relations in the two switching states and neglecting the voltage drop, one can get the following voltage relations:

$$V_{cja} = V_{cjb} = j * V_{in}, \quad j = 1, 2, 3. \quad \ldots\ldots\ldots (1)$$

The proposed converter is beneficial such as the switching devices required is only 2N for conversion ratio of N, thus it has low component switching devices. The capacitors required is N as that of FC and MMCCC but the capacitor voltage required is lesser since the two similar capacitor ratings equal to input voltage are enough for output voltage to be double instead of one capacitor with the input voltage rating and the other is double the input rating as in FC and MMCCC. The power loss is very less due to low component switching devices, low capacitor power ratings in addition with two symmetric short charge pumps. The voltage (or current) stress is low since device count is less and thus low TDPR. The bidirectional operation is possible along with simpler switching scheme. Thus it is modular structure make it use for high voltage gain applications at lower cost.

III. COMPARISON

In the comparison, Table 4, the most suitable converter is denoted by the bold letters in all comparative aspects. From the table 4, it is clear that the number of switching devices required is less as 2N in both flying capacitor and proposed converter. The number of switching states and number of switches to be conduct to charge a capacitor is maximum of 3 only in both multilevel modular capacitor clamped converter and new converter. The number of capacitors required is N which is same in all the three converters but the highest capacitance required is less as (N/2)*Vin and total capacitance required is also less as (((1+N/2)N)/2)*Vin in only proposed converter. Thus in all aspects mentioned above the proposed converter is efficient, least cost, less losses converter for high voltage gain applications.

Table 4: Comparison of FC, MMCCC and Proposed Converters.

Converter	**No. of Switching Devices**	**No. of Switching States**	**No. of Switches to be conduct to charge a capacitor**	**No. of Capacitors Required and Highest Capacitance range (Vin=12V)**	**Total Capacitance Voltage Rating**
Flying Capacitor (For N=6)	**2N (12)**	N (6)	N (6)	N and N*Vin (6 and 72V)	(1+N)N * Vin / 2 (= 252V)
MMCCC (For N=6)	3N-2 (16)	**2 (2)**	**At Most 3 (At Most 3)**	N and N*Vin (6 and 72V)	(1+N)N * Vin / 2 (= 252V)
Proposed Converter (For N=6)	**2N (12)**	**2 (2)**	**At Most 3 (At Most 3)**	**N and (N/2)*Vin (6 and 36V)**	**(1+N/2)N*Vin / 2 (= 144V)**

Now, the proposed converter is employed to feed the dc motor to study its performance characteristics. The motor chosen was the separately excited dc motor with the desired parameters as: Rating of 5 hp, Voltage of 240V, Current of 16.2 A and speed of 1220rpm. To drive this motor the 6X proposed converter is having a input voltage Vin of 40V is used then the output voltage Vout will be a constant of 240V. The separately excited dc motor is one of the most important drives in industrial application. The study of dc motor characteristics is illustrated in the simulation results.

IV. COST CONSIDERATIONS

The cost considerations of the proposed converter are compared with its conventional converters in the aspects as the TDPR, the capacitor voltage stress, current rating, and capacitance requirement. TDPR is an indication of how much total silicon area is needed for the semiconductor devices. Here, it is based on the product of the maximum voltage imposed on the device and the average current flowing through it over the duration when the device conducts. Note that neither the peak current nor RMS current is used.

1) If the 3X FC dc–dc converters are extended to an NX structure, all the 2N devices would have to sustain the voltage equal to the input voltage and the input current. Its TDPR is the same as the traditional boost converter

$$TDPR_{FC} = 2N*(Vin*Iin) = 2N\ Pin$$

where V_{in} is the input voltage and I_{in} is the input current.

2) The MMCCC have switching states reduce to two. The charge current into one capacitor is the discharge current from its preceding capacitor, except that the output capacitor has half the charge and discharge currents. Also, considering that the average charge current of one capacitor in half switching period equals its average discharge current in the other half switching period, the average current through each switching device is $2I_{out}$ in one of the two switching states. There is (N-2) switches sustain twice the input voltage, as stated earlier. Thus, the TDPR is

$$TDPR_{MMCCC} = 2N*Vin * 2Iout + (N-2) * 2Vin * 2Iout$$
$$= ((8N - 8) / N)\ Pin, \quad N= 2, 3, 4\ldots.$$

3) For the new converter, the (N-2) switches in the complementary phase leg convey the sum of the current in two charge pump paths, $4I_{out}$, which is twice the current through the rest switches. It is not hard to find the voltage stress of each switch. Hence, the TDPR can be derived as:

$$TDPR_{NEW} = (N-2)Vin*4Iout+(2+2)Vin*2Iout$$
$$+ (N-2) * 2Vin * (2Iout)$$
$$= ((8N - 8) / N)\ Pin, \quad N= 2, 4, 6\ldots.$$

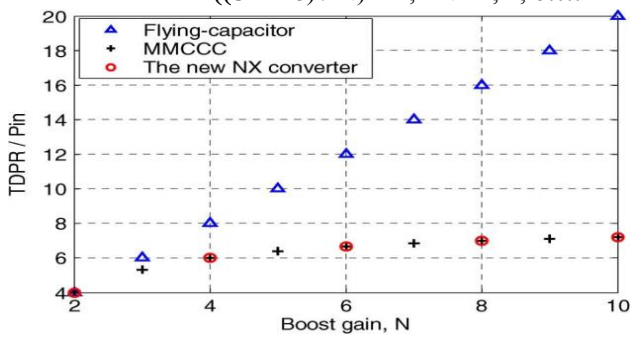


Fig.9. Normalized total device power rating versus voltage boost gain.

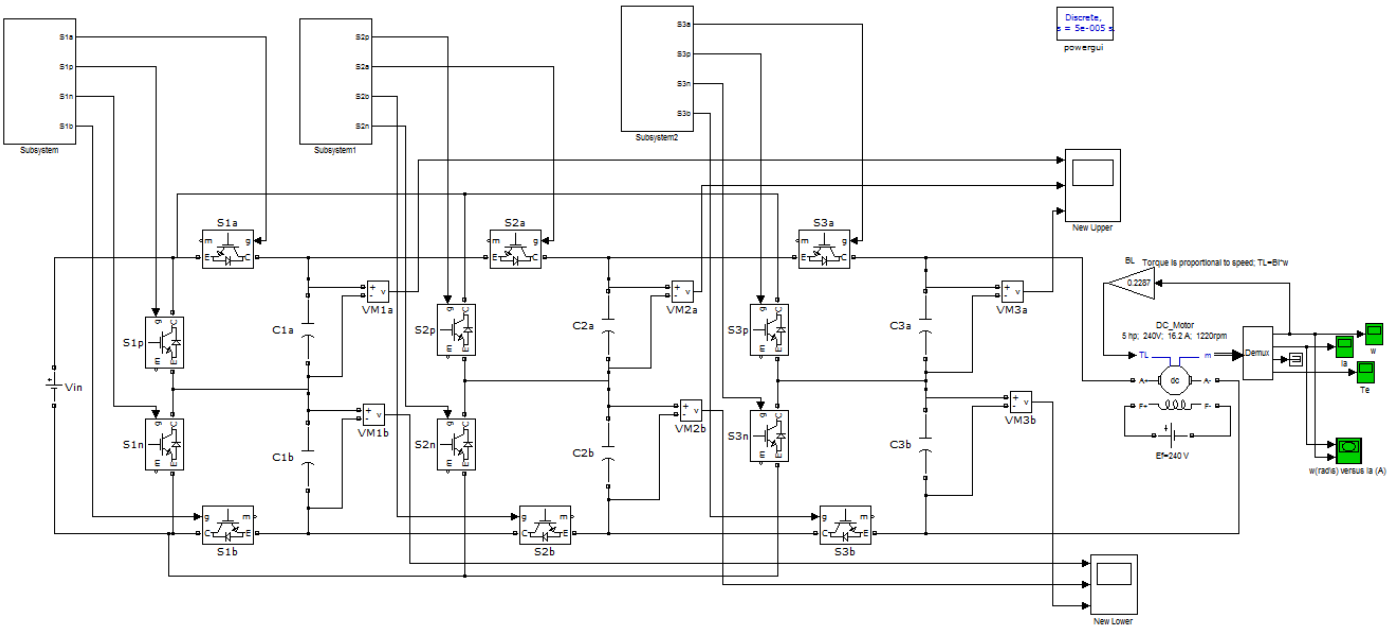


Fig.10. Simulation model file of 6X proposed converter fed dc separately excited motor.

The above equations clearly demonstrate that unlike the conventional FC structure, the new converter has no penalty of TDPR even with fewer devices than the MMCCC. The ratio of the TDPR and the input power is plotted with respect to voltage gain in Fig.9. It is quite interesting that this ratio for the new converter will get saturated as N approaches infinite. This property implies that the proposed converter requires less silicon area than the FC dc–dc converter does. the voltage ratings for the FC and the MM-CCC are the same, the voltage rating for the new converter is reduced nearly by half as illustrated in table 4.

V. SIMULATION RESULTS

The proposed switched – capacitor dc-dc converter along with the conventional flying capacitor dc-dc converter and multilevel modular capacitor clamped dc-dc converters have been designed with the common switching frequency of 10 KHz and input voltage of 12V. The capacitance of capacitor at the corresponding input voltage V_{in} is chosen in the order of 500uF, 240uF, 120uF and 60uF as C1, C2, C3 and C4 respectively for all three converter designs. The simulation results are shown for three different converters to justify to content.

Fig.10. shows the simulation model file of 6X proposed converter fed dc separately excited motor. The proposed converter fed dc separately excited motor is chosen as the separately excited dc motor with the desired parameters as: Rating of 5 hp, Voltage of 240V, Current of 16.2 A and speed of 1220rpm (= 127.758 rad/sec).

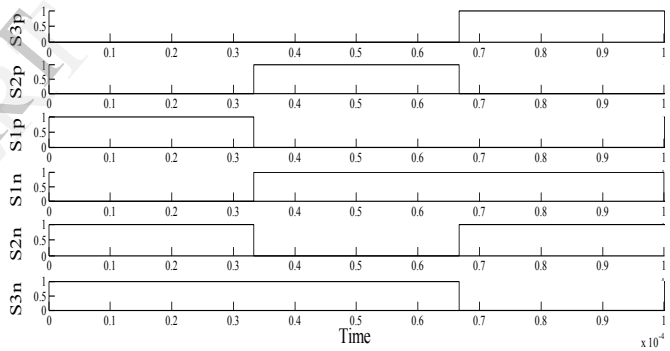


Fig.11.Simulated results of gate pulses of 3X FC Converter.

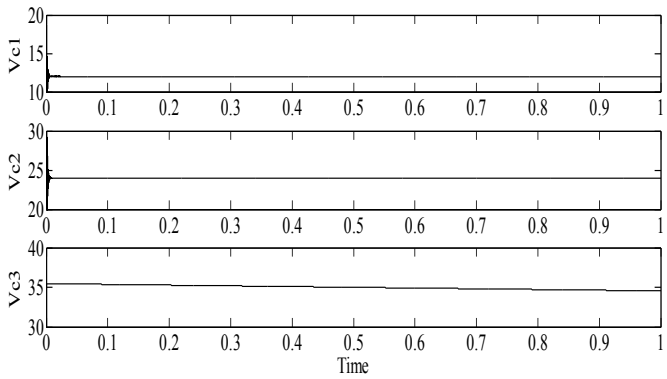


Fig.12.Simulated results of capacitor voltages of 3X FC converter.

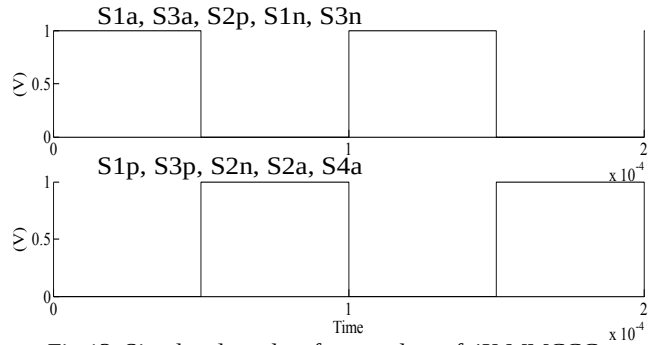


Fig.13. Simulated results of gate pulses of 4X MMCCC.

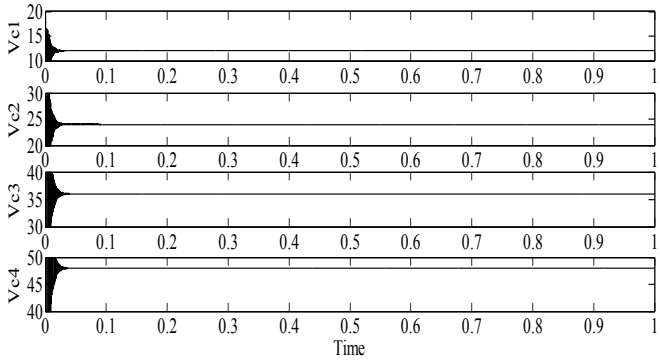


Fig.14.Simulated results of capacitor voltages of 4X MMCCC.

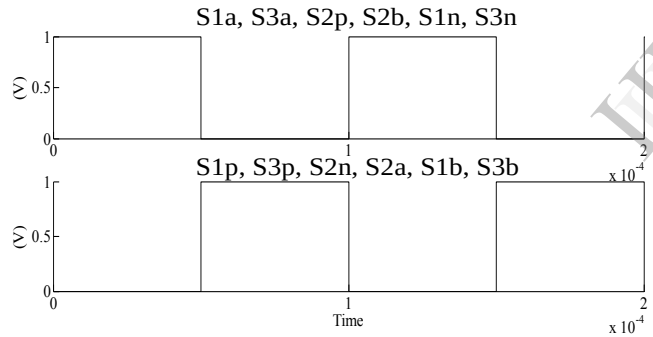


Fig.15.Simulated results of gate pulses of 6X proposed converter.

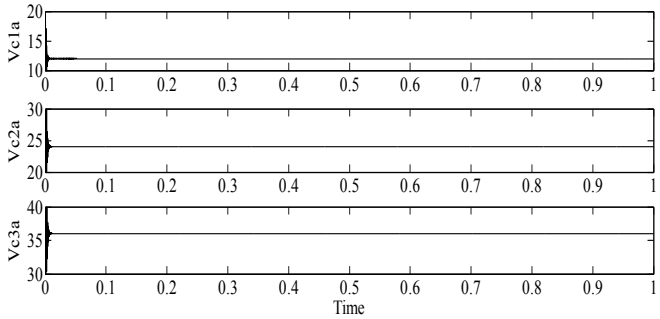


Fig.16.Simulated results of upper leg capacitor voltages of proposed converter.

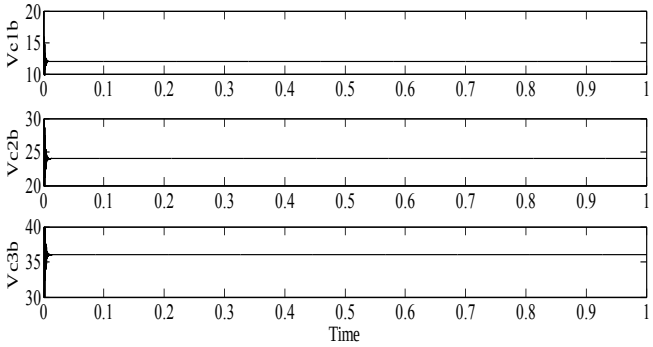


Fig.17.Simulated results of lower leg capacitor voltages of proposed converter.

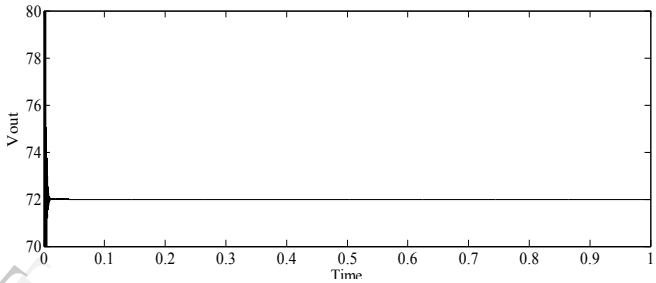


Fig.18.Simulated result of combined capacitor voltages of output capacitors of proposed converter.

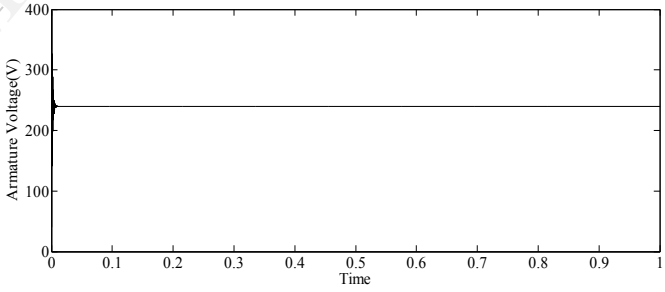


Fig.19.Simulated result of armature input voltage of proposed converter fed dc motor.

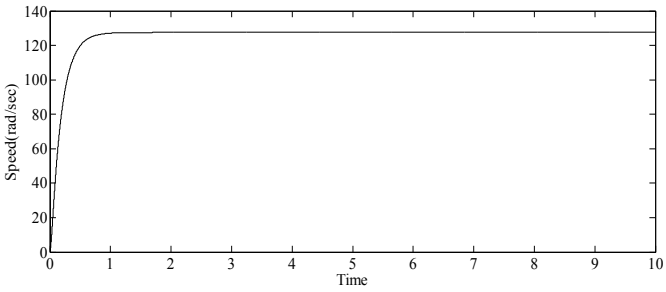


Fig.20.Simulated result of speed characteristics of the proposed converter fed dc motor.

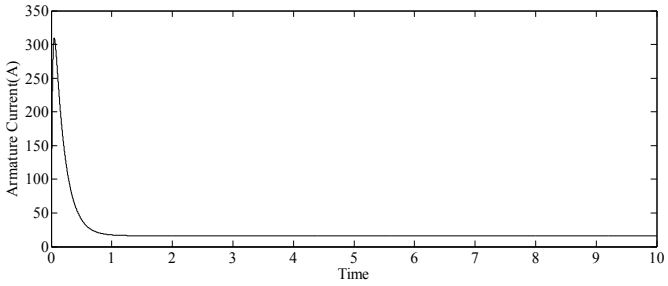


Fig.21.Simulated result of armature current characteristics of the proposed converter fed dc motor.

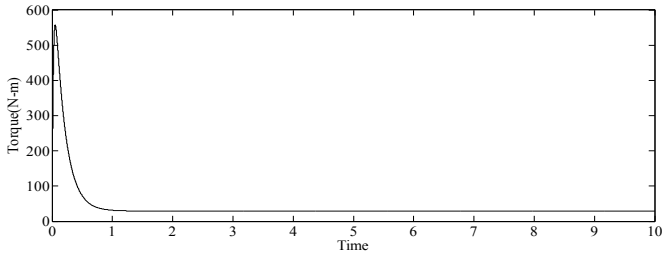


Fig.22.Simulated result of torque characteristics of the proposed converter fed dc motor.

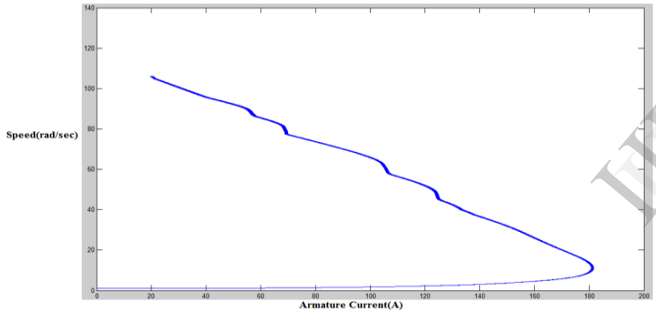


Fig.23.Simulated result of speed vs armature current characteristics of the proposed converter fed dc motor.

VI. CONCLUSION

The proposed strategy of high voltage gain switched-capacitor dc–dc converter is compared with conventional switched-capacitor dc–dc converter as counterpart along with the validate simulation results of each converter. Thus the proposed converter is completely modular with less power loss due to the two symmetric short paths of charge pumps, less component power rating, small switching device count, low TDPR, reduces total capacitor voltage ratings, lowers capacitance and ripple current requirement of the output capacitors, simpler gate drive and high frequency operation. Finally, a small and light weight, high voltage gain, high efficiency and low cost proposed switched – capacitor dc-dc converter is most suitable for industrial applications.

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