A Simple Application of FM0 Encoding in DSRC Applications

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***Abstract*:- The dedicated short-range communication (DSRC) system is the evolving technique used in the field of intelligent transport system (ITS) and Electronic Toll Collection (ETC). The DSRC standard employs FM0 encoding techniques to obtain dc-balance and enhances signal reliability. The codeword structure of FM0, thus limiting the hardware potential of existing DSRC systems. Dedicated short-range communications are one-way or two-way short-range to medium-range wireless communication channels specifically designed for automotive use and a corresponding set of protocols and standards. The performance of this paper is evaluated on the simulation Using Xilinx. The maximum operation frequency is 900 MHz for FM0 encodings. The power consumption is 1.14 mW at 900 MHz for FM0 encoding. The encoding capability of this paper can fully support the DSRC standards of America, Europe, and Japan.**

Index Terms— Dedicated short-range communication (DSRC), FM0, VLSI, intelligent transport system (ITS).

I. INTRODUCTION

FM0 technique is used to encode the data while transmit the signal through medium. Using FM0 coding, we developed the reused VLSI hardware architecture. Since, encoding plays the vital role in secured communication. Developing architecture for such encoding techniques is need of the hour. One sort of renowned and commonly used communication technique is DSRC (Dedicated Short Range Communication) which is designed support the variety of applications. Based on vehicular environments communication. DSRC, the subset of RFID (Radio Frequency Identification) for tracking and identification.

DSRC standards adopts both FM0 and Manchester encoding for signal reliability and dc balance. A new Manchester code generator designed at transistor level is presented by Benabes [1] . This generator uses 32 transistors and has the same complexity as a standard D flip-flop. It is intended to be used in a complex optical communication system.The main benefit of this design is to use a clock signal running at the same frequency as the data. Output changes on the rising edge and falling edge of the clock. Automotive industry is moving aggressively in the direction of advanced active safety. Dedicated short-range communication (DSRC) is a key enabling technology for the next generation of communication-based safety applications. One aspect of vehicular safety communication is the routine broadcast of messages among all equipped vehicles presented by J. Daniel[2] . Therefore, channel congestion control and broadcast performance improvement are of particular concern and need to be addressed in the overall protocol design. Furthermore, the explicit multichannel nature of DSRC necessitates a concurrent multichannel operational scheme for safety and non-safety applications provides an overview of DSRC based vehicular safety communications and proposes a coherent set of protocols to address these requirements.

The Radio Frequency Identification System (RFID) is becoming one of the most popular system in wireless technologies. The UHF RFID tag emulator is a part of RFID testing tools. The UHF RFID tag Emulator would be imitating the behavior of RFID Tag[3]presented by manoj Sharma.The main benefit of this design is the use of a clock signal running at the same frequency as the data presented[4] by A. Karagounis Output changes on the rising edge and falling edge of the clock. [5]Yu-Cherng Hung proposed a modified Manchester and Miller encoder that can operate in high frequency without a sophisticated circuit structure. Based on the previous proposed architecture, the study has adopted the concept of parallel operation to improve data throughput.

M.Ayob khan presented [6]high-level architecture of tag emulator and the design of FM0 encoder and Miller encoder. As motivated by Finite State Machine, encoders are discussed with particular focus to use the RFID Emulator as data transport device and debugging tool. With the release of FCC NPRM 13-22 (Docket 13-49), the United States Federal Communications Commission has proposed allowing unlicensed devices such as Wi-Fi to share the 5.9 GHz ITS band which is currently allocated for DSRC. [7] John B. Kenney explains the content and status of the DSRC standards being developed for deployment in the United States. He proposed, which would create a new set of rules for the band that would become U-NII-4, requires the unlicensed devices to recognize the existence of DSRC systems and defer to them. if Dedicated Short Range Communications (DSRC) at 5.9 GHz, in combination with vehicle positioning, can improve upon autonomous vehicle-based safety systems and/or enable new communications-based safety applications. This was given by F. Ahmed-Zaid [8] explained how these standards fit together to provide a comprehensive solution for DSRC.

A Bletsas[9] derived and evaluated single-antenna detection schemes for collided radio frequency identification (RFID) signals, i.e. simultaneous transmission of two RFID tags, following FM0 (biphase-space) encoding. Manchester coding and decoding (CODEC) schemes are proposed for dedicated short range

communication (DSRC) systems over high mobility fading channels presented by J.-H. Deng and F.-C. Hsiao[10]. Jim Lansford proposed, which would create a new set of rules for the band that would become[11] U-NII-4, requires the unlicensed devices to recognize the existence of DSRC systems and defer to them.

II. CODING PRINCIPLES OF FM0

The coding principles of FM0 and Manchester encoder are discussed as follows,

A. FM0 encoding:

FM0 encoding is also called as bi-phase space encoding scheme. In FM0 encoding, the signal to be transmitted and done according , to the following rules, It inverts the phase of the base band signal at the boundary of each symbol.

- For representing logic '0' level, it inverts the signal at the mid of the symbol.
- For representing logic '1' level, it constant voltage occupying an entire bit window

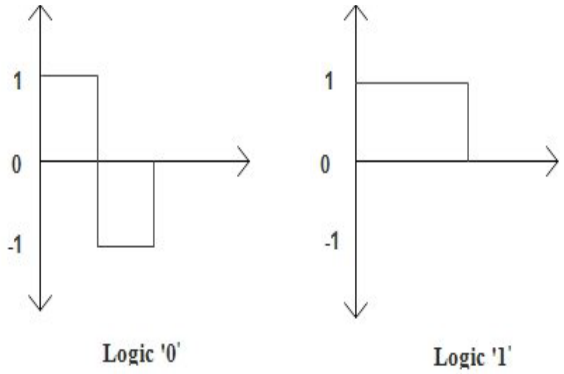
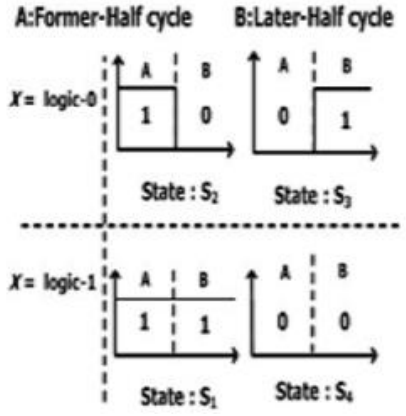


Fig1: Fm0 encoder rules.

THE STATE CODE PRINCIPLE FOR FM0:

The FM0 code starts with the FSM principle. The FSM of FM0 code classified into four states.

The four states as shown in the below figure.



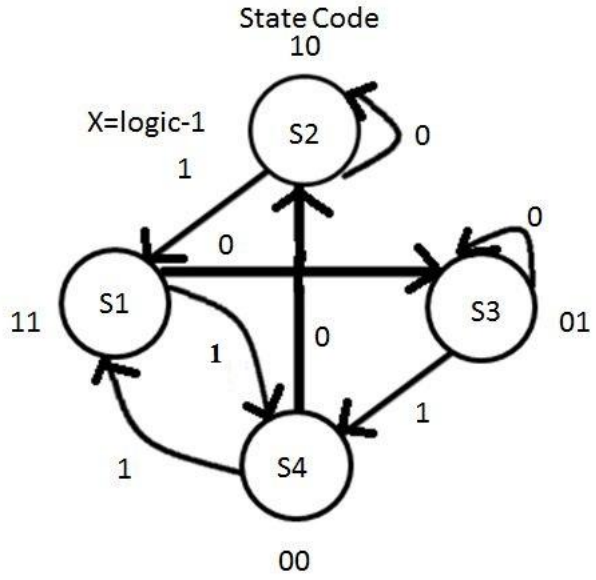


Fig2: State machine representation.

FSM of FM0 uppose the initial state is S1, and its state code is 11 for A and B, respectively.

1) If the X is logic-0, the state-transition must follow both rules for FM01 and 3. The only one next-state that can satisfy both rules for the X of logic-0 is S3. If the X is logic-1, the state-transition must follow both rules for FM0 2 and 3. The only one next-state that can satisfy both rules for the X of logic-1 is S4. Thus, the state-transition of each state can be completely constructed. The FSM of FM0 can also conduct the transition table of each state A(t) and B(t) represent the discrete-time state code of current-state at time instant t. Their previous-states are denoted as the A(t − 1)and the B(t − 1), respectively. With this transition table, the Boolean functions of A(t) and B(t) are given as

2) $A(t) = B(t-1)$ $B(t) = X \oplus B(t-1)$With both A(t) and B(t), the Boolean function of FM0 code is denoted as CLK A(t) +~ CLK B(t)

Previous state		Current state			
A(t-1)	B(t-1)	A(t) X=0	X=1	B(6) X=0	X=1
1	1	0	0	1	0
1	0	1	1	0	1
0	1	1	0	1	1
0	0	1	1	0	1

Table 1: Transition table.

III. HARDWARE ARCHITECTURE OF FM0 CODE:

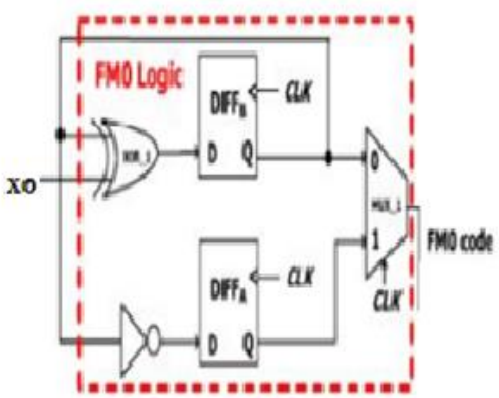


Fig3: Hardware architrecture.

This is the hardware architecture of the fm0 code. In fm0 code the DFFA and DFFB are used to store the state code of the fm0 code and also mux_1 and not gate is used in the fm0 code. When the mode=0 is for the fm0 code.

IV. FMO ENCODER USING SOLS TECHNIQUE

The SOLS technique is classified into two parts area compact retiming and balance logic operation sharing

A. area compact retiming:

For fm0 the state code of the each state is stored into DFFA and DFFB .the transition of the state code is only depends on the previous state of B(t-1) instead of the both A(t-1) and B(t-1).

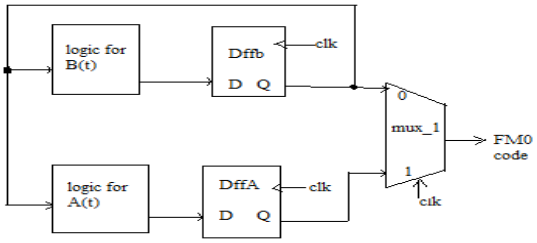


Fig4: Area compact retiming.

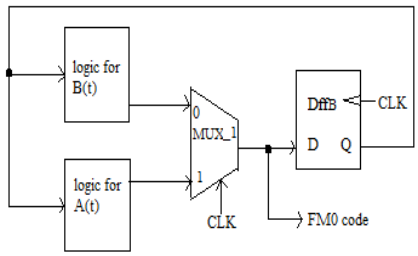


Fig5:FM0 encoding without area compact retiming.

The previous state is denoted as the A(t-1) and then cthe B(t-1).and then the current state is denoted as the A(t) and then the B(t)

V. MEMORY ORGANIZATION

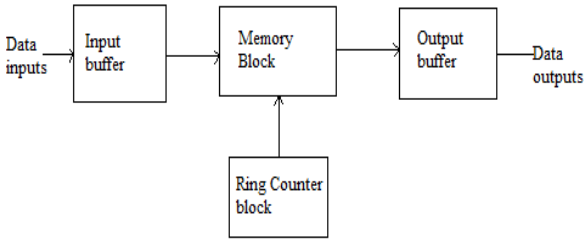


Fig6: Block diagram.

a) INPUT BUFFER

The Input buffer is also commonly known as the input area or input block. When referring to computer memory, the input buffer is a location that holds all incoming information before it continues to the CPU for processing. Input buffer can be also used to describe various other hardware or software buffers used to store information before it is processed.

b) MEMORY BLOCK

(RAM) Random-access memory (RAM) is a form of computer data storage. Today, it takes the form of integrated circuits that allow stored data to be accessed in any order (that is, at random). "Random" refers to the idea that any piece of data can be returned in a constant time, regardless of its physical location and whether it is related to the previous piece of data

c) RING COUNTER

A **ring counter** is a type of counter composed of a circular shift register. The output of the last shift register is fed to the input of the first register.

VI. SIMULATION RESULTS

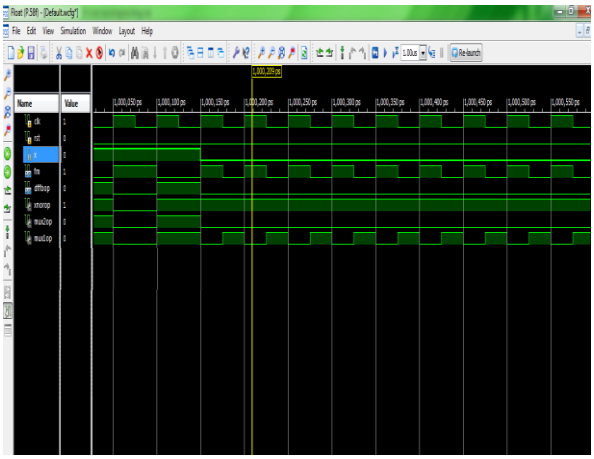


Fig7: Output wave forms.

VII. CONCLUSION

Using FM0 encoding techniques, hardware architecture is to be developed. FM0 coding are very popular code, as these codes are level insensitive, self-clocking and they provide signal absence detection and having the encoding clock rate embedded within the transmitted data. They encode the data as 1's and 0's. FM0 code is balance logic operation sharing along with clock gating technique. This deduced architecture of FM0 coding would well support the DSRC standards.

VIII. REFERENCES

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