A Robust and Reconfigurable Multi-Mode Power Gating System to Reduce Static Power Loss

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Abstract **- Multithreshold Complementary Metal Oxide Semiconductor (MTCMOS) is very effective for reducing standby leakage power during long periods of inactivity. A power-gating scheme was used to provide multiple power off modes and reduce the leakage power during short periods of inactivity. This scheme can suffer from high sensitivity to process variations of logic. We propose a new power-gating technique that is tolerant to process variations and scalable to more than two intermediate power-off modes.The Tanner Electronic Design Automation (EDA) tool is used to design the schematic for multiplier with power gating system.It is very simple and all-digital, and it is minimally sized. It consumes low static power. It has high tolerance to manufacturing process variations. The proposed design requires less design effort and offers greater power reduction and smaller area cost than the previous method.In addition, it will be combined with existing method to offer further static power reduction.The schematic design is to generate the waveform and produce some power consumption. A reconfigurable version of this method can be used to increase the manufacturability and robustness of the proposed design in technologies with larger process variations.**

Key words—Leakage power, MMPS, power consumption reduction, Tanner EDA, process variation.

I.INTRODUCTION

Multi-threshold CMOS is a budding know-how that provide high concert and low command function by utilizing both high and low V_t transistors. By low V_t transistors in the indication lane, the provide voltage can be lowered to diminish switching power indulgence. By dipping V_{dd}, the switching influence can be condensed quadratic ally, but as V_t decreases to continue routine, the sub entrance seepage contemporary will increase exponentially. For ruthless scaling, the better outflow supremacy can really direct the switching power. Recently, several dealer goods in the low command fixed liberty offer power-gating bear in the appearance of "sleep" modes, typically software run. One of numerous supercomputer cores, in such as arrangement, runs at the greatest in use regularity and the other mainframe cores can be power-gated off when the working classification detects a elongated inoperative loop. The destructive power-saving line of attack above, but, has the follow probable harms.

The scaling of development technologies to nanometer administration has resulted in a rapid make bigger in seepage power rakishness. Hence, it has befallen enormously significant to extend devise techniques to diminish fixed clout debauchery all through periods of immobility. The power lessening must be achieved devoid of trading-off show which makes it harder to reduce leakage during normal operation. On the other hand, there are several techniques for reducing leakage power in sleep or standby mode.This device is turned-off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides asubstantial reduction in leakage at a minimal impact on performance.

II. RELATED WORK

As chip density increases relentless along Moore law, power consumption is emerging as a major burden for contemporary systems [1] , To reduce the dynamic power, systems-on-chip (SoCs) are partitioned into voltage islands with separate supply rail and unique power characteristics [2]–[4].

Many techniques have been presented in the literature for reducing static power. One common approach is to synthesize the circuit using dual-$V_t$libraries [6]. High-$V_t$cells reduce the leakage current at the expense of reduced performance; in order to reduce static power, it controls the input vector and the internal state of the circuit during periods of inactivity [7]–[11].

Various techniques reduce peak rush current [22]–[25]. A more aggressive technique is the use of high- $V_t$power switches between the circuit and the power supply or the ground rail [6], [12]–[20]. These switches are turned off during the idle mode, thereby suppressing leakage current. A major problem is the large current rush during the re-activation of the core, which causes power supply and ground bounce [21], [22].

The authors of [28] proposed a structure with one intermediate power-off mode, which reduces the wake-up time at the expense of reduced leakage current suppression. Similar structures were proposed in [27] and [29]. The authors of [26] extended this tradeoff between wake-up overhead and leakage power savings into multiple power-off modes. Using these techniques, instead of consuming power by remaining in the active mode during the short periods of inactivity, the circuit is put into an appropriate power-off mode (i.e., low-power state), which is determined by both the wake-up time and the length of the idle period.

In this work, we present an effective and robust multimode power-gating architecture that has none of the above drawbacks of the architecture proposed in [26]. The proposed structure requires minimal design effort since it is very simple, and with no analog components. It is

considerably smaller than the architecture proposed in [26] and offers greater power savings for similar wake-up times. The proposed architecture is also more tolerant to processvariations than [26], thus its operation is more predictable. Finally, a reconfigurable version of the proposed architecture is also proposed, which can tolerate even greater process variations, enabling thus the utilization of the proposed architecture for newer technologies.

III. PROBLEM FORMULATION

The offered makeup requires least design endeavor seeing as it is exceedingly undemanding, and among no analog machinery. It is very much slighter than the planning accessible and offers superior control reserves for like awaken period. The projected construction is also added liberal to course variations; thus its action is more conventional. In vacant means four methods are there. In this methods are

- Active Mode
- Snore Mode
- Dream Mode
- Sleep Mode

A.ACTIVE MODE

- Transistors MP, M0, M1 are ON.

B.SNORE MODE

- Transistors MP , M0, and M1 are OFF.

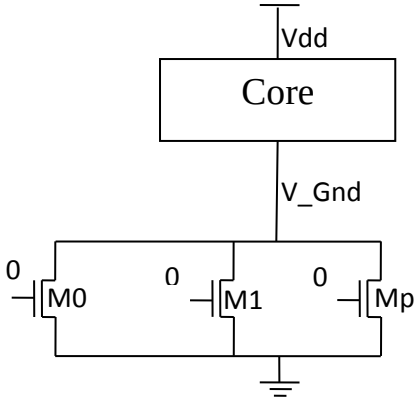

Fig.1 Snore mode

- The escape topical of the nucleus I Lcore, is the same to the amassed flight modern elegant throughout transistors M0, M1, MP (I Lcore = I LM0 + I LM1 + I LMP), which is very minute.
- The power plane at V_GND is secure to V_{dd} and the course consumes a small total of vigor, but the wake-up instance is elevated.

C.DREAM MODE

- Transistor M0 is on and transistors MP and M1 are OFF.
- In this holder, the contemporary smooth during transistor M0 increases as M0 is on (IM0 > I LM0).
- The exact value of IM0 depends on the size of transistor M0, VV_GND < V_{dd}. Thus the static power consumed by the core is higher compared to the snore mode, but the wake-up time is less.

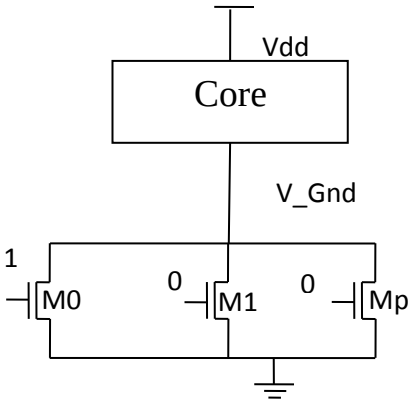

Fig.2 Dream mode

D.SLEEP MODE

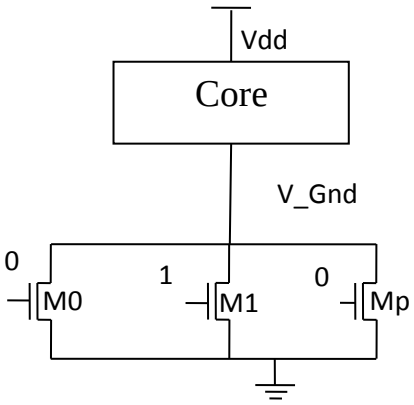

Fig.3 Sleep mode

- Transistor M1 is on, and MP, M0 are OFF.
- The transistor M1 has larger aspect ratio than M0 (WM1/LM1 > WM0/LM0), the aggregate current flowing through M0, M1, and MP increases even more when M1 is on.
- Consequently, the voltage level at the virtual ground node is further reduced compared to the dream mode and thus the wake-up time decreases at the expense of increased power consumption.

IV. SYSTEM DESCRIPTION

Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off

the current to blocks of the circuit that are not in use. In addition to reducing stand-by or leakage power, power gating has the benefit of enabling I_{ddq} testing.

A.MULTIMODE POWERGATING SYSTEM

The offered makeup requires least design endeavor seeing as it is exceedingly undemanding, and among no analog machinery. It is very much slighter than the planning accessible and offers superior control reserves for like awaken period.
The projected construction is also added liberal to course variations; thus its action is more conventional. In vacant means four methods are there. In this methods are

- Active Mode
- Snore Mode
- Dream Mode
- Sleep Mode
- Nap Mode

B.ACTIVE MODE

- Transistors MP, M0, M1 and M2 are ON.

C.SNORE MODE

- The virtual ground rail (V_GND) charges to a voltage level VSnore close to the power-supply.
- The leakage currents of the transistors of the circuit are suppressed. In this mode the leakage current of the core, ILcore, is equal to the aggregate leakage current flowing through transistors M0, M1, M2, MP (ILcore = ILM0 + ILM1 + ILM2 + ILMP), which is very small.
- Thus, the voltage level VSnore at virtual ground rail VV_GND approaches V_{dd} and the circuit consumes a negligible amount of energy.

In order to restore the voltage of the virtual ground rail to its nominal value when the circuit N transitions from the power-off mode to the active mode, the parasitic capacitance at the V_GND node has to be completely discharged through the power switch MP which is turned-on again.

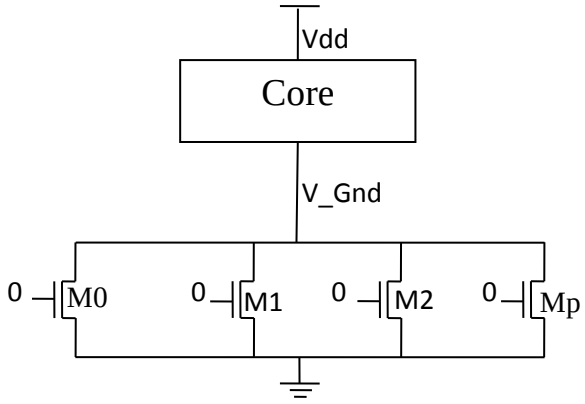

Fig.4 Snore mode

However, the aggregate size of the transistors comprising the power switch MP is relatively small compared to the size of the core and thus it cannot quickly discharge the V_GND node. Thus the wake-up time can be long relative to circuit clock period, and MP cannot be turned-off during short periods of inactivity.

D.DREAM MODE

- The current flowing through transistor M0 increases compared to the snore mode because M0 is on (IM0 > ILM0).
- The exact value of IM0 depends on the size of transistor M0, and it sets the V_GND node at a voltage level VDream which is lower than that of the snore mode (VDream < VSnore).
- Thus the static power consumed by the core increases compared to the snore mode, but the wake-up time drops.

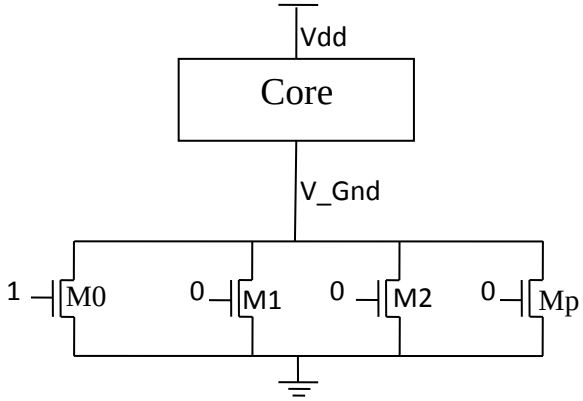

Fig.5 Dream mode

E.SLEEP MODE

- The sleep mode is implemented by decreasing the voltage level at the virtual ground node.
- This is achieved by using transistor M1 which has larger aspect ratio than M0 (WM1/LM1 > WM0/LM0).
- When only M1 is turned-on the aggregate current flowing through M0, M1, and MP increases even more and the voltage level VSleep at the virtual ground node is further reduced compared to the dream mode (VSleep < VDream < VSnore).

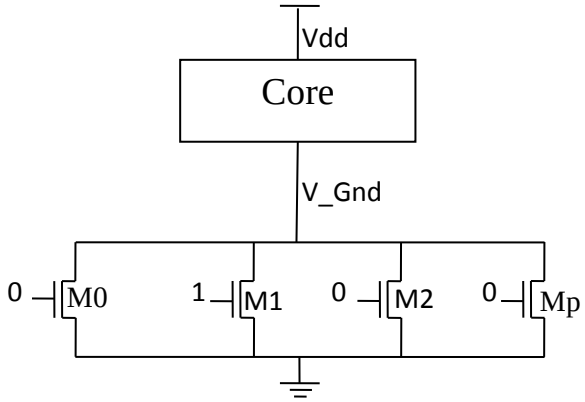

Fig.6 Sleep mode

- The wakeup time decreases at the expense of increased static power consumption, which however, remains much lower than the static power of the active mode.

F.NAP MODE

- The "nap" mode is implemented by further increasing the aspect ratio of the respective power switch (i.e., WM2/LM2 > WM1/LM1 > WM0/LM0).

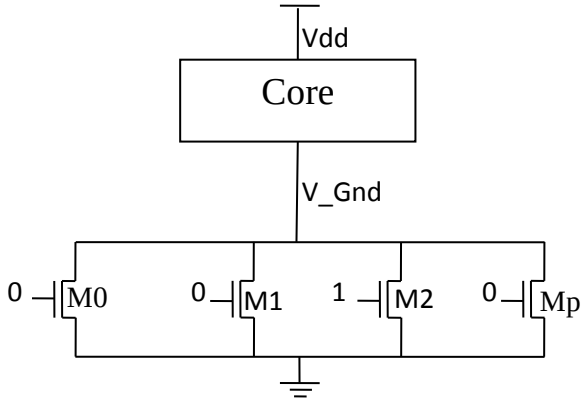

Fig.7 Nap mode

- In nap mode the voltage level at V_GND node is set at VNap, where VNap < VSleep < VDream < VSnore.
- The static power consumption increases and the wake-up time reduce even more.

V. RESULT AND DISCUSSION

The system can be implemented using Tanner EDA tool. A 4×4 multiplier circuit can be used as a logic circuit and ground of logic can be connected on the Power switches. Various mode of operation can be simulated and its ground voltage can be calculated.

Table (1):Power consumption for various modes

Mode	Ground voltage(v)	Power (mW)
Snore Mode	1.85	25
Sleep Mode	1.65	33
Nap Mode	0.95	37
Dream Mode	0.45	44

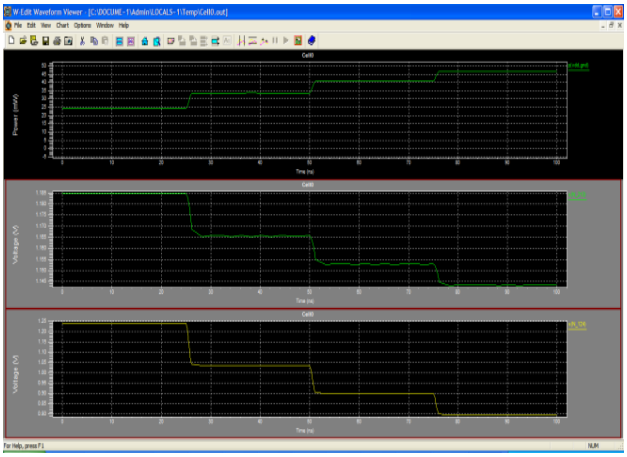

Fig.8 power Gating system Output

In future we have to use multimode power gating system to reduce Dynamic power loss and also reduce the Delay. Otherwise, A new low voltage charge pump is developed to help start up a step-up converter in energy harvesting applications.

VI.CONCLUSION

Amultimode power-gating system is used to reduce the static power loss.In this scheme that provides multiple power-off modes. The proposed design offered the advantage of simplicity and required minimum design effort. Extensive simulation results showed that, in contrast to a recent power-gating method, the proposed design is robust to process variations and it is scalable to more than two intermediate power offmodes. Moreover, it requires significantly less area and consumes much less power than the previous design.

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