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A Review Paper on Design of Positive Edge Triggered D Flip-Flop using VLSI Technology

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***Abstract* - A Delay (D) flip-flop is an edge triggering device. A high speed, low power consumption, positive edge triggered Delay (D) flip-flop can be designed for increasing the speed of counter in Phase locked loop, using VLSI technology. The designed counter can be used in the divider chip of the phase locked loop. A divide counter is required in the feedback loop to increase the VCO frequency above the input reference frequency. The propose circuit will be faster than conventional circuit as it will be a fast reset operation. The circuit will be consuming less power as it prevents short circuit power consumption.**

Keywords - PLL, D-ff, PFD and VCO.

I. INTRODUCTION

The D flip-flop is an important part of the modern digital circuit. Flip flop can be regarded as a basic memory cell because it stores the value along the data line with the vantage of the output being synchronized to a clock. Flip flops are used as registers. D flip flop is a best choice for storage registers. The many logic synthesis tool use only D flip flop or D latch. The working of D flip flop is similar to the D latch except that the output of D Flip Flop takes the state of the D input at the moment of a positive edge at the clock pin (or negative edge if the clock input is active low) and delays it by one clock cycle. That's why, it is commonly known as a delayed flip flop.

The proposed work would be a brief overview of Phase Locked Loop (PLL). A phase locked loop with an excellent performance widely studies in recent years. Frequency divider and PFD are indispensable modules of PLL, which uses D flip-flop as an integral component. Edge Triggered D flip flops are often implemented in integrated high speed operations using dynamic logic. This means that the digital output is stored in the parasitic device capacitance while the device is not transitioning. This design of dynamic flip flops also enables simple resetting since the reset operation can be performed by simply discharging one or more internal nodes. The conventional D flip-flop which uses E-TSPC (True signal phase clock) logic has higher operating frequencies but it features static power dissipation. However, this causes a small increase in power dissipation, since at the frequencies of interest dynamic power consumption is dominant. In the proposed circuit dynamic power consumption was reduced by lowering internal switching and speed is increased by shortening input to the output path.

II. PHASE LOCKED LOOP (PLL)

Phase locked loop is generally used in wireless communication and data recovery circuits. At present, for the above mentioned application a low voltage, low area and high performance integrated circuits are used which complicates the execution of such type of integrated circuit.

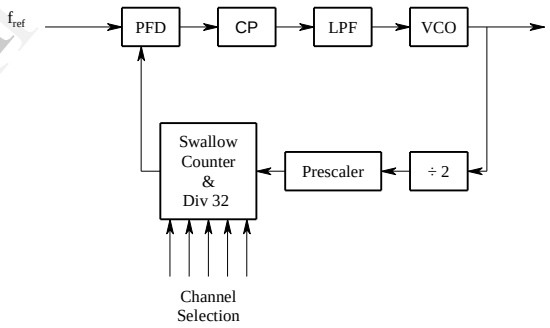

Fig. 1Block diagram of PLL

A PLL is a control system that generates a signal that has a fixed relation to the stage of a "reference" signal. A phase-locked loop circuit responds to both the frequency and the phase of the input signals, automatically raising or lowering the frequency of a controlled oscillator until it is coupled to the character in both frequency and phase. Phase locked loops are built of a detector, charge pump, low pass filter, voltage-controlled oscillator (VCO) and frequency divider placed in a negative feedback closed-loop configuration. A phase detector compares two input signals and produces an error signal which is proportional to their phase difference. The error signal is then low-pass filtered and used to drive a voltage-controlled oscillator (VCO) which creates an output frequency. The output frequency is fed through a frequency divider back to the input of the system, creating a negative feedback loop. If the output frequency drifts, the error signal will increase, driving the VCO frequency in the opposite direction so as to reduce the error. Thus the output is locked to the frequency of the other input.

A. *Phase Frequency Detector*

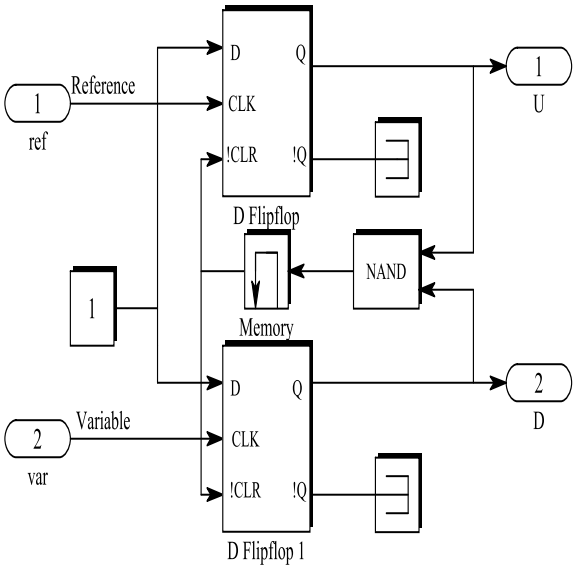

Fig. 2 Block diagram of PFD

A phase frequency detector (PFD), is a device which compares the phase of two input signals and provides a signal in the form of phase error. It accepts two inputs which correspond to two different input signals, usually one from a voltage-controlled oscillator (VCO) and the other is a reference source. It has two outputs which instruct subsequent circuitry on how to adjust to lock onto the phase. A charge pump circuit is used to convert the digital signal from the phase frequency detector to an analog signal, the output of which is used to control the frequency of the voltage control oscillator. To form a phase-locked loop (PLL), the phase error output of PFD is fed to a charge pump and then to loop filter which integrates the signal to get a sharper and smoother signal so that the disturbances at the input of VCO get minimized. As can be ascertained from the following diagram, the D flip-flop is an integral part of pfd. Hence, to make the operation of PFD faster, a fast D flip-flop is required.

B. *Frequency Divider*

Frequency divider divides the VCO frequency to generate a frequency which is compared with reference frequency. In the block diagram PLL, the prescaler and swallow counter together acts as a frequency divider. D flip flop is an integral part of both of them.

C. *Voltage Controlled Oscillator*

A voltage-controlled oscillator or VCO is an electronic oscillator whose oscillation frequency is controlled by a voltage input. The applied input voltage determines the instantaneous oscillation frequency. Consequently, modulating signals applied to control input may cause frequency modulation (FM) or phase modulation (PM). A VCO may also be part of a phase-locked loop.

D. *Low Pass Filter*

A low-pass filter is a filter that passes low-frequency signals. Attenuates signals with frequencies higher than the cutoff frequency. The actual amount of attenuation for each frequency varies depending on specific filter design. It is sometimes called a high-cut filter, or treble cut filter in audio applications. A low-pass filter is the opposite of a high-pass filter. A band-pass filter is a combination of a low-pass and a high-pass.

Low-pass filters exist in many different forms, including electronic circuits, anti-aliasing filters for conditioning signals prior to the analog-to-digital conversion, digital filters for smoothing sets of data. Also for acoustic barriers, blurring of images, and so forth. The moving average operation used in areas such as finance is a particular kind of low-pass filter, and can be analyzed with the same signal processing techniques as are used for other low-pass filters. Low-pass filters provide a smoother form of a signal, removing the short-term fluctuations, and leaving the long-term trend. An optical filter can correctly be called a low-pass filter, but is conventionally called a long pass filter (low frequency is long wavelength), to avoid confusion.

III.RELEATED WORK

From the rigorous review of related work and published literature, it is noted that many researchers have designed D flip flop for Phase Locked Loop (PLL) by using different techniques like analog and digital simulation applying mathematical/logical relations. Researchers have undertaken different systems, processes or phenomena with regard to design and analyze performance of D flip flop and attempted to determine the unknown parameters. Since in the real world today VLSI/CMOS is in very much in demand, from the careful study of reported work it is observed that very few researchers have taken a work for designing a D flip flop for PLL with CMOS/VLSI technology.

In 1998, R. J. Bakcer, H. W. Li and D. E. Boyce proposed CMOS design, layout and simulation [1]. They introduced the technology, design and simulation of CMOS integrated circuits. The proposed evolution of integrated circuit (IC) manufacturing techniques is a unique fact in the history of modern manufacture. The improvements in terms of speed, density and cost kept constant for more than 30 years. By the end of 2004, "System-on-Chips" with about 300,000,000 transistors will be fabricated on a single piece of silicon no larger than 2x2 cm. This proposed work presented some information illustrating the technology scale down.

In 1999, Won-Hyo Lee and Jun- Dong Cho proposed a high speed and low power phase frequency detector and charge pump [2]. The publisher introduced a high speed and low power Phase Frequency Detector (PFD) that is designed using modified TSPC (True Signal Phase Clocked) positive edge triggered D flip flop. This PFD has a simpler structure by utilizing only 19 transistors. The proposed PFD is independent of the duty cycle of input signals. A new charge-pump circuit is presented that is designed using a charge-amplifier. The input phase errors are detected by Phase Detector (PD) or Phase Frequency Detector (PFD).

These phase or frequency errors are converted into current or voltage to control the output frequency of a Voltage Controlled Oscillator (VCO) by the charge pump in a charge - pump PLL. PD detects a phase error between the reference signal and the output signal of the PLL. And the error detection range can be extended with PFD. This PFD has a large dead zone in phase characteristics at the steady state which generates a large jitter in locked state in PLL. Also, they discussed a large amount of power consumption cannot be avoided in high frequency operations because internal nodes of PFD are not completely pulling up or tear down.

In 2002, Yubtzuan Chen, Chih Ho Tu and Jein Wu proposed a CMOS phase/frequency detector with a high speed, low power D type master slave flip fop [3]. A high-speed low-power CMOS D-type master-slave flip-flop is proposed and adopted in the PFD. Higher speed and lower power operation are attributed to the reduced node capacitance. Charge-sharing phenomena are circumvented in the proposed PFD. The proposed PFD shows improvement in frequency sensitivity at high operating frequency. The proposed PFD is suitable for high-speed low-power operation.

In 2011, K. G. Sharma, Tripti Sharma, B. P. Singh and Manisha Sharma proposed modified SET D flip flop design for low power VLSI application [4]. The designed low power device is now a vital field of research due to increase in demand of portable devices. This researched paper proposed the modified Single Edge Triggered (SET) D-flip flop design for the portable applications. Design is tested for various substrate bias voltages in the sub - threshold region to opt for better design. The comparison between previously reported design and modified design is performed at 65nm and 45nm to show technology independence. Comparative simulation results show that area and power efficient SET D-FF design is the best choice for portable applications.

In 2011, S. Jagannathan and T. D. Loveless, implemented the single event tolerant flip flop design in 40nm bulk CMOS technology [5]. The radiation response of a single-event tolerant flip-flop design named the Quatro flip-flop is presented. They designed circuit level simulations on the flip-flop show 1) the critical charge of the sensitive nodes to be greater than that of DICE flip-flop, 2) the number of sensitive nodes and the sensitive area to be less than that of DICE flip-flop. A test-chip designed and fabricated in the 40-nm bulk CMOS technology node consisting of Quatro, DICE, and the standard D flip flop was used for heavy-ions, neutrons, and alpha particle exposures. The resulted experimentally demonstrate superior performance of the Quatro flip-flop design over conventional DICE and D-flip-flop designs.

In 2012, R. H. Talwekar and S. S. Limaye, proposed a high speed, low power consumption, positive edge triggered D flip flop for high speed phase frequency detector in 180nm CMOS technology [6]. A survey of D flip flop for the PLL is presented by Talwekar in his paper. Both classical and modem approaches are discussed. He suggested that although the design of the PLL is fairly well documented, more needs to be done to pinpoint the formal design of the D-PLL, the primary use of the PLL has been in more sophisticated communication systems, however, with the rapid development of IC Technology, time is not far when PLL's will be used widely in consumer electronics. The designed counter has been practiced in the divider chip of the phase locked loop.

In 2013, Mathan N, Ravi T, and Kannan V., proposed low power single edge triggered D flip flop based shift register using VLSI technology [7]. They analyzed of average power, delay and power delay product was produced in various shift registers (SISO, SIPO, PISO and PIPO) using this technology. Low power flip-flops is crucial for the design of low-power digital systems. As Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices are reduced to nanometer ranges, Complementary MOS (CMOS) circuit's total Power consumption has a new definition. Due to integration of millions of components and shrinking process technology, nowadays leakage power tends to play a major role in total power consumption. In this report, the shift registers are designed using VLSI technology with 1GHz and 2GHz frequencies and their performance are examined.

IV.PROPOSED WORK

The proposed study will be to design, the positive edge triggered D- flip flop in a VLSI technology. Also, some work done thereafter on this, but that is not sufficient so we are designing a new D-flip flop. By using this technique the required percentage of power consumption is low and also the speed of performing the procedure is high.

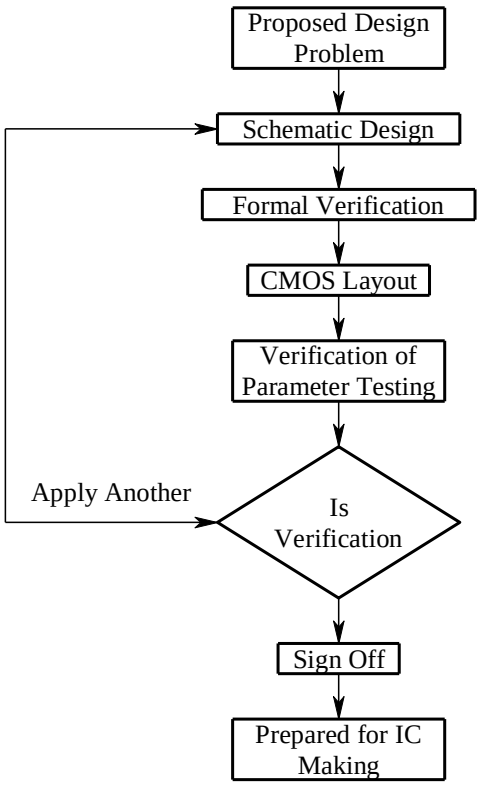

Fig.6. Flow chart of proposed work

V. CONCLUSION

We could offer a positive edge triggered D flip flop in VLSI technology. In the proposed circuit dynamic power consumption will reduce by lowering internal switching and also speed will be increased by shortening input to the output path. It has numerous advantages such as: increase the speed, efficient timing and low power consumption.

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