A Review paper on Approach of Low Cost Digital Test Stimulus Generation for Sigma Delta ADC Built-in Self-Test

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***Abstract*-Design issues of analog to digital converter play very important role in mixed signal design and SoC. Testing of a SoC (System on Chip) is a challenging task, especially for its growing analog and mixed-signal core. In this paper, we have reported a brief review on different BIST approach for sigma-delta ADC to measure offset error and gain error of sigma-delta modulator. This review is made up of a generator of stimulus and an analyzer of response. We compare a digital technique for the test of static characteristics of the modulator with existing work. A shift register based signal generator is reported which can concurrently produce test stimulus and reference signals.**

Keywords: BIST; Mixed Testing; ADC converter; Stimulus generator; Sigma delta modulator; Analyser; Soc.

I. INTRODUCTION

The task of testing a VLSI chip to guarantee its functionality is extremely complex and very time-consuming. The problem of testing the chips themselves, the combination of the chips into systems has caused test generation's cost to grow exponentially. Built-in self-test (BIST) is widely accepted approach to deal with the testing problem at the chip. This increases the controllability and the observability of the chip, thereby making the test generation and fault detection easier.

In conventional testing, test patterns are generated externally by using computer-aided design (CAD) tools. The test patterns and the expected responses of the circuit under test to these test patterns are used by automatic test equipment (ATE) to determine if the actual responses match the expected ones. On the other hand, in BIST, the test pattern generation and the output response evaluation are done on the chip; thus, the use of expensive ATE machines to test chips can be avoided.

The paper is organized as follows: Section 2describes Sigma Delta ADC Testing. Section 3 describes The Basic Built-in Self-Test (BIST) Structure. Section 4 discusses previous work regarding testing Delta Sigma converters. Section 5 describes proposed work and finally the conclusions are drawn in Section 6.

I. SIGMA DELTA ADC TESTING

ADC testing can roughly be divided into two separate parts, static and dynamic testing. In static testing, the converter under test is subjected to a series of dc voltage levels and the output values are monitored to determine the converters accuracy. One major limitation in static testing is that nonlinearities related to the input signal bandwidth may pass undetected.

Dynamic testing is when the converter is stimulated by periodic waveforms instead of dc levels. This type of testing is usually better suited for production testing due to easier signal generation and less time-consuming behaviour. The signal bandwidth can be higher than in static testing and thereby resembling the actual applications signal. However one disadvantage is that dynamic tests are usually not deterministic in nature, the analog input is not compared to the resulting digital code; instead the converter transfer function is interpreted from the resulting out data. To ensure sufficient resolution under test, the signal source needs a resolution at least 3-bit greater than the device under test. (IEEE_Std_1241, 2001)

II. THE BASIC BUILT-IN SELF-TEST (BIST) STRUCTURE

A basic BIST configuration is shown in Figure 1. The main function of the test pattern generator is to apply test patterns to the unit under test (assumed to be a multi-output combinational circuit). BIST increases the controllability and the observability of the chip, thereby making the test generation and fault detection easier. The resulting output patterns are transferred to the output response analyzer. Ideally, a BIST scheme should be easy to implement and must provide high fault coverage.

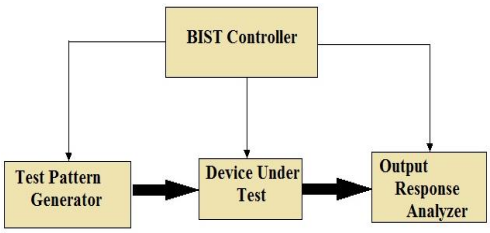

Fig. 1 Basic BIST configuration

BIST controller is used to control the whole testing process. The test pattern generator and output response analyser can be modified according to accuracy and area of the chip.

III. LITERATURE REVIEW

A number of research papers of various journals and conferences were studied and survey of existing literatures in the proposed area is reported below:-

In [2], describes a method for obtaining a short periodic approximation of the PDM pattern and identifies two methods of integrating this analog test scheme into the current digital test environment: scan-based storage and RAM. Using such design for test logic as the 1149.1-1990 JTAG architecture and a typical RAM BIST controller, these

analog signal generation techniques can be added to digital integrated circuits (IC's) with minimal additional hardware overhead, and also explained two memory-based PDM techniques which utilize an arbitrary finite-length bit pattern for analog signal generation.

In [3], demonstrated a new method for generating analog signals with very low complexity and hardware requirements. It consists of periodically replicating short optimized bit streams recorded from the output of a sigma–delta modulator. A technique to generate sine waves and other signals with small hardware area and simple circuits is presented. It consists of reproducing periodically the output of a sigma–delta modulator with some memory on the IC and also demonstrated the various types of signals that can be generated with the bit stream approach.

In [4], proposed a built-in self-test structure to test the static parameters of analog to digital converters (ADCs). To serve the test stimulus, they used ramp signal generated by an integrator.A specific range of signal is divided into2+1 segment, with each segment corresponding to one output combination of a n+1-bit counter, where n is the number of bits of the ADCs under test. The testing process is ended with digital data processing by comparing the outputs of ADCs under test with the outputs of the n+1-bit counter. The advantages of this structure are less area overhead, High speed, Simple structure.

In [5], explained a BIST scheme for testing on-chip AD and DA converters. On-chip generation of linear ramps as test stimuli for measuring the DNL and INL of the converters. The proposed BIST scheme in this work employs the delta-sigma modulation technique to generate the required linear ramp for testing the converters.For ADC testing, proposed BIST strategy is "linear histogram testing" and measure differential/integral nonlinearities (DNL/INL). For DAC testing, proposed test scheme that employs an analog comparator and two counters for measuring the DAC parameters. The DAC BIST strategy is immune from the common offset voltage of the analog comparator since it is cancelled out in the analysis process and thus has little effect on the test accuracy also.

In [6]**,** measure the four key parameters of A/D converters, namely offset error, and gain error, integral nonlinearity error and differential nonlinearity error. In proposed scheme, a sigma-delta modulation based signal generator is used which can concurrently produce analog sinusoidal test stimuli and digital sinusoidal reference signals on a chip. By comparing the sinusoidal histogram of the ADC output signals with that of the generated reference digital signals, the testing parameters can be determined on-chip also in signal generator is implemented on-chip which not only can supply a high quality analog signal to the A/D converters under test, but also is able to concurrently produce a digital reference signal without any extra area overhead. Based on this real-time generated reference, there is no need to calculate the reference histograms in apriority, nor is it necessary to store the histograms of any fixed frequencies.

In [7], new architecture for the sigma-delta modulator so that its performance can be determined using only digital test stimulus. This architecture does not require analog test stimuli, which is prone to distortion while setting up the high-resolution modulator to perform testing. Simulation results show that this technique is capable of accurately determining the performance of a second-order sigma–delta modulator ADC. A sigma–delta DFT architecture that can be tested with a digital signal. This feature eliminated the need to generate an analog signal, which can be costly for high-resolution modulators.

In [8], presented a low-cost BIST scheme based on linear histogram for testing ADC. A parallel time decomposition technique is used to minimize hardware overhead, it also minimize the testing time of the BIST scheme based on histogram. To generate the on-chip precise analog stimulus and simplify the analog circuit of the generator at same time, the technique digital delta-sigma noise shaping is used. Triangular waveform is used for test stimulus. The scheme follows the concept of time decomposition to reduce the area overhead of analyser. Regarding increasing testing time in the scheme of time decomposition, the parallel time decomposition technique is proposed further to reduce testing time of the ADC BIST based on the linear histogram.

In [9], proposed a Built-In Self-Test (BIST) technique for the test of SNDR (Signal-to-Noise plus Distortion Ratio) in ΣΔADCs. The technique is mostly digital, uses a bit stream as test stimulus and carries out a sine-wave fitting algorithm to analyse the output response. The test signal generation and the output response analysis both are performed on-chip. Simulations results show the capability of this technique to obtain measures of the SNDR for a 16-bit audio ΣΔADC.A 4^{th} order since filter has been used instead of a 3^{rd} order in the decimation filter. Equally, larger digital paths have been employed in the last stages of the decimation filters. Two possible implementations have been presented, for ICs with or without a memory. In both cases, the test time is much reduced (0.03s). Only an additional attenuated reference voltage and several switches need to be added in the analogue modulator.

In [10], presented a Built-In Self-Test (BIST) methodology to measure offset error and gain error of sigma-delta modulator. This structure is made up of a generator of stimulus and an analyser of response. A memory-based signal generator is presented which can concurrently produce test stimuli and reference signals. Contribution is the detection of the static parameters by analysing the output bit stream of the 1-bit first-order sigma-delta modulator in order to have a logic test decision. This technique can be easily implemented, since the digital sequence stored in memory can be at the same time the digital test stimulus and test reference. Hence, testing of the static characteristic of the modulator under test with a simple response analyser by comparing the real bit stream output with the ideal one.

Study of more than 10 research papers can be summarized in following manner:-

- Most of the researchers have addressed static specifications of the sigma-delta modulator.
    - Offset error.

- Gain error.
- Differential nonlinearities.
- Integral nonlinearities.

- Different types of test stimulus generator were used such as:-
  - Ramp type stimulus generator.
  - Sinusoidal type stimulus generator.
  - Bitstream or digital bit generator.
  - Triangular type stimulus generator.
  - Memory-based stimulus generator.
- Different types of tester or analyser were used.
  - Histogram based.
  - Counter based.
  - Memory-based.
  - Shift resister based.
- Different order of sigma-delta modulator are is tested such as-
  - First order sigma delta modulator.
  - Second order sigma delta modulator.
- Parameter used to estimate the performance is: SNR, SNDR, dynamic range, power consumption, FOM, resolution, bandwidth, hardware cost, oversampling ratio.
- Digital bit stream pattern generator takes very less area on a chip.
- Sigma delta modulator can beused in form of pattern generator.
- Ramp stimulus generator is depending on the accuracy of integrator.
- Memory based built in self-test takes a large area.

A. *Problem Identification*

After reviewing the papers we find that there are some limitations in the process taken. Some of them are –

- There is a tread off between area, complexity and speed.
- Complex circuit consumes more power.
- Analog stimulus generator requires digital to analog converter.
- Bitstream or digital bit in memory takes more area and makes the testing process complex.
- Ramp stimulus generator is depending on the accuracy of integrator.
- Complex computation and more number of input pins.

IV. PROPOSED METHODOLOGY

Figure 2 is showing the basic building blocks of complete testing for sigma-delta analog to digital converter. Major blocks areTest Stimulus Generator, Sample & Hold circuit, Mux, Response Analyzer, Devices under test.

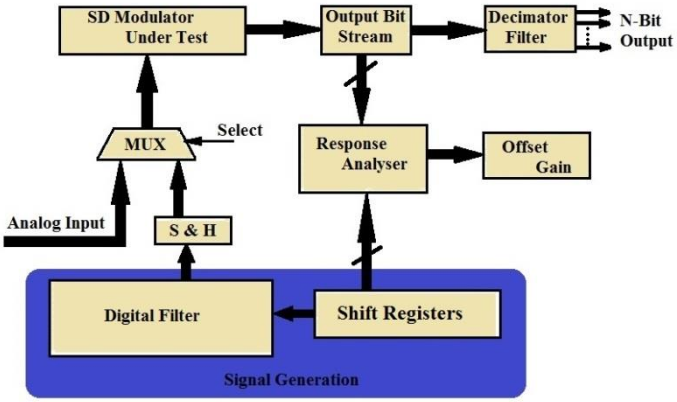

Fig 2 Block Diagram of Proposed Work

A. Test stimulus generator

Test stimulus generator consists of two blocks. Shift Registers and Digital filter.

Bitstreams are generated with the help of shift registers. These patterns are sending into digital filter and analyser. Digital filter excess these patterns and convert it into discrete analog level. One bit DAC can be used here. Digital filter works like digital to analog signal generator.

B. *Sample and hold circuit*

Maintain the desired analog input to the modulator during a required time.

C. *Mux*

Switches between controlling function during the test mode and functional configuration during usual mode. Select signal is high for test mode and low for a usual mode.

D. *Response Analyser*

Response analyser has two input digital signal. One from shift registers and the other one is from the output of sigma-delta modulator. Analyser compares these input bit by bit. A window method can be used.

E. *Window method*

In this method, a fixed analog input is applied to the modulator under test and the corresponding output level is evaluated. The principle of test consists of the comparison between the real measured and the ideally stored bit stream. The modulator response analysis is determined by a window with Test period and L length, the test procedure is represented by the figure 3. The output code does not change during T_t. T_t must be enough in order to find the initial state of the modulator after a number of L iterations. Thus, we can propose the following hypothesis: the analog magnitude

applied to the input of the device during T_t is constant since the signal dynamics is very low.

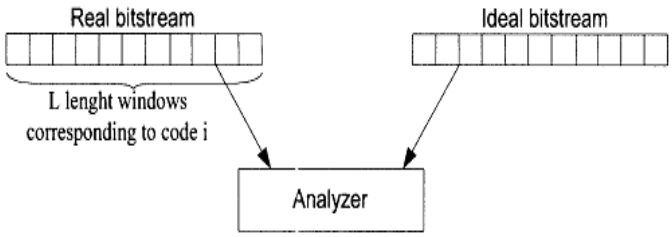

Fig. 3 the Window Method

F. Flow Diagram

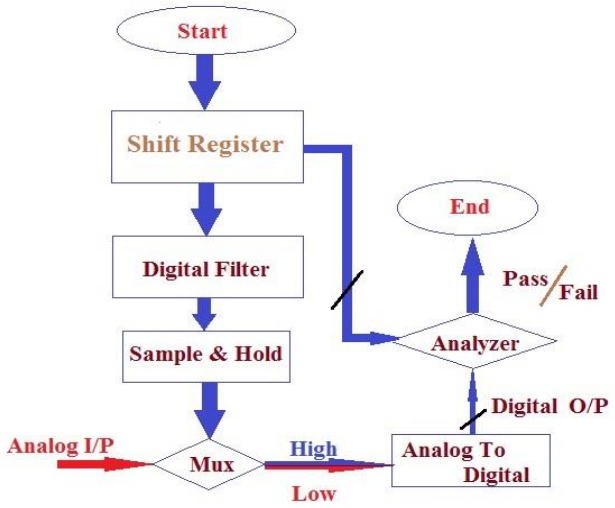

Fig. 4 Flow chart of proposed work

VI. CONCLUSION

This technique uses digital bit stream as test stimulus and a digital filter to convert bit stream into its analog value. Since the digital sequence is generated from shift register hence, pattern generator takes less area. We can measure the static characteristic (offset error and gain error) of the modulator under test with a simple response analyser by comparing the real Bit stream output with the ideal one. Conclusion is that proposed methodology is less complex and also testing time is very less. Because of these cost and power consumption would be less.

REFERENCES

[1] Johns, D. A. & Martin, K. (1997) Analog Integrated Circuit Design, John Wiley & Sons, Inc.

[2] Evan M. Hawrys hand Gordon W. Roberts. (June 1998),"An Integration of Memory Based Analog Signal Generation into Current DFT Architectures", IEEE Transactions on Instrumentation and Measurement, Vol. 47, No. 3.

[3] Dufort, B. & Roberts, G. W. (1999) "On-Chip Analog Signal Generation for Mixed-Signal Built-In Self-Test". IEEE Journal of Solid-State Circuits, 34, 318-330.

[4] Yun-Che, W. & Kuen-Jong, L. (2000) "An On-Chip ADC Test Structure. Proceedings of Design", Automation and Test in Europe.

[5] J. L. Huang, C. K. Ong, And K. T. Cheng (2000), "A BIST Scheme For On-Chip ADC And DAC Testing", Design, Automation And Testing Europe, Pp.216-220.

[6] Kuen-Jong, L., Soon-Jyh, C. & Ruei-Shiuan, T. (2003), "A Sigma-Delta Modulation Based BIST Scheme for A/D Converters", 12th Asian Test Symposium.

[7] Chee-Kian, O., Kwang-Ting, C. & Wang, L. C. (2004), "A New Sigma-Delta Modulator Architecture for Testing Using Digital Stimulus". IEEE Transactions on Circuits and Systems, 51, 206-213.

[8] Wang, Y.-S., Wang, J.-X., Lai, F.-C. & Ye, Y.-Z. (2005), "A Low-Cost BIST Scheme For ADC Testing", 6th International Conference On ASIC.

[9] Rolindez, L., Mir, S., Bounceur, A. & Carbonero, J. L. (2006) "A SNDR BIST for Sigma Delta Analogue-To-Digital Converters". Proceedings ofthe24th IEEEVLSI Test Symposium.

[10] K. Abbes, A. Hentati, M. Masmoudi (2008), "Test and Characterization Of 1bit Sigma Delta Modulator", 5th International Multi-Conference on Systems, Signals and Devices.

[11] ADC and DAC Glossary © Jul 22, 2002, Maxim Integrated Products, Inc.

[12] http://www.slideserve.com/sandra_john/delta-modulation.

[13] An Introduction to Logic Circuit Testing, Parag K. Lala, Morgan & Claypool Publishers.

[14] Nabil Chouba, Laroussi Bouzaida, "A BIST Architecture For Sigma Delta ADC Testing Based On Embedded NOEB Self-test And CORDIC Algorithm", International Conference On Design & Technology Of Integrated Systems In Nanoscale Era, 2010.

[15] Jiun-lang Huang andKwang-ting (Tim) Cheng, "Testing And Characterization Of The One-bit First-order Delta-sigma Modulator For On-chip Analog Signal Analysis", ITC International Test Conference, 2000 IEEE.

[16] IEEE_STD_1241 (2001) IEEE standard for terminology and test methods for analog-to-digital converters. IEEE Stud 1241-2000.