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A Review on Multiplier based on Reversible Logic Gate and Vedic Algorithm for Quantum Computing

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***Abstract*— A system performance is determined by the speed of the multiplier, which is the major element in the various of the application like Microprocessor, Digital signal processing, Quantum Computing etc. The Vedic algorithm improves the speed of the calculation and different types of reversible gates is used ,which ensures the zero power consumption because having ability of reversible computation that means no information loss take place , Some of the reversible logic gate from reversible logic families detect the fault in the circuit by preserving the parity at the input and output side. Reversible logic has wide application in the emerging technologies such as quantum computing, optical computing, Nano-technology etc. The different design of multiplier and techniques have evolved with the eagerness for the efficient multiplier architecture .This paper presents the comparison of the various multiplier . From the survey is finds that the reversible Vedic multiplier is the best in the terms of power ,area, delay and quantum cost .**

Keywords*— Reversible Gates; Fault Tolerant Property; Vedic Multiplier; Delay; Power ; Quantum Cost

I. INTRODUCTION

Multiplier is the most chief element in the computing systems such as Digital signal processing, Microprocessor, FIR filter etc. So the performance of these application can be improved by optimizing the various parameter of the multiplier such as power, speed, area and fault tolerance property. Since these parameter is very much important .Reversible logic circuit or information lossless circuit has zero internal power dissipation and also there are few families of reversible gate that have inherent fault tolerance property. As reversible circuit have application in variety of emerging technology such as quantum computing, nanotechnology etc. According to the Moore's law ,by the 2020 the basic memory components of a computer will the size of the individual atoms. At such scales current theory of computer will be fail and an quantum computing reinvented the theory of computer science, Quantum computer can complete task in the breathtakingly time with no internal power dissipation.

Multiplication process involves generation of partial product, addition of partial product and finally product is obtained. So the performance of the multiplier depends on the number of partial product and the speed of the adder . Vedic mathematic has 16 formula for performing arithmetic calculation. An Urdhav Tiryakbahayam formula is used for the multiplication , application for all types for multiplication . its literal means " Vertical and Cross-wise" which enhance the speed of multiplication operation. This paper deals with the survey and comparison of the various multiplier mainly in terms of the power, delay, area, quantum cost and fault tolerant property . From the survey it is find that the reversible Vedic multiplier based on the Urdhav tiryakbhayam aphorisms is offer the best results in terms of delay, area, power and quantum cost.

II. LITERATURE REVIEW

A number of research papers of various journals and conferences were studied and survey of existing literatures in is reported below:-

Panchal et al.[1] (2013) proposed an 4x4 reversible multiplier circuit which is implemented using Peres and Toffoli reversible gate and compared with the existing designs , The proposed reversible multiplier is better in terms of hardware complexity, number of gates, garbage output, constant inputs and total quantum cost.

Morankar et al. (2014) presented an reversible multiplier using Peres gate and full adder. The proposed reversible multiplier is better compared with conventional multiplier in terms of area, power and delay . Furthermore it has minimum number of garbage outputs and garbage inputs as compared to the other reversible multiplier . A new efficient multiplier is implemented and coding is done in VHDL, simulated and synthesized on Xilinx 13.1 tool.[2]

Saligram et al. (2013) proposed an high speed low power multiplier using reversible gate[3] in 2013. Here on 4x4 multiplier involves Urdhav Tiryakbhayam Vedic algorithm which makes computational speed faster and implemented .The four 2x2UT multiplier is used to obtain 4x4 multiplier using Peres gate and Feynman gate. The partial product is added with ripple carry adder which is constructed using HNG gate. The proposed multiplier design is compared with all other designs , It is find that the quantum cost of the proposed multiplier design is minimum . Quantum cost shows that the delay in the circuit.[3]

T.R et al. (2013) presented the multiplier based on Urdhav Tiryakbahayam Vedic multiplication algorithm are used .The two proposed modified multiplier design uses a reversible gate and is implemented using Peres, Feynman ,NFT,B VPPG and The partial product is added with ripple carry

adder which is constructed using HNG gate are compared in terms of the number of gates, constant inputs , garbage outputs ,quantum cost and Total Reversible Logic Implementation Cost(TRLIC).It find that the TRLIC is minimum .Since the proposed modified design has the lowest delay. [4]

Parween et al.(2014) 4x4 Vedic reversible multiplier is proposed using Peres and Feynman gate which is efficient in terms of constant inputs, garbage outputs, quantum cost, area ,speed and area .In this method ripple carry adder is used to add the partial products which is constructed using HNG gates .The design is simulated using Verilog. They had done an a comparative analysis between 4x4 Array and 4x4 Vedic multiplier using Reversible gate . Finally the author proved that Vedic Multiplier using reversible gate is the best in terms of area, speed, power and quantum cost. [5]

Krishnaveni et al. (2014) designed a 4x4 multiplier using Urdhav Tiryagabhyam sutra and also a new 4-bit adder is proposed which used in multiplier ,reduces the delay .This designed is simulated using VHDL and The comparison between the Proposed Vedic Multipler and Array Multiplier is done. It is seen that speed of the Proposed Multiplier is higher than Array Multiplier.[6]

Harish Kumar (2013)implemented and compares an architectures of multiplier they are of array and vedic multiplier. In this paper two Urdhva Triyagbhyam and Nikhilam sutras are used ,which reduces the number step for computation . While results are compared between these Vedic multiplier and array multiplier in terms of power, delay and area The coding is done using Verilog and result is simulated in Xilinx 10.1 ISE. The comparison results shows that the Urdhava Tiryakbhyam multiplier is the best multiplier as compare to Nikhilam multiplier and array multiplier.

Vengadapathiraj.et al (2015) proposed an high speed vedic multiplier using Carry look ahead adder and also a pipelined Vedic multiplier using Urdhva Tiryabhyam sutra. The coding is done in Verilog and simulation is performed using Xilinx 12.4 The comparison between proposed Vedic multiplier using CLA, Non pipelined Vedic multiplier using RCA and modified booth multiplier is done .It is find that proposed vedic multiplier using CLA based on pipelined design is faster.[9].

Jamal et al.(2013) proposed an new fault tolerant reversible gate that is LMH gate , also some of the theorems on the numbers of gates, garbage outputs and quantum cost of the fault tolerant reversible is presented which proves the optimality. The proposed 4x4 multiplier is compared with the existing fault tolerant reversible multiplier . Finally the author proved the proposed fault tolerant reversible Vedic multiplier is the best in terms of number of gates, garbage outputs, constant input and quantum cost.[11]

Somayeh et al. (2012) proposed the fault tolerant reversible multiplier circuit, which is constructed by using parity preserving gates they are modified IG gate and Fredkin gates which has the fault tolerant property , means able to detect the errors. Also the proposed fault tolerant vedic reversible 4x4 multiplier is compared with the reversible multiplier . It is finds that the proposed multiplier is fault tolerant property.[12]

Haghparast et al. (2013) presented nanometric parity preserving4x4 reversible Vedic multiplier gate . The Fault tolerant gates like double Feynman , NFT and IG gates are used .[13] . Also the Urdhav Tiryakbahayam Vedic algorithm has been used.[13]

III. RESULTS AND DICUSSIONS

The various types of multiplier are reported here . The results are survey is shown below in the Table-1. The multiplier is implemented using Fault tolerance reversible Vedic exhibits the fault tolerant property ,means able to detect error.

Paper No.	No of Gates	Constant Inputs	Garbage Outputs	Quantum Cost	TRLIC	Fault tolerant Property
First Design[4]	33	33	43	164	273	No
Second Design[4]	33	33	39	168	273	No
[3]	37	29	62	162	290	No
[2]	28	20	20	80	148	No
[1]	28	28	28	137	221	No
[5]	35	29	62	162	288	No
[11]	28	49	49	205	328	Yes
[12]	48	52	64	244	408	Yes
[13]	92	102	110	352	656	Yes

Fig 1. Comparison of different types of Reversible Multiplier and Reversible Vedic Multiplier

IV. CONCLUSION

From the survey it is found that the computation time is reduced, by minimizing the number of steps required to produce the product. and also increase the speed of the multiplier with the features of Vedic method and Reversible gates provide low power dissipation and area. The reversible Vedic multiplier is the best in terms of area, power, delay and Quantum cost. Also reported that the some reversible multiplier exhibits the property of fault tolerance.

V. REFERENCES

[1] Vijay K Panchal, Vimal H Nayak, "Analysis of multiplier Circuit using Reversible Logic" , International Journal for Innovative Research in Science & Technology, Volume 1 , Issue 6 , pp-2349-6010,Nov 2013.

[2] Prof . Amol D. Morankar, Prof Vivek M.Sakode, " Reversible Multiplier with Peres Gate and Full Adder" , International Journal of Electronics Communication and Computer Technology, Volume 4,Issue 4,pp-2249-7838, July 2014.

[3] Rakshith T.R and Rakshith Saligram, "Design of High Speed Low Power Multiplier Using Reversible logic: A Vedic Mathematical Approach" , International Conference on Circuits, Power and Computing Technologies, 2013.

[4] Rakshith T.R and Rakshith Saligram, "Optimized Reversible Vedic Multiplier For High Speed Low Power Operations", IEEE Conference on Information and Communication Technologies, 2013.

[5] A. Shifana Parween and S. Murugeswari, " A Design of High Speed, Area Efficient, Low Power Vedic Multiplier using Reversible Logic Gate" , International Journal of Emerging Technology and Advanced Engineering, Volume 4,Issue 2, February 2014.

[6] Krishnaveni D and Umarani, " VLSI Implementation of Vedic Multiplier with Reduced Delay", International Journal of Advanced Technology & Engineering Research, Volume 2,Issue 4, July 2012.

[7] Sadhu Suneel and L.M.L.Narayana Reddy, "Design of a High Speed 8x8 UT Multiplier Using Reversible Logic Gates", International Journal of Computer Science information and Engg,Volume 3, Issue4,2014.

[8] Ch. Harish Kumar , "Implementation and Analysis of Power, Area and Delay of Array, Urdhva,Nikhilam Vedic Multipliers", International Journal of Scientific and Research Publications, Volume 3, Issue 1, January 2013.

[9] Vengadapathiraj.M, ,Rajendhiran.V, Gururaj.M,Vinoth Kannan.A and Mohamed Nizar.S, " Design and FPGA Implementation of High Speed 128x 128 bits Vedic Multiplier Using Carry Look-Ahead Adder", international journal of advanced research in electronics and communication engineering ,Volume 4, Issue 2, february 2015.

[10] [10] Aneesh R and Sarin K Mohan, "Design and Analysis of High Speed,Area Optimized 32x32-Bit Multiply Accumlate Unit Based on Vedic Mathematic", International Journal of Engineering Research and Technology , Volume 3, Issue 4,April 2014.

[11] Lafifa Jamal, Md. Mushfiqur Rahman and Hafiz Md. Hasan Babu , "An Optimal Design of a Fault Tolerant Reversible Multiplier", IEEE,2013.

[12] Somayeh Babazadeh and Majid Haghparast, " Design of a Nanometric Fault Tolerant Reversible Multiplier Circuit" ,Journal of Basic and Applied Scientific Research, 2012.

[13] Majid Haghparast and Masoumeh Shams, "A Novel Nanometric Parity Preserving Reversible Vedic Multiplier", Journal of Basic and Applied Scientific Research,2013.