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A Review on Low Power Designs of Operational Transconductance Amplifier with Linearity Techniques

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***Abstract:* — In this paper the relationship among power consumption and linearity performance of CMOS OTA for RF applications are studied, that are illustrated in different literatures. Comparison among the OTA are done in terms their linearity, technology, supply voltage, power consumption, current consumption, open loop dc gain and unity gain frequency. This paper helps the future researchers to design better OTA in terms of linearity, low power consumption and high frequency of operation.**

Keywords—CMOS, IC (Integrated circuit), low power, linearity, low voltage, OTA (operational transconductance amplifier), deep submicron, RF (radio frequency).

I. INTRODUCTION (*Heading 1*)

In portable high performance, high density ICs the power consumption should be considerably minimized. This, in turn shrinks down IC both in terms of area and power supply. Hence ICs are required to be designed in deep submicron technology with low voltage and power supply. OTA are widely use in wireless analog processing applications such as continuous time OTA-C filters, four quadrant multiplier, mixer, modulator ,data converter, variable gain amplifier, oscillators and other interface circuits. In many of these applications OTA at the input stage determines the overall linearity of the system [1]. So, it is required to improve the linearity of OTAs. As device sizes, supply voltage and power consumption are scaled down to achieve higher operating-speeds, obtaining high linearity with reasonable output signal levels becomes ever challenging. Several circuit techniques have been proposed in literature to improve the linearity of MOS transconductors. These linearity techniques are discussed in section II.

II. TRANSCONDUCTANCE POWER MINIMIZATION LINEARITY ENHANCEMENT TECHNIQUES

In this section various linearity techniques are assembled at once from previously reported literatures to facilitate development of enhanced transconductors. Linearity is important constraint to make the input stage of the OTA output more reliable also the better is the linearity of transconductor the better is the reconstruction of input signal at the output. OTA generates output current for input voltage signal and act as a VCCS (voltage controlled current source) [3]. Linearity of the transconductor can be defined on the basis of linear relationship between output current and the differential input voltage. Linearity also means that the transconductance is constant for wide range of input voltage swing [3]. The techniques reported in pervious literature for low power input transconductor are: - a) Floating gate MOS differential pair [10, 12]. b) Bulk driven MOS differential pair [5, 14]. c) Pseudo differential MOS transconductor [8, 11]. To enhance linearity we can adopt: - a) Source degeneration [6, 17]. b) Bias offset technique [7]. c) Adaptive biasing [9]. d) Cross coupling [10, 18]. e) Class AB linearization technique [4, 13]. Among these mentioned technique adaptive biasing can be used for both linearity and as a low power technique.

i. DETAILS OF THE LINEARITY AND LOW POWER TECHNIQUE MENTIONED ABOVE: -

A. FLOATING GATE LOW POWER TECHNIQUE

In [10], a low voltage class-AB OTA fig 1 using the quasi floating gate MOSFET (QFG-MOS) is proposed. It is known that QFG-MOS is suitable for low voltage operation [9]. The circuit uses positive feedback to enhance the input impedance, and novel feed-forward technique to simultaneously suppress common-mode signals and enhance the differential-mode signals. The circuit exhibits large input/output swing with good linearity.

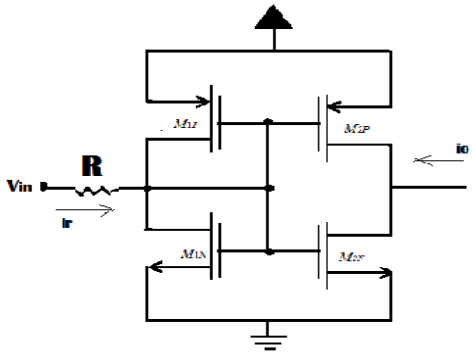

Figure 1: Single ended class AB linear OTA

The differential OTA in Fig. 2 is known as Pseudo-differential amplifier (PDA). One can see that the differential-mode transconductance (G_{dm}) is the same as the common-mode transconductance (G_{cm}), making the OTA prone to interferences and supply noises. To suppress the common-mode response, a newly developed feed-forward circuitry has been proposed. The technique employs feed-forward amplifier (FFA) and body-driven as shown in Fig. 2. As seen, FFA consists of two independent CMOS inverters ($M_{2AN,P}$ and $M_{2BN,P}$) and inverting amplifiers ($-A$), which serves two purposes: 1) to suppress the common-mode current signals (i_{o1} and i_{o2}), and 2) to enhance the differential transconductance (G_{dm}) of the system.

From Fig. 2, the differential-mode (*Gdm*) and common-mode (*Gcm*) transconductance gains can be derived and shown as

$$G_{dm} = g_{m2N,P} + A\, g_{mb2N,P}$$
$$G_{cm} = g_{m2N,P} - A g_{mb2N,P} \quad \_\_\_\_\_ (1)$$

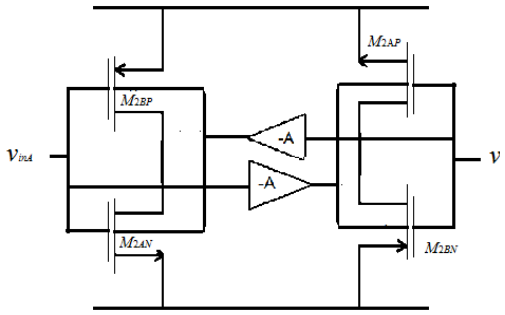

Figure 2: Proposed class-AB linear OTA

Where A is the voltage gain of the inverting amplifier, $g_{m2N,P}$ and $g_{mb2N,P}$ are the gate and the body transconductance of $M_{2AN,P}$ ($M_{2BN,P}$), respectively. The proposed QFG-inverter is employed, enabling the circuit to operate under low voltage supply. Feed-forward technique is used to suppress the common-mode response. The circuit demonstrates wide input/output swing and good linearity over an entire range of the input signal. The differential-mode gain is increased, while the common-mode gain is suppressed.

B. BULK DRIVEN LOW POWER TECHNIQUE

One major limitation of conventional OTAs is its limited linear range. As device sizes are scaling down, traditional saturation-based OTAs are facing design challenges to overcome poor linearity and limited output impedance. "Bulk driven" technique is come into practice for low threshold voltage devices for proper scaling of supply voltage that must be done to appropriately bias the device. In this method the gate-to-source voltage is set to a value sufficient to form inversion layer while the input signal is applied to bulk terminal. In gate-driven MOS transistor the gate-to-source voltage controls the drain current of the transistor while for a bulk driven MOS transistor where, threshold voltage is a function of the bulk-to-source voltage, controls the drain current. Using this technique, transistor can remain in active mode even at zero-input bias voltage and also significant improvement in input common-mode range (ICMR) can be observed. However, there are few drawbacks in bulk-driven transistors like one most important drawback is its low dc gain [5]. The current expression for well-input MOS transistor in sub-threshold mode is given by:

$$I = Ioe^{-kVgs/VT}e^{-(1-k)Vws/VT} \quad \_\_\_ (2)$$

Where *Vgs* and *Vws* is the gate-to-source and well-to source voltage, k is sub-threshold exponential coefficient (generally greater than 0.5), I_o is sub threshold exponential parameter, VT (kT/q) is thermal voltage. From (1), it can be observed that dependence of k on gate and ($1-k$) on well creates the condition that when gate is active, well remains inactive and when well is active gate is inactive.

The architecture of OTA using modified Wilson current mirror is shown in Fig. 3. The architecture works on low supply thereby introducing appreciable reduction in power consumption and increases the open loop dc gain. With the replacement of simple current mirror by modified Wilson circuit there is sufficient increase in *out r* and slight decrease in overall transconductance g_M. A bias current generator circuit is attached to OTA which generates current in the range of nano-amperes.

This paper [5] explored the approach of low-voltage OTA design using the bulk-driven technique and enhancement of gain through Wilson mirror. The design of such low voltage, high performance OTA circuit on TSMC 0.18 micron technology satisfies the required parameters for its implementation not only in power-saving devices but also in biomedical portable devices like biomedical implantable sensors, disk read channel integrated circuits (ICs), video filters, ADSL front-ends, and RF ICs. However, since several biomedical signals have frequencies much less than 609.46 KHz, so less emphasis has been made on achieving high UGB rather enhancement in DC gain has been done.

C. PSEUDO DIFFERENTIAL AMPLIFIER LOW POWER TECHNIQUE

Many approaches have been proposed to design low voltage OTA using pseudo-differential (PD) configurations. PD is based on two independent inverters without tail current source. It is known that avoiding the voltage drop across the tail current source, in a PD structure, allows wider input and output ranges, and makes the architecture attractive for low power supply applications. However, PD structure requires an extra common-mode feedback (CMFB) circuit, which serves two purposes: 1) to fix the common-mode voltage at high impedance nodes and 2) to suppress the common-mode signal components. As shown in fig.4 the pseudo differential amplifier has an internal input common mode detector (M1, M2) and a feed forward path M4 to remove DC component of the output current. The node named V_{cm} contains common mode information of the input signal. Since this Gm cell is usually used in a chain structure i.e. in Gm-C filter its

common mode extracting feature can help the previous blocks to have a better estimation of their output common voltage.

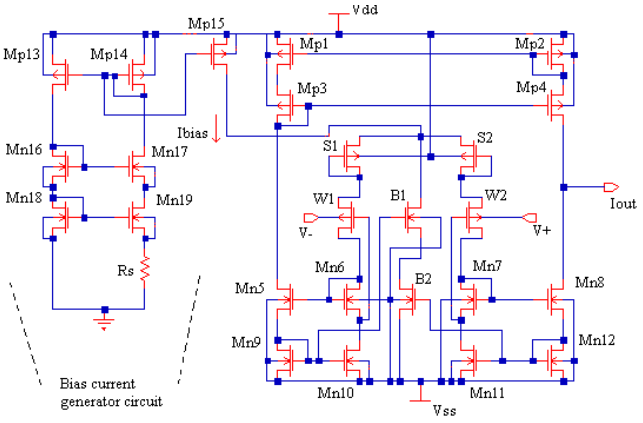

Figure 3- OTA using bulk driven and modified Wilson mirror

Considering the non-linearity of the transistor and expressing in terms of Taylor series as:

$$I=I_{dc}+a_1v_1+a_2v_2^2+\ldots\ldots \quad \text{(3)}$$

The total expression for V_{cm} can be expressed as:

$$V_{cm}=g_{m3}\ (I_1+I_2)\ =g_{m3}[2a_2(Vac)^2+\ 2a4\ \ (Vac)\ \ ^4\ +\ldots..] \quad \text{(4)}$$

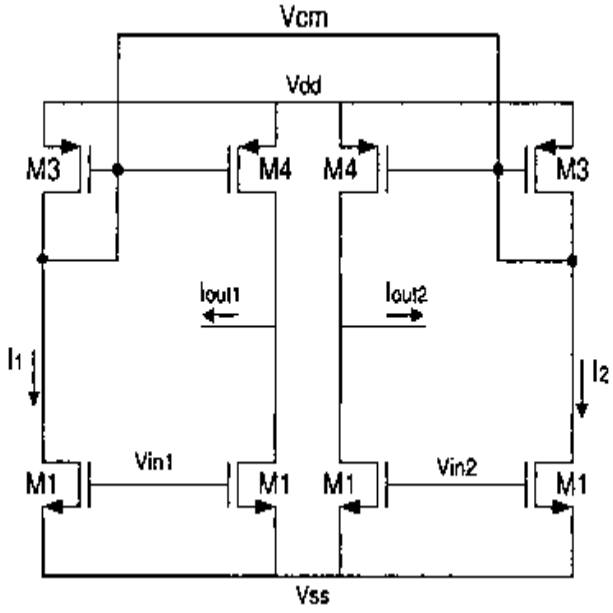

Figure 4: Basic pseudo differential amplifier structure

Equ.4 shows that with the same input g_m and the power of output current is twice in fig.5 as compared to fig.4.

D. SOURCE DEGENERATION LINEARITY TECCHNIQUE

Next technique is for linearization is based on source degeneration technique which is further used two techniques based on the use of resistors and the MOS transistors. Each one has their own advantage and disadvantage.

MOS Transconductors with Resistive Source Degeneration

In the following analysis we will consider perfectly quadratic I-V characteristics for the MOS transistors in the saturation region and the channel length modulation effect will be neglected for simplicity. Therefore, the drain current is given by

$$Id=\frac{\beta}{2}(Vgs-VT)^2 \quad \text{(5)}$$

Where β is the transconductance parameter and is the V_T threshold voltage of the MOS transistor. Using (5) the simple differential MOS transconductor shown in Fig. 4(a) has a transfer characteristic given by

$$io=\sqrt{2\beta Io}\ Vi\sqrt{1-\frac{\beta Vi^2}{8Io}}$$

Better linearity can be achieved for large effective gate-to source voltages, $V_{GS,\ off}=V_{GS}$ —V_T. For low-voltage applications this constitutes a major drawback. One of the simplest topologies to linearize the transfer characteristic of the MOS transconductor is the one with source degeneration using resistors and depicted in Fig. 6(b). The disadvantage of this configuration is the large resistor value needed to achieve a wide linear input range. Since in this case $G_m=1/R$, the obtained transconductance is restricted to small values. Moreover, this technique eliminates the electronic tuning capability of the transconductance because its value is set by the degeneration resistor.

MOS Transconductors With Source Degeneration Using MOS Transistors

By replacing the degeneration resistors with two MOS transistors operating in the triode region, the circuit in Fig. 7 is obtained. Considering perfectly matched transistors M1 –M2, M3–M4, and Neglecting

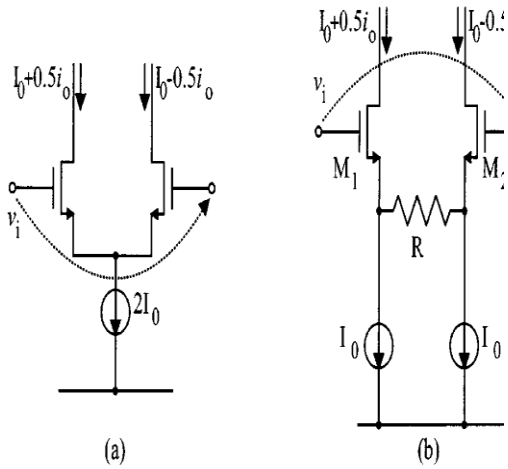

Figure (6) :-(a) Simple differential MOS transconductor. (b) MOS transconductor with resistive source degeneration.

The body and channel length modulation effects, the transfer characteristic of this transconductor is given by

$$io = \frac{\sqrt{2\beta Io}}{a}\, Vi\sqrt{1-\frac{\beta Vi^2}{a^2 Io}} \quad \text{(6)}$$

Where

$$a = 1 + \frac{\beta 1}{4\beta 3}$$

Usually, the nonlinear term under the square root can be made much smaller than unity and improved linearity and larger input dynamic range can be obtained. However, increased linearity means smaller equivalent transconductance and reduced tuning capability. The circuit has bandwidth and noise performances comparable to the simple differential pair.

When the input voltage increases beyond a certain value

$$v_i > \sqrt{\frac{4Io}{\beta 1}}\frac{a}{\sqrt{1-2a+2a^2}}$$

One of the two degeneration transistors enters in the saturation region (M4 for Vi>0, respectively M3 for Vi<0). The output differential current in this case is given by

$$Io = \left(\frac{vi\sqrt{\beta 1(4a-2)}+\sqrt{(4a-2)Io-\beta 1 vi^2}}{4a-1}\right)^2$$

When the amplitude of the input signal rises, the triode-mode degeneration MOS resistors will be more biased such that the synthesized resistance is reduced. This allows less degeneration and results in more gm of the differential pair to compensate for the drop of gm. The quantitative relationship is expressed as follows:

$G_m = [4K_{n1}\, K_{n2}\, (V_{GS1} - V_{thn})\, \sqrt{Iss}\,] / [(4K_{n3} - K_{n1})\sqrt{K}n1]$

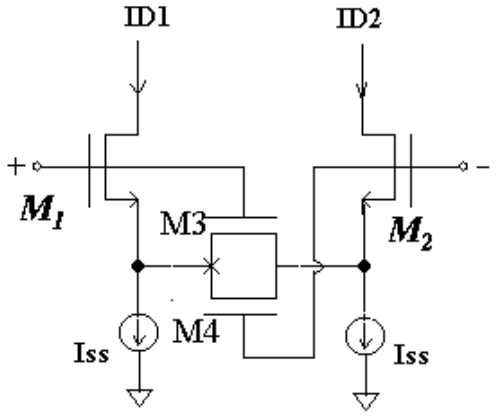

FIGURE 7: - Transconductors Using MOS Transistors Source Degeneration

E. BIAS OFFSET LINERAITY TECHNIQUE

Another linearity technique opted [WANG, 7] is the bias offset linearization technique. In this technique linearization is by cross-coupling the outputs of two offset biased and matched differential pairs as shown in Figure 8.

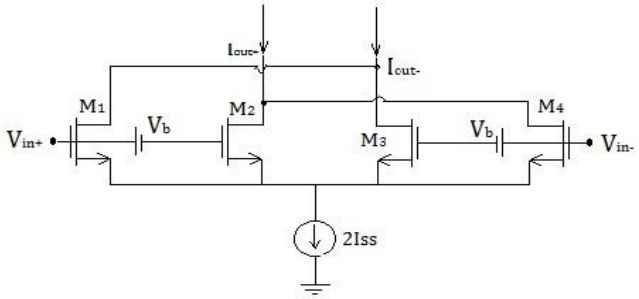

Figure 8:- MOS transconductor using bias offset technique

Assuming the drain current of an MOS transistor obeys the square law characteristics, I_D of M1-M4 are expressed as

$I_{D1} = K_N (V_{in+} - V_S - V_{THN})^2$ _____ (6.a)
$I_{D3} = K_N (V_{in-} - V_S - V_{THN})^2$ _____ (6.b)
$I_{D2} = K_N (V_{in+} - V_B - V_S - V_{THN})^2$ _____ (6.c)
$I_{D4} = K_N (V_{in-} - V_B - V_S - V_{THN})^2$ _____ (6.d)

Where V_s is negative supply and K_N is an ideal transconductance factor, V_{THN} is the threshold voltage of M1-M4, respectively. The output current I_{out} is expressed as

$$I_{out} = (I_{D1} - I_{D3}) - (I_{D2} - I_{D4}) \_\_\_\_\_ (7)$$

Assuming that the input voltage is a fully differential signal, the input voltage V_{in} is expressed as

$$V_{in} = V_{in+} - V_{in-} = 0 \_\_\_\_\_ (8)$$

From equation (2) - (4), the relation between the input voltage V_{in} and the output current I_{out} is expressed as

$$I_{out} = 2K_N V_B V_{in}$$

$$G_m = \frac{dIout}{dVin} = 2K_N V_B \_\_\_\_\_ (9)$$

From equation (5) G_m is determined by the transconductance factor K_N of M1-M4 and the bias voltage V_B. Thus the transconductance is the linear function of output current which governs the linear relationship between input voltage and output current. This is only a first order linearization as it ignores mobility degradation and other higher order effects.

F. ADAPTIVE BAISING LINEARITY TECHNIQUE

Above mentioned technique provide only first order nonlinearity cancellation, but it cannot protect the output signal from second order non linearity effects occurred due short channel length due to nano scaling of the device. Adaptive biasing technique is used for improving of the device linearity from second order by employing the MOS transistor as the square law device. Considering quadratic *i* - v characteristics for the MOS transistors and neglecting the channel length modulation effect, the simple differential MOS transconductor (shown in Figure.6) has a transfer characteristic given by

$$io_{+}=\frac{1}{2}\,\mathrm{k}\,\mathrm{v_i}\sqrt{\frac{8io}{k}-Vi^2} \quad \text{(10)}$$

Where k represents the transconductance parameter ($k = \mu CoxW/L$).

Better linearity can be achieved for large effective gate-to source voltages $V_{GSeff} = V_{GS}-V_{TH}$. For low-voltage applications this constitutes a major drawback. Furthermore, large transconductance values can be obtained only by using large bias currents and large area transistors; however this changes cause to enlarge the power consumption and active area. One of the topologies for linearization of the transfer characteristic of MOS transconductors is using the adaptive Biasing current source. The idea is using a dynamic bias current containing an input dependent quadratic component to cancel the nonlinear term in equation (6). Hence, if the bias is defined as equation (7),

$$io=\sqrt{2\mathrm{kIo}'\,\mathrm{vi}} \quad \text{(12)}$$

And put this equation in equation (6) the transfer characteristic becomes linear and could be realized according to equation (8)

$$Io=Io'+(kvi_2/8) \quad \text{(11)}$$

Fig.7 shows circuit for generating the adaptive bias current.

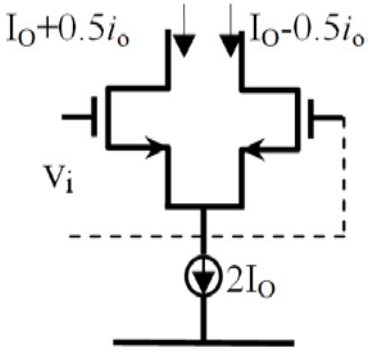

Figure 9:-Simple differential MOS transconductor

If a copy of the current of MC is mirrored into the tail current of basic differential pair the transfer characteristic becomes completely linear according to relation (9):

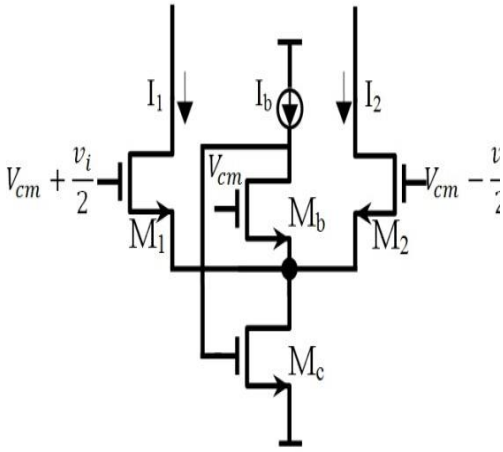

Figure 10: - Adaptive bias current generator

$$io=0.5\mathrm{kVi}\sqrt{\frac{2}{k}Ib+\frac{8}{kb}ib} \quad \text{(13)}$$

MOS transconductor that uses the linearization approach presented above. The circuit consists of 3 main blocks; an adaptive biasing current generator, a high performance current mirror and a main differential pair (fig. 9). MC1- MC4 Formed a high performance current mirror. This circuit copy the dynamic current that produced by Adaptive bias current generator circuit which formed by Ma1, Ma2, Mb and Mc into the source of the transistors of main differential pair with source degeneration transistor which formed by M1- M2.

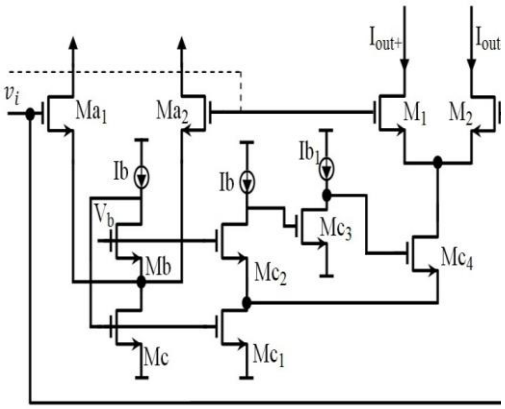

Figure 11:- The novel linear transconductor

G. CROSS COUPLING LINEARITY TECHNIQUE

The cross coupling linearization technique is proposed in [18].Cross-coupled differential pair cancellation technique to significantly minimize the third-order harmonic-distortion component. Consider a matched pair (M,, M2) coupled by two

voltage sources of equal value ($V_{th} + V_x$) as shown in Fig. 11. Representing V_1—V_2 by *v*,

$$I_D = (1/2)\,\mu_n C_{ox}\,(W/L)\,(V_{GS} + V_{TH})$$

Gives

$$I_1 = k\,(V_x + v)^2$$
$$I_2 = k\,(V_x - v)^2$$

The output current $i = I_1 - I_2$, obtained by a simple p-channel current mirror, will be

$$I = I_1 - I_2 = 4kV_x v$$

Thus this configuration exhibits a perfectly linear transconductance of value $g_m = 4kV_x$.

Consider implementing the sources ($V_{th} + V_x$) by two additional n-channel transistors M3 and IV& biased by constant currents. Note that Ml and M4 share a p-well connected to their common source node, whereas M2 and I& are in a separate well to avoid back-gate bias effects. For obtaining reasonable voltage sources with low source impedance, these devices must be wide and biased with currents that are large compared to the signal currents through them. The resulting circuit is a cross-coupled quad configuration shown in Fig. 13. M1, M2, M3, and M4 have the same channel length, but M3 and M4 are made n times wider than M1 and M2. For maintaining the same value of $V_b = \sqrt{(I/k)}$, M3 and M4 are biased with "nI".

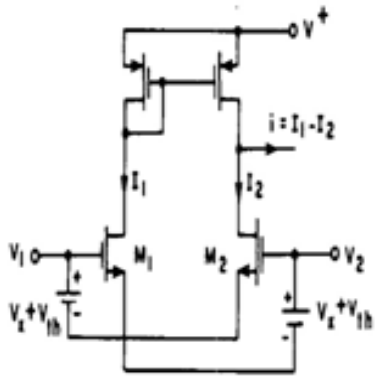

Figure 12: - Linear transconductor.

H. CLASS AB LINEARITY TECHNIQUE

When the OTA is employed with negative feedback (as an op-amp) in applications such as SC circuits or buffers for driving capacitive loads, it must exhibit a large slew-rate and sufficient gain-bandwidth product (GBW) in order to achieve a fast settling response. As it is known, Class-A circuits cannot achieve these requirements without significantly increasing their power consumption.

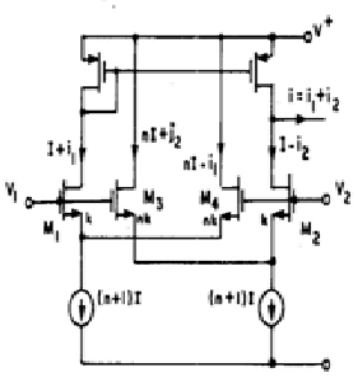

Figure13:- Linear transconductance the cross-coupled quad configuration

Class-AB OTAs have been designed using two approaches: increasing the tail current of the differential input pair for large input signals or increasing the current in the active load of the differential input pair.

The class AB V-I linearization technique can be shown in fig.14. In this topology, the transistors M3, M4,M5, M6 are biased in triode region, therefore the voltage at drain of M1, M2 would be very close to supply voltage and the source voltage can be as low as several tens mV and can here be neglected [13]. The transfer function is given by

$$I_{out} = Im_7 - Im_8 = \frac{KnKn'(Vcm - Vtn)(Vn_1 - 2Vtn)}{2Kp(Vb' - Vtp)} V_{id} \quad \text{(14)}$$

Where Kn, Kn', Kp are transconductance parameter of NMOSs (M1, M2), (M7, M8), and PMOS (M3, W4), respectively. Vtp is threshold voltage of PMOS. $V_{id} = V_{in+} - V_{in-}$, $V_b' = V_{dd} - V_b$, $V_{nl} \approx V_1 + V_2 - 2V_{s,\,M7,\,M9}$, and $V_1 - V_2 = V_{d,\,M3} - V_{d,M4}$. As can be seen from (14) that the output current I_{out} is a function of the differential input voltage V_{id}. V_1 and V_2 are very close to V_{dd}, thus $V_1 + V_2$ is almost constant and its nonlinear effect can be ignored. However, with the supply voltage lower than 2V, nonlinear term can be occurred

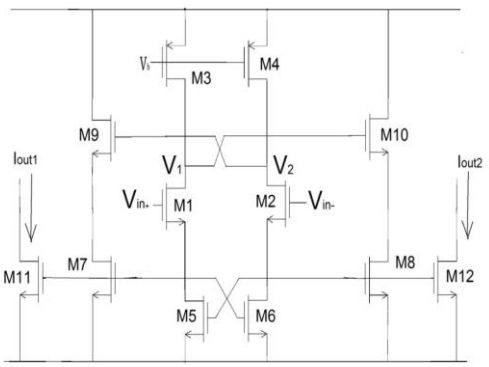

Figure 14:- Class AB Transconductor

III. CONCLUSION

There are three basic requirements of present and future techniques they are: - I) low voltage. II) High linearity. III) High frequency. (I) and (III) can be achieved optimally by downscaling of device size. As the voltage decreases the range of input voltage swing decreases or we can say that the higher voltage swing gets distorted which imposes linearity issue on the input stage of the OTA, technique for linear performance of input stage for OTA presented in paper from previous works can be used. Using of more than one linearity and power optimization technique can optimize the design suitable for any application. Each of the techniques has their own advantages and disadvantages. So the techniques should be used according to design requirement only.

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