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A Review on Low power Design Techniques for CMOS Operational Transconductance Amplifier

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***Abstract*— In VLSI design low power consumption is as important as speed in many applications since it leads to a reduction in the package cost and extended battery life. Discussion of various low power techniques like Miller compensation capacitance, Bulk Driven and DTMOS configuration is carried out in this paper. Comparison among the different OTA is done in terms of their technology, supply voltage, open loop gain, power consumption, phase margin and CMRR. This paper assists the future analysts to develop proper design of OTA in terms of stability, low power utilization and high frequency operation.**

***Keywords*—OTA (operational transconductance amplifier); Low power; Bulk driven; DTMOS; Miller compensation capacitance**

I. INTRODUCTION

Since the past decade low voltage and low power IC design have been given much attention because power consumption is an essential need in VLSI circuits. The reduction in power consumption and supply voltage helps in achieving higher operating speeds. However, reducing the supply voltage also affects various performance parameters. Therefore, new strategies are required to obtain the appropriate linearity, bandwidth and gain. The growing requirements for low power consumption as well as low power supply circuits arises the significance of operational transconductance amplifiers in analog systems [3].

CMOS Operational Transconductance Amplifier (OTA) is a fundamental building block of analog circuits and applications including consumer, industrial, and scientific portable monitoring systems such as data converters, multipliers, modulators and continuous-time filters. CMOS OTA is an amplifier that takes differential voltages as an input and produces current as an output. Section II, III and IV includes various low power strategies like miller compensation capacitance, Bulk-driven and DTMOS respectively. Finally, section V gives conclusion of the paper.

II. MILLER COMPENSATION CAPACITANCE

The basic CMOS two stage OTA is divided into four subsections of circuit: Differential gain stage, second gain stage, compensation circuitry and bias circuit.

1) Differential-transconductance stage: This stage forms the input of the op amp and sometimes provides the differential to single-ended conversion.

2) Second gain stage: If the op amp has to steer a low-resistance load, then the second stage must be implemented by a buffer stage whose aim is to reduce the output resistance and maintain a large signal swing.

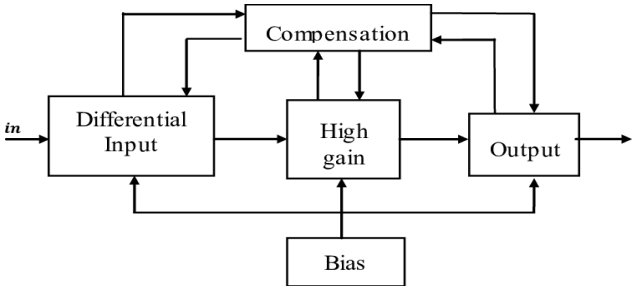

Figure 1: Block diagram of Two stage op-amp [3]

3) Bias circuits: It is used to initiate the proper operating point for each transistor in its quiescent state.

4) Compensation circuitry: This circuit is required to achieve stable closed-loop performance. The approach of compensation is to preserve stability when negative feedback is applied around the op amp.

The basic idea behind the miller compensation is to achieve proper stability of the designed system, i.e. to get a proper measure of phase margin. Now, consider an uncompensated op-amp with negative feedback and its frequency response is shown in Figure 2.

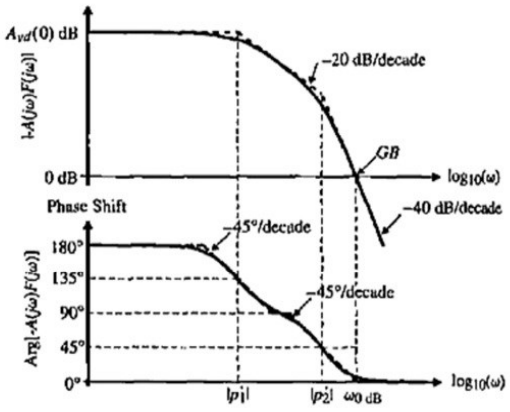

Figure 2. Open-loop frequency response of uncompensated op- amp [1]

International Journal of Engineering Research & Technology (IJERT)
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As per analog circuit designs desired range of phase margin is of at least 45˚, with 60° is preferable in most situations. Miller compensation is applied by connecting a capacitor from output to the input of differential stage (transconductance stage). The resulting small signal model is illustrated below.

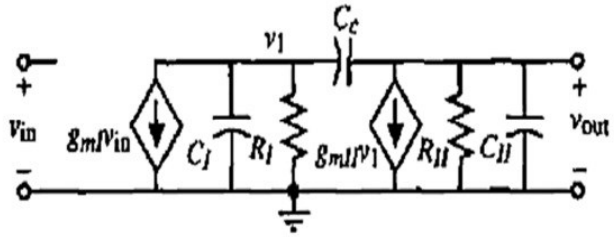

Figure 3. Small signal model of OTA with miller compensation [1]

By adding miller capacitor between the output and the input of the second transconductance stage produces two below results,

1) Pole P1 =1/R1*C1. Therefore, if C1 is increased, then P1 is decreased and P1 will move towards origin of the complex frequency plane.
2) The pole which is the new location of P2' is moved away from the origin of the complex frequency plane.

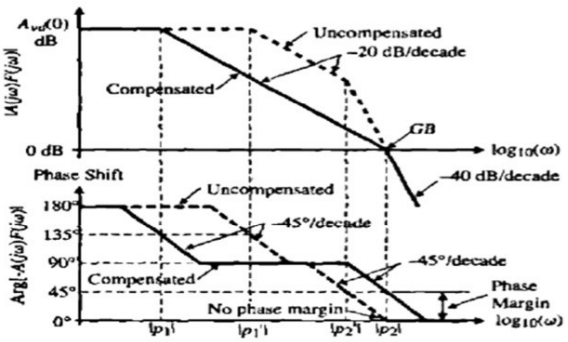

Figure 4. Magnitude and phase response before and after compensation [1]

So, the second pole will not affect the magnitude and only the first pole is dominant pole. Hence the two-stage system response will become the first stage system response. The difference between uncompensated and compensated system is shown in Figure 4.
S.M.Vishwanathan [1] proposed design and analysis of CMOS operational transconductance amplifier (OTA) under 180nm technology using LTspice software. Both the theoretical calculations and the computer aided simulation analysis meets with the given specifications**.** In this paper, high gain of 70 dB and low power dissipation of 260 µW is achieved and also the designed circuit is stable.

Along with the miller compensation technique, Rajeev and Sreenidhi Prabha [2] have introduced nulling resistor technique for two stage OTA. The OTA was simulated in the standard 180nm CMOS technology with 1.8V supply voltage. Nulling resistors are used in the series combination attached with compensation capacitance (Cc) used to move the right-hand plane zero hence it improves the phase margin of the system, which is a crucial parameter in designing the stability of complete network. Total power reduction from 834µW to 489µW is achieved using compensation capacitance technique.

For achieving minimum power dissipation design, A. Krishna P, A. R. Nair and P. R. Sreenidhi [3] have proposed an OTA design under 130nm and 180nm technology nodes operates at two different supply voltages of 1.2V and 1.8V. All the device parameters such as Gain, Phase margin, slew rate, CMRR, Gain bandwidth and Power dissipation are theoretically calculated and analyzed using LT spice software for 130nm and 180nm technology for given specifications.

S. Suman [4] has designed the OTA that exhibits a gain of 86.23 dB at 3.3V supply voltage with 350nm technology and power dissipation of 240µW.The paper shows the simulated parameters values and graphs of the all parameters.

Goswami Shikha, and Satnam Singh [5] have developed Op-amp meets nearly all parameters, including a high DC gain of 75.1dB, Unity gain bandwidth of 30.5 MHz, Phase Margin of 53.8, and CMRR of 77.7dB. Significant power savings can be accomplished, with savings of 18% and 35% for supply voltage scaling of 1.5V and 1.2V, respectively with minimal compromises in phase margin and slew rate, as well as a few other properties such as gain, UGB and CMRR.

Table 1 shows different parameters of OTA using Miller compensation technique.

TABLE 1. SUMMARY OF MILLER COMPENSATION CAPCITANCE TECHNIQUE

Ref.	Tech. (nm)	Parameters				
		V_{DD} (V)	CMRR (dB)	Phase margin	Gain (dB)	Power consu-mption
S.M Viswanathan [1]	180	0.9	-	68°	70	260 µW
A.K.P, S.P. Rajeev [2]	180	1.8	77.01	66.34°	70.6	836.44µW
A.K. P, A.R.Nair ,P.R. Sreenidhi [3]	180, 130	1.8	77.65	60°	75.6	513.02µW
S.Suman [4]	350	3.5	93	49°	86.2	240 µW
Shikha, S.Singh [5]	180	1.8	77.7	53°	75.1	536.5 µW

International Journal of Engineering Research & Technology (IJERT)
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III. BULK-DRIVEN TECHNIQUE

Bulk driven technique is same as to the gate driven technique but only difference is that ac input signal in applied to the bulk terminal for the creation of conduction between source and drain terminal shown in Figure 5.

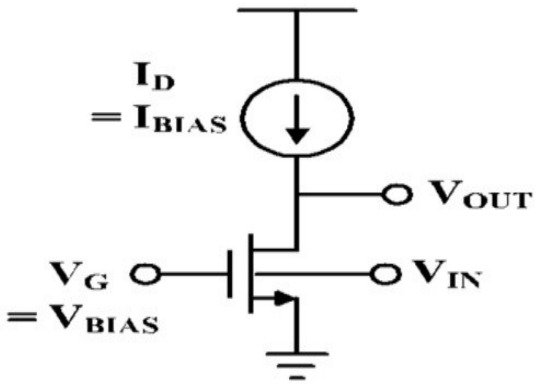


Figure 5. Bulk-driven Technique [16]

Bulk driven transistor requires the lower amount of the threshold voltage than the gate driven transistor. In bulk-driven MOSFET, by feeding AC input signal into bulk terminal to regulate the conducting channel, very small fixed bias voltage is needed that is slightly above the threshold voltage to turn ON the MOSFET. This can be proven by equation (1) where the threshold voltage is decreasing with bulk voltage.

$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{(2\phi_F + V_{SB})} - \sqrt{|2\phi_F|}\right) \quad \text{(1)}$$

Unfortunately, the bulk-driven technique also has several drawbacks. First, the bulk-driven MOSFET has lesser transconductance g_{mb} when compared to its counterpart g_{md} as shown in (2).

$$g_{mb} \cong \eta\, g_{md} \quad \text{(2)}$$

where η is between 0.2 and 0.4. gmb is transconductance of the bulk-driven transistor and gmd is trasconductance of gate driven transistor.

Also, the input bulk terminal capacitance $C_{in,bulk}$ of bulk-driven MOSFET is approximately equal to the total of bulk-to-source parasitic capacitance C_{BS} and bulk-to-substrate capacitance C_{BSUB}. This capacitance affects the transitional frequency which will determine the speed of the MOSFET. Transitional frequency is described as in (3).

$$f_T = 1/2\pi\, (g_m/C_{in,bulk}) \quad \text{(3)}$$

When given that $g_{mb} \cong \eta_{\ gmd}$, $C_{in,bulk} = \alpha\, C_{in,gate}$ the transitional frequency of bulk-driven MOSFET described as in

$$f_{TB} = \eta/\alpha\, f_T$$

where f_{TB} is transitional frequency of bulk-driven MOSFET and f_T is transitional frequency of gate-driven MOSFET.

Dipesh Panchal, Amisha Naik [6] have achieved very low power using class AB OTA with bulk driven inputs. Also, graphical method gmb/Idrain is used for designing aspect ratio of MOS transistor rather than the analytical method. The power dissipation achieved in terms of nano watt for the subthreshold operation of MOS devices with Vdd < Vth of 0.25V. However, the proposed method has limitation of gain and gain-bandwidth product.

Yongqing Wang, Qisheng Zhang, Xiao Zhao, Liyuan Dong [7] have proposed feed-forward control strategy to enhance the transconductance of bulk-driven OTAs. In this method, Robust Transconductance Enhancer (RTE) module employs a high pass filter for the feedforward path between the bulk-driven input to gate terminal. Future work may include designing of new topologies for the further reduction in power while having a high transconductance.

Arindom Chakraborty, Upal Barua Joy, Tonmoy Kumar Dey, Quazi Md Abrar Hamim, Sujan Chowdhury, Mehedi Hasan [8] have discussed and implemented a low power consuming bulk-driven design of an OTA using 90 nm CMOS technology. A high open loop gain of 57 dB was achieved by using the bulk-driven approach, which required 3.76 µW of power from a 0.5 V supply voltage. Due to the high gain from low power consumption, the proposed OTA is suitable for bio-medical applications and consumer portable electronics. However, due to low noise performance and limitations at higher frequency of bulk-driven design, further research is required to ensure the proposed OTA design can reach a more optimal performance and consume less power.

Engin afacan [9] has presented a low power and high performing bulk-driven 3 stages CMOS OTA in a 130 nm standard CMOS technology. In this paper the author has adopted a gain boosting stage by replacing the bias circuitry that consists of constant current source by resistors and that resistors in the gain boosting part have been replaced by MOSFETs acting as resistors. The design process of the proposed OTA is explained in detail and the post-layout simulations results are validated. The OTA is powered by ±0.45 V voltage source, where the power consumption is around 27 µW. The open-loop gain, unity gain frequency, and the phase margin are 73.24 dB, 5.167 MHz, and 78°, respectively.

Indu Prabha Singh, Anirudh Srivastava, Ankit Tiwari, Harsh Vardhan Garg [10] have proposed low power operational amplifier using cascoded input to get high input impedance, high bandwidth and high isolation between the input and the output stage. The proposed methodology employs the cross-coupled output stage that increases the transconductance of the output stage without occupying additional chip area. Hence, overall gain of the amplifier increased. The power consumption for the Op Amp is 19.7µw is achieved using the proposed methodology.

Table 2 shows different parameters of OTA using bulk-driven technique.

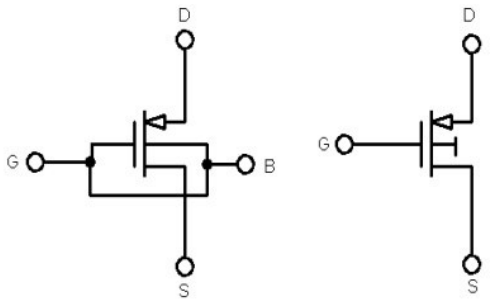
International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Volume 13, Issue 03 March 2024

TABLE 2. SUMMARY OF BULK-DRIVEN TECHNIQUE

Ref.	Tech. (nm)	Parameters				
		VDD(V)	CMRR (dB)	Phase margin	Gain (dB)	Power consu-mption
Dipesh Panchal, Amisha Naik [6]	180	0.25	-	60°	31	6.5 nW
Wang, Zhang, Zhao, Dong [7]	180	0.6	111.01	73.8°	53.81	252 nW
Chakraborty, Upal Joy, Tonmoy,Abrar Hamim, Sujan Chowdhury, Mehedi Hasan [8]	90	0.5	75.24	56°	57.85	3.76 µW
Engin afacan [9]	130	±0.45	-	78.21°	73.24	27 µW
Indu Singh, Anirudh Srivastava, Ankit Tiwari, Harsh Vardhan Garg [10]	250	1.0	39	137°	33	20 µW

IV. DTMOS (DYNAMIC THRESHOLD MOSFET) TECHNIQUE

In DTMOS technique the body and gate of the MOSFET transistor are connected to each other as shown in figure 6.



(a) (b)

Figure 6. DTMOS technique (a) equivalent circuit, (b) symbol [7]

This technique reduces the leakage current when the transistor is turned off and reduces the threshold voltage while the transistor is on to increase the overdrive voltage [2]. The DTMOS technique can offer several advantages over the bulk driven technique. The advantages of this technique are: lowering the threshold voltage, smaller circuit with fewer transistors and wide range of input voltages compared to the case where the signal is applied only to the gate terminal. Harsh Jain, Kartik Kumar, Parth Khandelwal, Raghav Agarwal, Mihika Mahendra, Trupti Taori [11] have designed DTMOS based OTA with slew rate enhancement circuit in 180nm technology. There is a significant increase of 24.58% and 20.6% in gain as compared to conventional OTA and bulk driven respectively. Moreover, there is a significant increase of 90.92% and 17.59% in gain bandwidth product as compared to conventional OTA and bulk driven respectively.

Amir Baghi Rahin, Mohammad Hosein Ghasemi, Vahid Baghi Rahin [12] have proposed a dynamic threshold MOS (DTMOS) based OTA with low supply voltage and low power consumption and simulated with TSMC 180 nm CMOS technology. The operating voltage of this circuit is 0.8 V and its DC gain is 75.31 dB. The unity gain frequency and the phase margin of this OTA are 8.40 MHz and 54° respectively. For eliminating common-mode signals the proposed OTA has a feedforward path on the first stage, and a common-mode feedback (CMFB) circuit on the second stage is provided to stabilize the common-mode output voltage.

Mihika Mahendra, Shweta Kumari and Maneesha Gupta [13] have implemented low-voltage low power two stage fully differential transconductance amplifier using 180 nm CMOS technology. In this paper, dynamic threshold voltage MOSFET (DTMOS) and unique adaptive biasing technique are used to obtain the enhanced slew-rate with minimized power supply requirement. It provides average slew-rate of 168 V/µS with 104 µW static power consumption. The dc gain of the circuit is calculated as 73.86 dB with a 72° phase margin. In adaptive biasing technique, single NMOS transistor is employed to control the tail current by using input signal itself. It enhances the tail current, which leads to achieve enhanced slew-rate.

Mesut Atasoyu [14] presented a design of a process-voltage temperature (PVT) variation tolerant inverter-based OTA employing both DTMOS technique and constant voltage biasing (CVB) scheme. The proposed OTA provides both the higher bandwidth and higher input transconductance value than a conventional inverter-based OTA design. The OTA operates in the sub-threshold region to enable low supply voltage circuit operation at the lowest 0.6V. The gain value of 50.6-dB and gain bandwidth product having value of 7 MHz is achieved.

Amitkumar S. Khade, Sandeep Musale, Ravikant Suryawanshi, Vibha Vyas [15] have focused on design of recycling folded cascode (RFC) OTA that is employed using a DTMOS based differential pair with class AB operation. Class AB operation is achieved using an adaptive biasing technique comprising a flip voltage follower which boosts the dynamic current and gain-bandwidth product of OTA. Conventional current mirrors are replaced with source degenerated current mirrors to achieve

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Volume 13, Issue 03 March 2024

high slew rate. The conventional and proposed RFC structures are designed and simulated in 180 nm CMOS process at 1 V supply voltage. However, due to the more dynamic current provided by the adaptive biasing circuit, the performance enhancement is obtained with approximately 28% extra power in comparison to the conventional RFC OTA.
Table 3 shows different parameters of OTA using DTMOS technique.

TABLE 3. SUMMARY OF DTMOS TECHNIQUE

Ref.	Tech. (nm)	Parameters				
		VDD (V)	CMRR (dB)	Phase margin	Gain (dB)	Power consumption
Harsh Jain, Kartik, Parth, Raghav, Mihika, Trupti [11]	180	±0.4	-	104°	77.69	6.5 nW
Amir Rahin, Mohammad Ghasemi, Vahid Baghi Rahin [12]	180	0.8	116.31	54°	75.31	160 µW
Mihika Mahendra, Shweta Kumari and Maneesha Gupta [13]	180	±0.5	121.87	72.16°	73.86	104 µW
Mesut Atasoyu [14]	65	0.6	-	85.7°	50.6	48.65 µW
Amitkumar S. Khade, Sandeep Musale, Ravikant Suryawanshi ,Vibha Vyas [15]	180	1.0	136.67	85.13°	67.91	20.85 µW

V. CONCLUSION

There are several low power techniques have been discussed which can be used to optimize the suitable design of CMOS OTAs. Depending upon the need of specifications of an OTA, particular topology or technique is utilized. In case if both low power and high gain is required then DTMOS technique can be adopted. If requirement is for even more low power consumption design with the compromise of gain, then bulk driven technique is suitable. Miller compensation capacitance technique is used when proper gain and phase margin is required with moderate power consumption.

VI. ACKNOWLEDGEMENT

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