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A Review of Bidirectional DC-to-DC Cuk Converter Topologies using MATLAB SIMULINK

P. Anbalagan [a,1], S. Rajalakshmi [a], Lokesh. S [b], S. Arun Prasath [b]
[a]Assistant Professor, Department of Electrical and Electronics Engineering
[a]Assistant Professor, Department of Electrical and Electronics Engineering
[b]UG Student, Department of Electrical and Electronics Engineering
University College of Engineering, BIT Campus,
Anna University, Tiruchirappalli, TN, India

***Abstract* – A Bidirectional DC-to-DC Cuk Converter is a modified cuk converter topology in which the current flows in a bidirectional way where the diodes in the conventional cuk converter topology are replaced with another switch mostly by a MOSFET switch. This topology has been designed in order to minimize the current ripple at the input end and at the output end of the converter. This converter is a combination of Boost and Buck converter topology that consisted of a series capacitor with the function as an energy storage where the output voltage (Vo) can be adjusted higher or lower than the input voltage (Vin) according to the duty cycle with reverse polarity on output side. While implementing this kind of bidirectional DC-to-DC cuk converter topologies in the real time applications like Hybrid Electric Vehicles, Energy Storage Applications and other Renewable Energy Applications, it experiences losses due to switching transitions and by means of dv/dt and di/dt losses, as a result it provides a low power conversion efficiency to the load applications with the inclusion of these losses. In order to overcome these difficulties various soft switching techniques has been implemented with the bidirectional DC-to-DC cuk converter topologies like Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS). This soft switching technique can be achieved by means of clamping action as the resonant circuits absorb almost all the parasitic reactance of switches, including transistor output capacitances which makes this converter, suitable for high-frequency operation. In this paper, the literature review of various bidirectional DC-to-DC cuk converter topologies has been made with respect to their Mode of Operation, Steady State Analysis, and a performance comparison of these converter topologies has been simulated using MATLAB SIMULINK software.**

Keywords* – *Bidirectional DC-to-DC Cuk Converter, soft switching techniques, clamping actions, high frequency applications, switching transition losses, dv/dt and di/dt losses.

I. INTRODUCTION

The DC-to-DC Cuk Converter topology is a good choice when it is necessary to control the non-isolated dc-dc converters, where the output voltage are in a large range of values. It means that the output voltage can be lower or higher than the input voltage. Especially in a high-power-factor applications, when a converter with an inductor at the front end is frequently desirable, the dc-to-dc cuk converter is useful because the output voltage level can be lower than dc input voltage. The conventional dc-to-dc cuk converter is basically a boost converter followed by a buck converter with a capacitor to couple energy. As this converter topology has low power conversion efficiency and has a higher electromagnetic interference and uncontrolled power flow due to wide input voltage variation with respect to the switching losses and dv/dt and di/dt losses, there is a need for a bidirectional dc-to-dc cuk converter to overcome these difficulties. A bidirectional dc-to-dc cuk converter topology is implemented by replacing the diodes of the conventional cuk converter topology by a MOSFET switch, which allows the current to flow in a bidirectional way as a result it minimizes the current ripple at the input end and at the output end of the converter. Different topologies has been proposed to operate bidirectional dc-to-dc cuk converters in high frequency. This paper describes about the literature review of various topologies of bidirectional dc-to-dc cuk converters starting from the conventional cuk converter topology, bidirectional dc-to-dc cuk converter topology using Lead Acid Batteries, the bidirectional quasi cuk dc-to-dc converter with reduced voltage stress on capacitor and capability of changing the output polarity, and the Zero Voltage Switching (ZVS) Active-clamping of dc-to-dc cuk converter.

II. TOPOLOGY OF CONVENTIONAL DC-TO-DC CUK CONVERTER

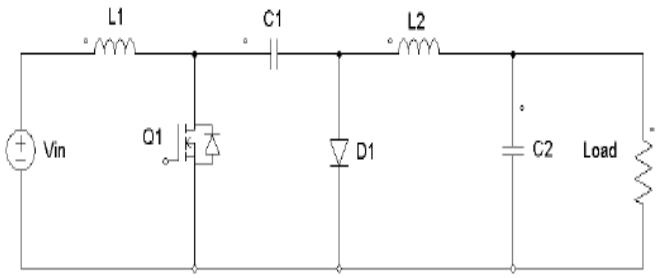

Fig. 1 Conventional DC-to-DC Cuk Converter

The fig. 1 represents the equivalent circuit diagram of the conventional dc-todc cuk converter which is essentially a modified buck-boost converter with a capacitor to couple the energy. Similar to the buck-boost converter with inverting topology the output voltage of non-isolated dc-to-dc cuk converter is typically also inverting and can be lower or higher than the input. It uses the capacitor as its main energy-storage component, unlike most other types of converters which uses an inductor. Because of the power transfer that flows

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continuously via the capacitor, this type of switcher has the minimized Electromagnetic Interference (EMI) radiation.

A) Modes of Operation :

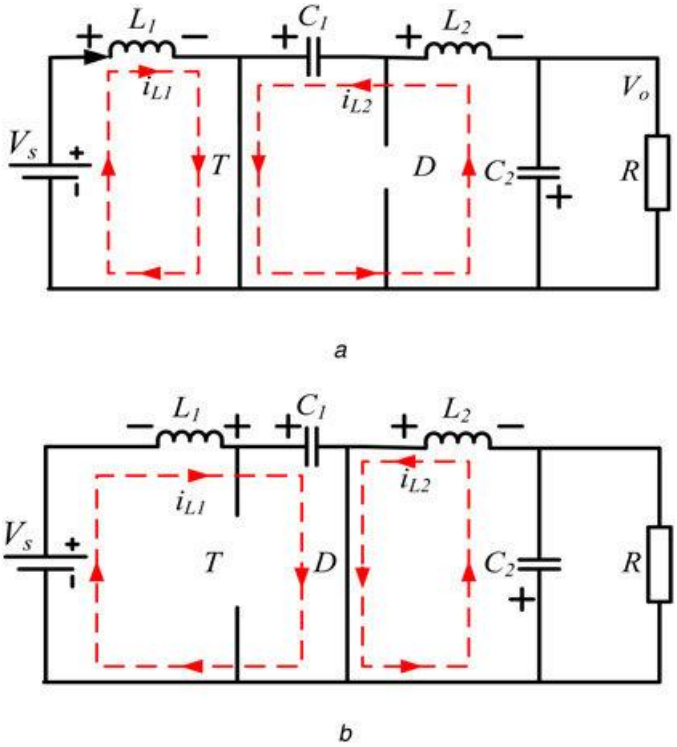

Fig. 2 Operational Modes of Conventional DC-to-DC Cuk Converter (a) Mode 1 (b) Mode 2

Fig. 2 (a) and (b) represents the various operating modes of Conventional DC-to-DC Cuk converter for the given topology.

Mode 1 (Q1 is ON and D1 is OFF): In this mode, the transistor Q1 is ON, when the gate pulse is applied at t=0. During which the inductor current (iL1) rises, at the same time , the voltage of capacitor (Vc1) reverse biases the diode D1 and turns it off. The capacitor C1 discharges its energy to the circuit formed b C1, C2, load and L2.

Mode 2 (Q1 is OFF and D1 is ON): In this mode, the transistor Q1 is OFF, when the gate pulse is removed at t=Ton, at the same time, C1 is charged from the input supply and the energy stored in the inductor L2 is transferred to load. Diode (D1) and the transistor (Q1) provides a synchronous switching action.

B) Steady State Analysis and Design Considerations :

At mode 1, assuming that the current of the inductor (iL1) rises linearly from iL11 to iL12 in time t1 where Ton ~ t1, therefore

$$t1 = (L1.del\ I1) / Vs \qquad (1)$$

and due to the charged capacitor (C1), the current of inductor (iL1) falls linearly from iL12 to iL11 in time t2 , where t2 ~ Toff, therefore

$$t2 = (L1.del\ I1) / (Vs-Vc1) \qquad (2)$$

where Vc1 is the average voltage of the capacitor C1 and

$$del\ I1 = (Vs-Vc1).t2 / L1 \quad (3)$$ therefore

$$t1 = (L2.del\ I2) / (Vc1-Vo\ ) \quad (4)$$

and the current of the inductor L2 falls linearly from iL22 to iL21 in time t2.

$$Vo= -L2(del\ I2 / t2) \qquad (5)$$

$$del\ I2 = t1(Vc1-Vo) / L2 \qquad (6)$$

where del I2 is the peak to peak ripple current flows through the load side,

average capacitor voltage (Vc1) is given by:

$$Vc1 = -Vo(1-2D) / D \qquad (7)$$

$$Vo = -D.Vs / (1-D) \qquad (8)$$

$$Is = D.Io / (1-D) \qquad (9)$$

$$del\ I1 = Vs(Vs-Vc1) / (f.L1(2Vs-Vc1)) \quad (10)$$

or

$$del\ I1 = (Vs.D) / (f.L1) \quad (11)$$

where ‘ f ’ is the switching frequency, ‘ Vs ‘ is the input DC voltage, del I1 is the peak to peak ripple current of the inductor L1, ‘ D ‘ is the duty ratio of the converter.

$$del\ I2 = Va.(Vc1-Va) / f.L2.(\ 2Va-Vc1) \quad (12)$$

or

$$del\ I2 = (\ Vs.D) / (\ f.L2) \qquad (13)$$

when transistor Q1 is OFF at mode 2, the energy transfer capacitor C1 is charged by the input current for t=t2. The average charging current for C1 is iC1 = Is and the peak to peak ripple voltage of capacitor C1 is :

$$del\ Vc1 = Is(1-D) / (f.C1) \qquad (14)$$

If we assume that the load current ripple (del Io) is negligible, then del iL2 = del iC2. Average charging current of C2, which flows for T/2 is iC2 = del I2/4. Peak to peak ripple voltage of capacitor C2 is given by:

$$del\ Vc2 = (del\ I2) / (8.f.C2) \qquad (15)\ (or)$$

$$del\ Vc2 = (D.Vs) / (8.C2.L2.f\text{^}2) \qquad (16)$$

Input current to the conventional dc-to-dc cuk converter is continuous . This circuit has low switching losses and high efficiency. When Q1 is turned ON, it has to carry the current of inductors L1 and L2. As a result, a high peak current flows through Q1. Since, the capacitor provides energy transfer, del iC1 is also high.

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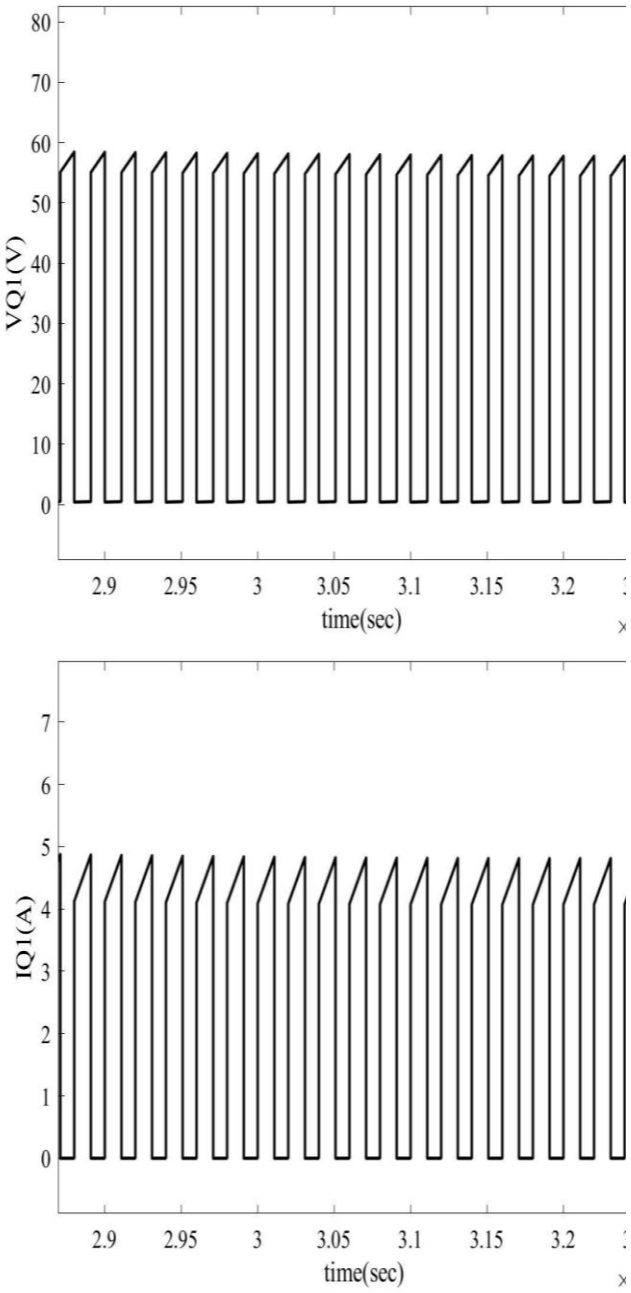
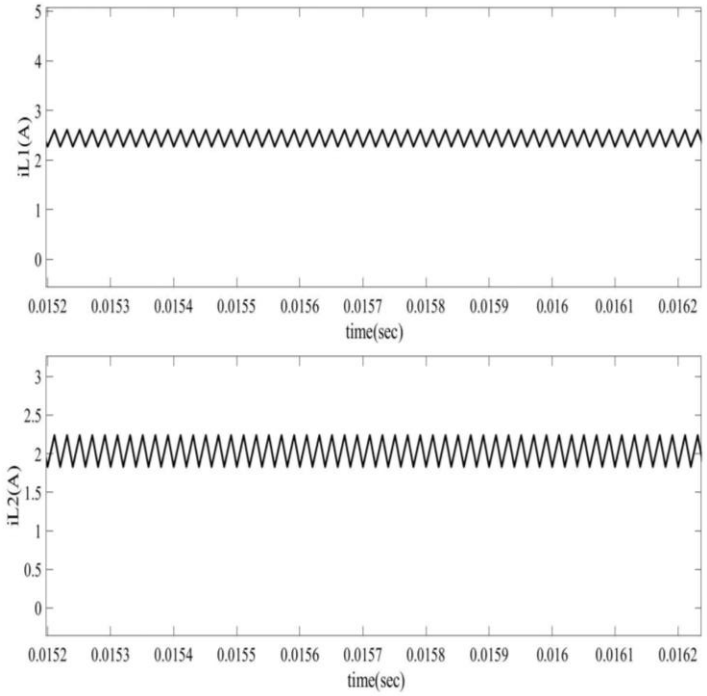
C) Simulated waveforms of Conventional DC-to-DC Cuk Converter :



(a)



(b)

Fig. 3 (a) Voltage across Q1 and Current flowing through Q1. (b) Current flowing through L1 and L2.

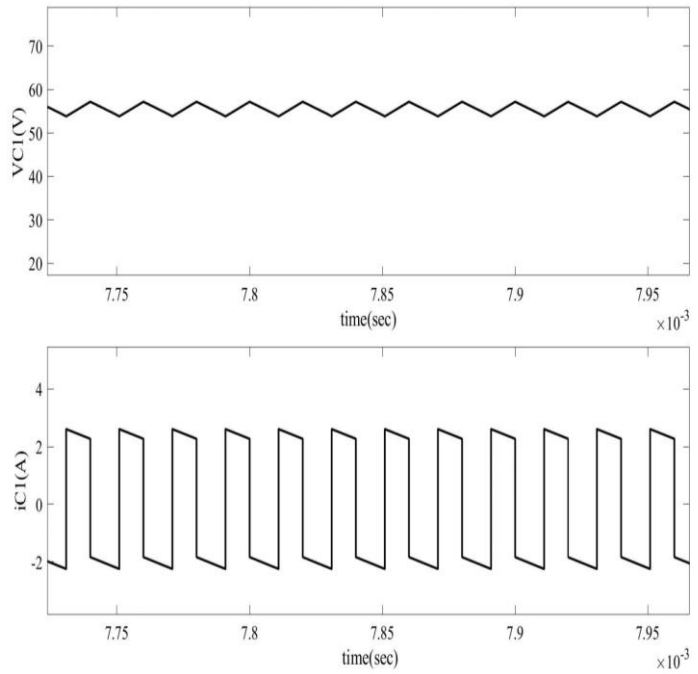


Fig. 4 Voltage across C1 and Current flowing through C1

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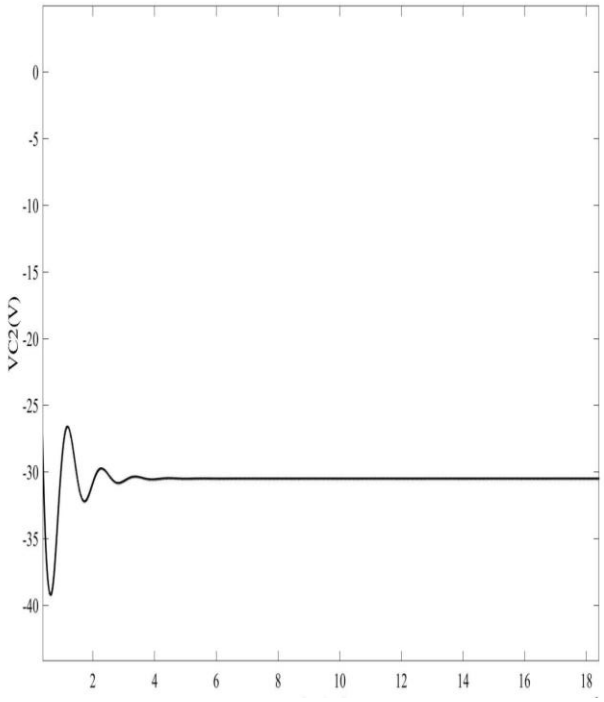
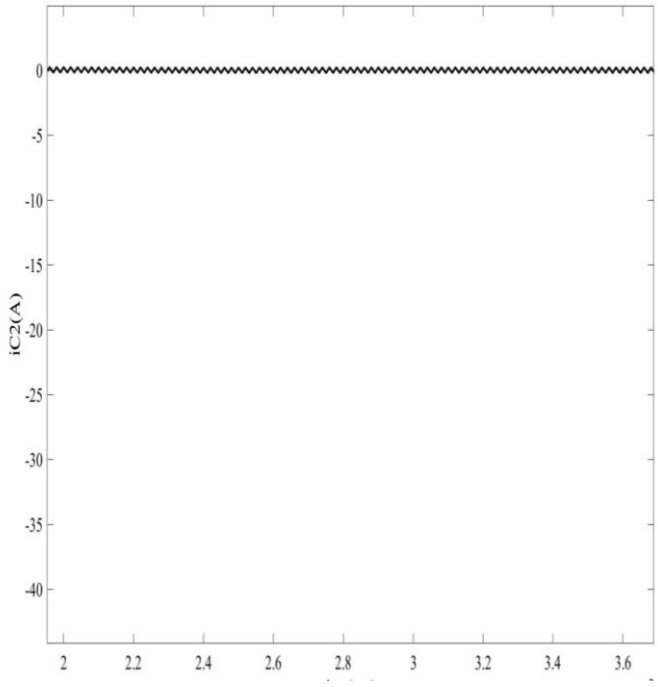


(a)



(b)

Fig. 5 (a) Voltage across C2 (b) Current flowing through C2.

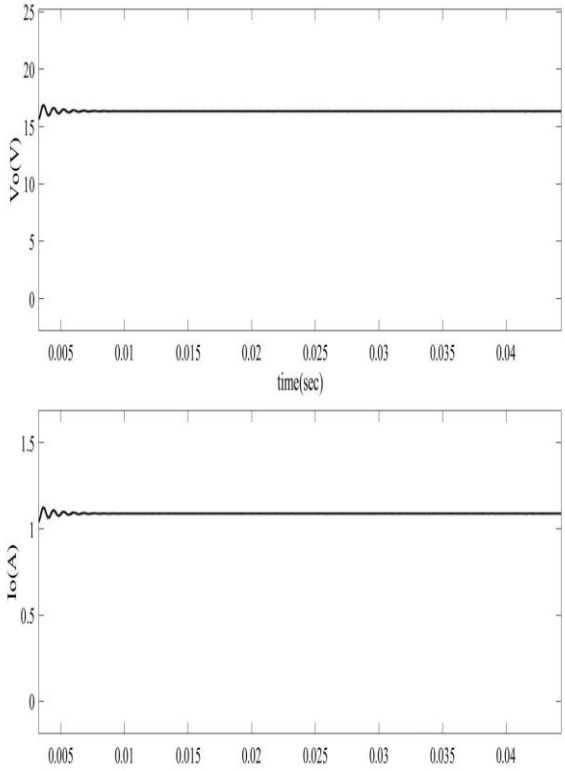


Fig. 6 Voltage across Load (R) and Current flowing through Load (R)

The above fig. 3(a) and (b) represents the Voltage and Current Waveform of the Switch S1 and Current Waveforms of both the inductors (L1) and (L2), in which when a gate pulse is applied to Switch, the inductor current rises linearly to a positive peak and linearly drops to the negative peak, due to the reverse flow of current during the Backward Conduction Period. Then the fig. 4; 5 and 6 represents the Voltage and Current waveform of the Capacitors (C1) ,(C2) and Resistive Load (R), in which the capacitors charges during the forward conduction mode and discharges during the Regeneration mode, where the Load rises parabolic to a maxima and then it gets saturated to the constant value.

D) Simulation Results of the Conventional DC-to-DC Cuk Converter :

The Conventional DC-to-DC Cuk Converter was simulated with the following specifications:

fs=50kHz; Rload=15 Ohms; Vs=25V; Vo=30V; Po=60W;

D =0.5454; L1=826.364 micro Henry; L2=681.75 micro Henry; C1 = 6.611 microfarad; C2 = 3.33 micro farad.

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III. TOPOLOGY OF BIDIRECTIONAL DC-TO-DC CUK CONVERTER USING LEAD-ACID BATTERY

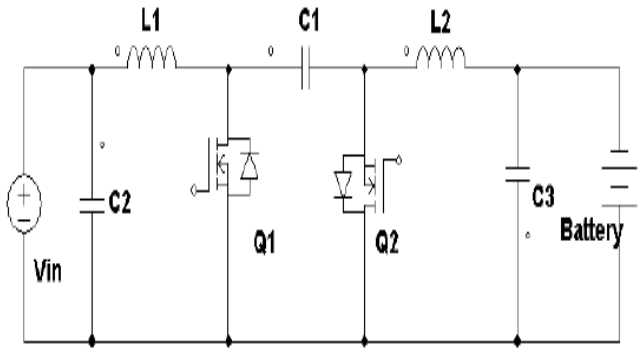

Fig. 7 Bidirectional DC-to-DC Cuk Converter

The fig. 7 represents the equivalent circuit of the proposed bidirectional dc-to-dc cuk converter. It is a modified conventional DC-to-DC cuk converter topology that can flow the current in two ways, where the diodes in the conventional cuk converter topology are replaced with MOSFET. This design has low current ripple at the input and the output, which provides an advantage that makes this design suitable for use in applications related to batteries. The basic concept of bidirectional dc-to-dc cuk converter is a combination of boost and buck topology that consists of the series capacitor with the function as an energy storage, where the output voltage can be adjusted higher or lower than the input voltage according to the duty cycle with reverse polarity on the output side.

A) Modes of Operation:

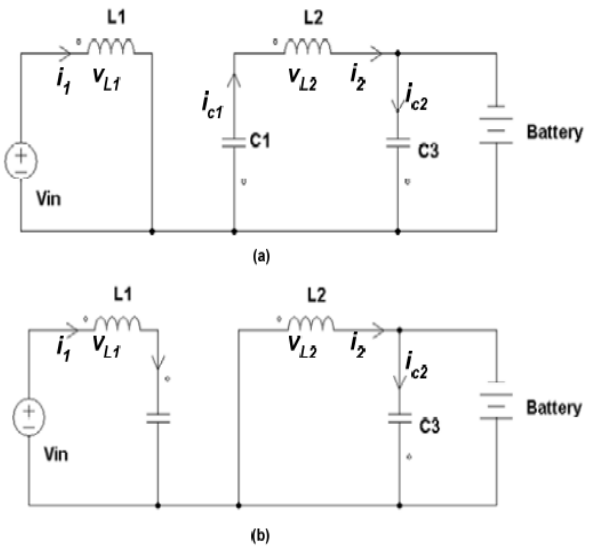

Fig. 8 Operational modes of Bidirectional DC-to-DC Cuk Converter (a) Mode 1; (b) Mode 2

Mode 1: Similar to the conventional dc-to-dc cuk converter at forward mode, MOSFET Q1 would work as a controlled switch by gate pulse generator and Q2 would go OFF, hence it will work as a regular diode.

Mode 2: On the backward mode the Q2 would be controlled by gate pulse generator and Q1 would work as a regular diode. Here is the current flow during backward and forward mode of the converter, and the steady state condition can be used to obtain the proper components of the converter.

B) Steady State Analysis and Design Considerations:

Dc-to-DC Cuk Converter is actually formed by combination of boost and buck converter, where the energy from Vin is stored through C1 before it is transferred into Vout. Therefore, the voltage of C1 is defined by:

$$Vc1 = (1/1\text{-}D).Vin \qquad (17)$$

Where ' D ' is the duty cycle of switching period to Q1. On the other hand, the output voltage, a buck converter from input of Vc1 can be determined as,

$$Vout = DVc1 \qquad (18)$$

Therefore from the equations (17) and (18), the ratio between the output voltage towards the input voltage can be calculated as ,

$$Vout = (D / 1\text{-}D).Vin \qquad (19)$$

C) Simulated waveforms of Bidirectional DC-to-DC Cuk Converter:

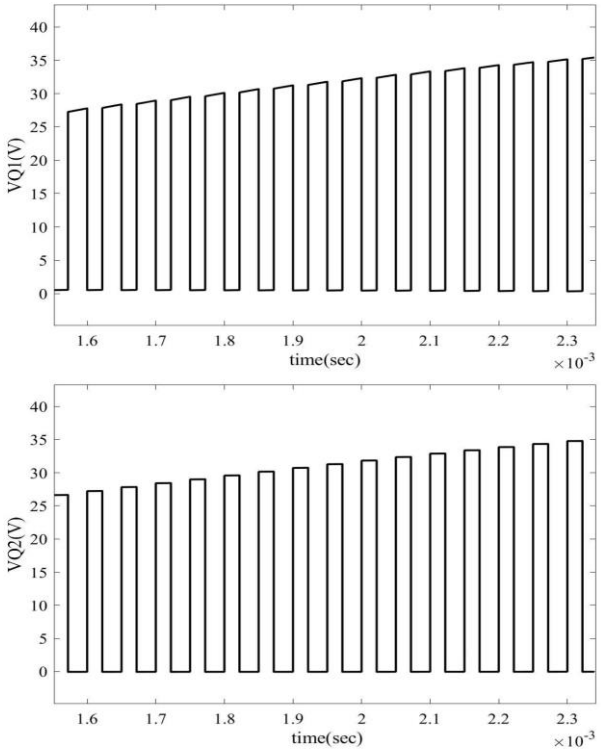

Fig. 9 Voltage across the switches Q1 and Q2

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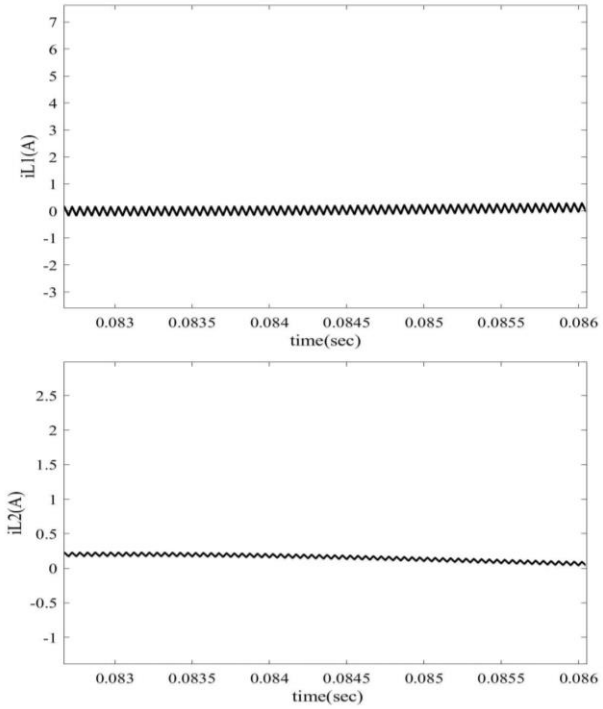

Fig. 10 Current flowing through inductors iL1 and iL2

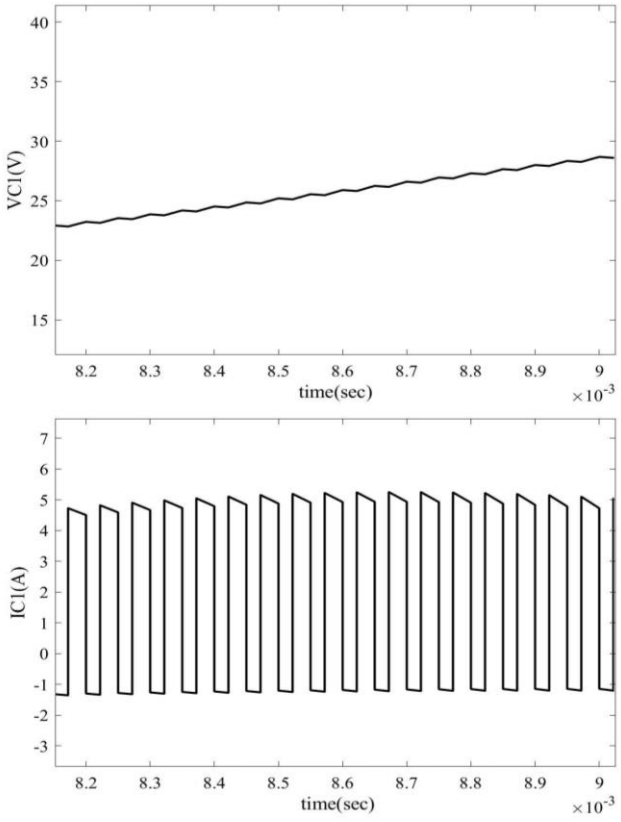

Fig. 11 Voltage across C1 and Current flowing through C1

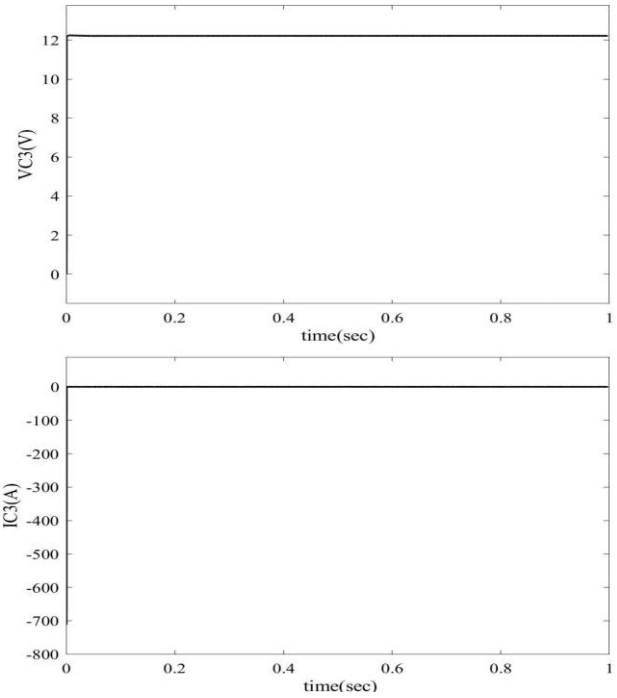

Fig. 12 Voltage across C3 and Current flowing through C3

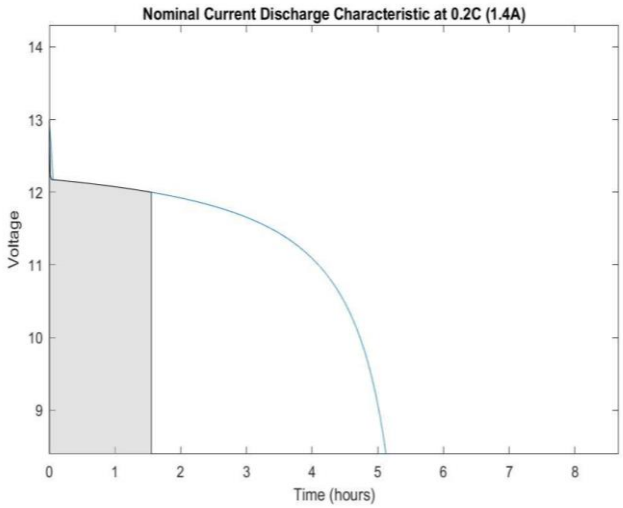

Fig. 13 Nominal Current Discharge Curve for the proposed testing of Lead-Acid Battery

D) Simulation Results of the Bidirectional DC-DC Cuk Converter:

The Bidirectional DC-DC Cuk Converter was simulated with the following specifications:

Vin=15V; fs=20kHz; Po=60W; Vout=12V; D=0.44; L1=1mH; L2=6mH; C1=330micro farad; C3= 1000 micro farad;

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The Parameters of Lead-Acid Battery as follows:

Nominal Voltage = 12V; Rating Capacity = 7, 2Ah,

Cut-off Voltage = 9.6V; Initial Voltage = 13.1V; Discharge current = 1. 25A; Final Voltage = 11.43V; initial SOC = 80-95%.

IV. TOPOLOGY OF BIDIRECTIONAL QUASI-CUK DC-TO-DC CONVERTER WITH REDUCED VOLTAGE STRESS ON CAPACITOR AND CAPABILITY OF CHANGING THE OUTPUT POLARITY

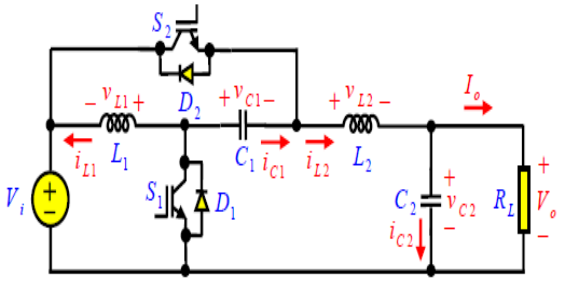

Fig. 14 ZVZCS Bidirectional Quasi-Cuk Converter

The fig. 14 shows the equivalent circuit of ZVZCS Bidirectional Quasi-Cuk Converter . According to this figure, inductors L1 and L2, capacitors C1 and C2, switch S1 with anti-parallel diode D1 and switch S2 with anti-parallel diode D2 associated with input source with voltage Vi and the output load with Resistance Rload are constituting the elements of the converter.

A) Modes of Operation:

When the Bidirectional Quasi-Cuk Converter, has four operating modes, this operation is called SD operation.For simplicity, in analysis of bidirectional quasi-cuk converter , all the elements are considered ideal.

Mode 1: In this operating mode and in the steady state, S1, S2, D2 are OFF, thus the sum of currents through L1 and L2 flows through D1. Given to the fact that in this operating mode voltage across L1 is negative and constant , therefore the current through the inductor decreases linearly from its maximum value(iLP1) and energy of that decreases. The current through the L1 and L2 are calculated from the following equations:

$$iL1 = iLP1 - (Vi/L1).t \quad (20)$$

$$iL2 = iC1 = iLP2 - (Vi/L2).t \quad (21)$$

The time interval of first operating mode (t1) can be obtained as follows:

$$t1 = (\ Le(iLP1+iLp2)) / Vi \quad (22)$$

where Le is calculated from:

$$Le=(1/L1)+(1/L2) \quad (23)$$

Mode 2: At t1 the first operating mode ends, and the second operating mode starts. Owing to the fact that sum of the inductors current is negative, thus D1 is OFF and S1 is ON, at the start of second operating mode the voltage and current of S1 is zero, thus the switching turns ON with ZVS and ZCS. The ZVZCS causes decrease in power losses. The time interval of first and second operating mode is DTs, in which one of elements S1 or D1 is ON. Zero crossing time of current through L1 in time interval DTs occurs at 1t . The maximum voltage across C1 occurs in time interval DTs at t2. In this moment, the current through it is equal to zero. t1 and t2 are calculated from equations (20) and (21) as follows:

$$t1 = (L1 / Vi).iLP1 \ , t2 = = (L2 / Vi).iLP2 \quad (24)$$

The maximum value of voltage across C2 at tP . In this moment, current through it is equal to zero. tP is obtained as follows:

$$tP = (L2(iP2-Io)) / Vi = DTs / 2 \quad (25)$$

The value of iLP2 can be calculated as follows:

$$iLP2 = Io + (D.Vi) / \ (2.L2.fs) \quad (26)$$

Mode 3: In the steady-state, S1 and S2 , and D1 are OFF, thus the sum of L1 and L2 current is negative and flows through D2 . In this operating mode, the voltage across L1 is positive and constant, therefore, current through L1 increases linearly and also energy of that increases. The currents through L1 and L2 are calculated as follows:

$$iL1 = - iC1 = iLP1 – (Vi.D.Ts) / (L1) + (Vc1 / L1).(t-D.Ts) \quad (27)$$

$$iL2 = iLP2 – (Vi.D.Ts) / (L2) + (Vc1 / L2).(t-D.Ts) \quad (28)$$

The ending moment of the third operating mode (t2) can be calculated as follows:

$$t2 = (1 + (Vi / Vc1)).D.Ts – (Le.(iLP1+iLP2)) / (Vc1). \quad (29)$$

Mode 4: At t2, the third operating mode ends and fourth operating mode starts. Due to this fact that the sum of inductors current is positive, thus, D2 is OFF and S2 is ON. At the start of the second operating mode, the voltage and current of S2 is zero, thus, this switch turns on with ZVZCS, which causes a decrease in power losses. The time interval of the third and fourth operating modes is (1−D).Ts = D′Ts, in which one of elements D2 or S2 is ON. Zero crossing time of current through L1 in time interval D′Ts occurs at t1′, which is calculated from (28) as follows:

$$t1' = ((Vi + Vc1)D.Ts-L2.iLP2) / Vc1 \quad (30)$$

B) Steady State Analysis and Design Considerations:

The maximum value of voltage across C1 occurs in time interval DT′s at t2′ . In this moment, current through it is equal to zero. t2′ is calculated from (27) as follows:

$$t2' = ((Vi + Vc1).D.Ts – L1.iLP1) / Vc1 \quad (31)$$

The minimum value of voltage across C2 occurs at tV . In this moment, the current through it is equal to zero. tV is calculated as follows:

$$tV = (\ (D+1) / 2).Ts \quad (32)$$

Owing to the fact that in the steady-state, average current through capacitors in a switching period is zero , thus by using (26) we have:

$$iLP1 = (D / 1-D\ ).Io + ((D.Vi) / (2.L1.fs)) \quad (33)$$

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Currents through L1 and L2 in terms of the output current are obtained respectively as follows:

$$iL1 = (D / 1-D).Io, \quad iL2 = Io \qquad (34)$$

The equations of Vc1 and voltage conversion ratio (Mv) are obtained respectively as follows:

$$Vc1 = (D / 1-D).Vi \qquad (35)$$

$$Mv = (Vo) / (Vi) = (1-2D) / (1-D) \qquad (36)$$

If the number of operating modes decreases from four to two, in a way that in a switching period only S1 and D2 are ON, in this case the operation of the BQ-Cuk converter is called S1D2 operation. Also, if the number of operating modes decreases from four to two in a way that in a switching period only S2 and D1 are ON, in this case the operation of the BQ-Cuk converter is called S2D1operation. The boundary conditions for changing from SD operation to S1D2 operation are as follows:

$$t1 = 0, t2 = Ts \qquad (37)$$

Using (24) and (29) and considering the condition of (37), critical inductance Le crit S1D2 is obtained as follows:

$$Le\ crit\ S1D2 = D.(1-D)^{\wedge} 2 /(-2.fs.(1-2D)).Rload\ ;\ D>0.5 \qquad (38)$$

The boundary conditions for changing from SD operation to S2D1 operation are as follows:

$$t1 = t2 = DTs \qquad (39)$$

Using (24) and (29) and considering the condition of (39), critical inductance Le crit S2D1 is obtained as follows:

$$Le\ crit\ S2D1 = D.(1-D)^{\wedge} 2 /(2.fs.(1-2D)).Rload;\ D<0.5 \qquad (40)$$

The design of the proper inductances of inductors is carried out by considering the acceptable range of the current ripple (xL%). The acceptable range of the current ripple is defined as follows:

$$xL\% = (iLP - iLV) / (iL).100 \qquad (41)$$

By using (41), the rated inductances of L1 and L2 in terms of the acceptable range of the current ripple are calculated as follows:

$$L1 = (Rload.(1-D)^{\wedge} 2) / ((1-2D).fs.xL1\%) . 100 \qquad (42)$$

$$L2 = (Rload. D(1-D)) / ((1-2D).fs.xL2\%) . 100 \qquad (43)$$

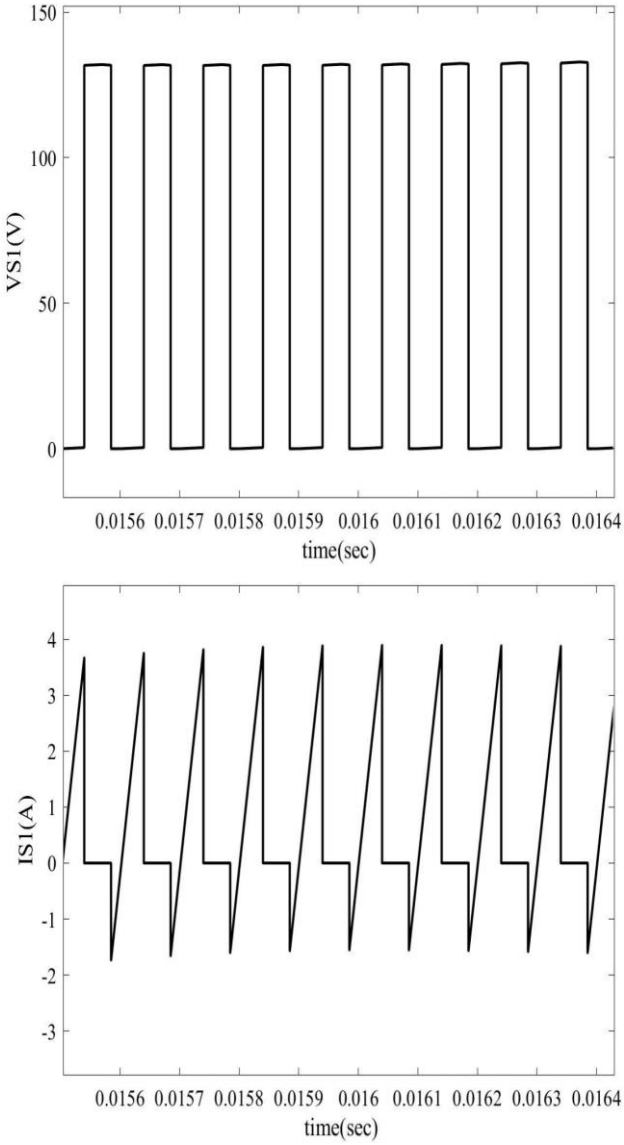
The proper design of the output capacitor, which is paralleled to the output load, is very important. The acceptable range of the voltage ripple of capacitor (xC%) is defined as follows:

$$xC\% = (Vc,max – Vc,min) / (Vc).100 \qquad (44)$$

By using (44), the capacitance of the output capacitor in terms of xC2% is calculated as follows:

$$C2 = (D.(1-D)) / (8.L2.fs^{\wedge}2(1-2D).xc2\%) .100 \qquad (45)$$

C) Simulated waveforms of ZVZCS Bidirectional Quasi-Cuk Converter:



.Fig. 15 Voltage across S1 and Current flowing through S1

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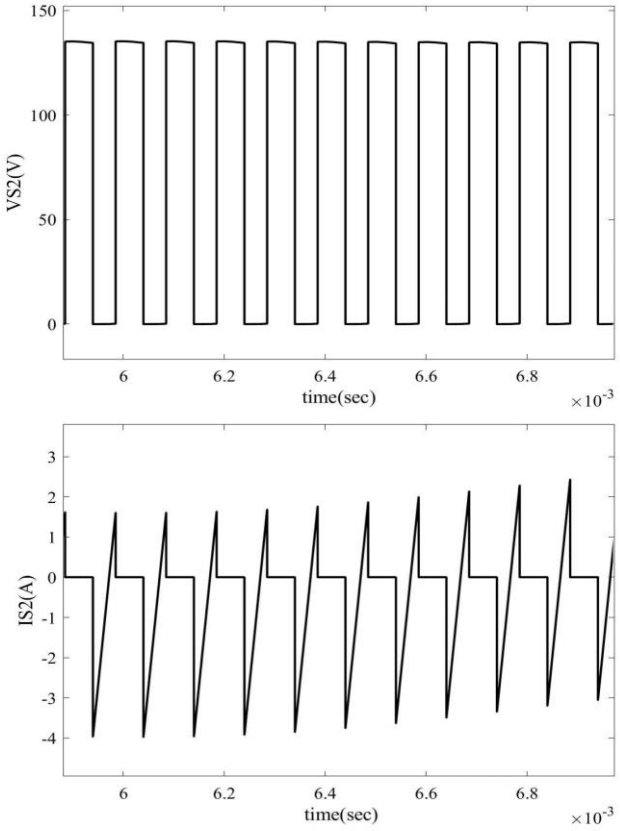

Fig. 16 Voltage across S2 and Current flowing through S2

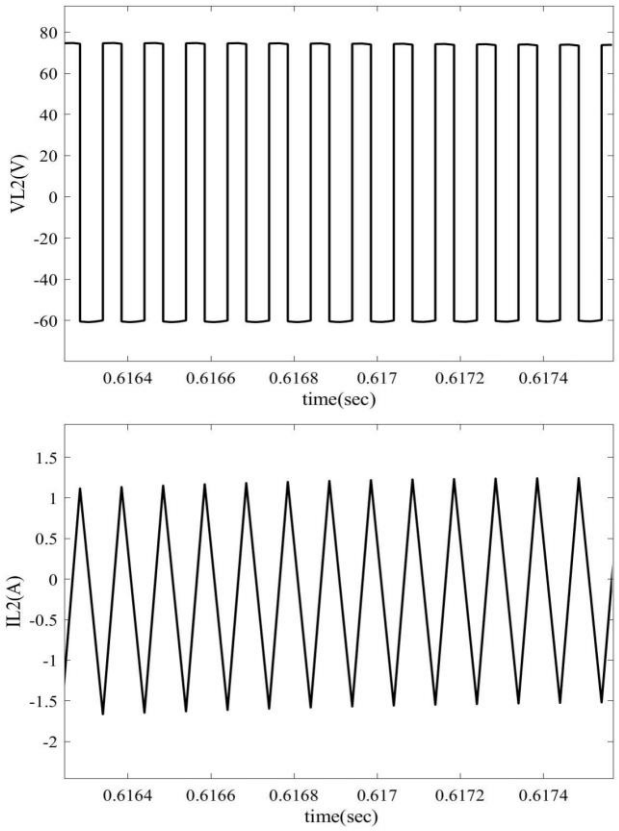

Fig. 18 Voltage across L2 and Current flowing through L2

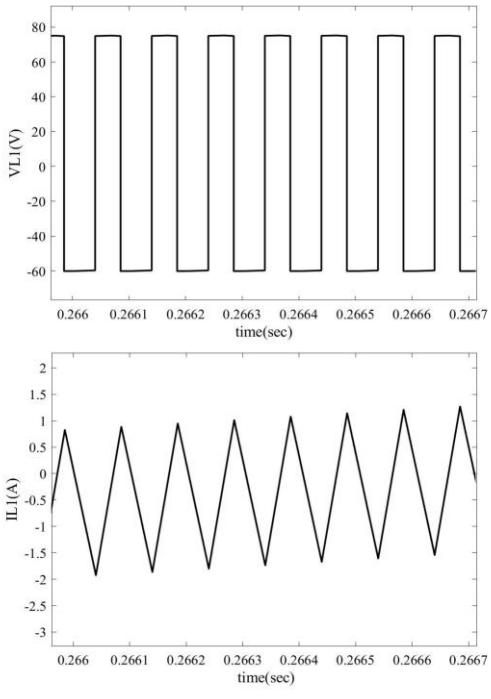

Fig. 17 Voltage across L1 and Current flowing through L1

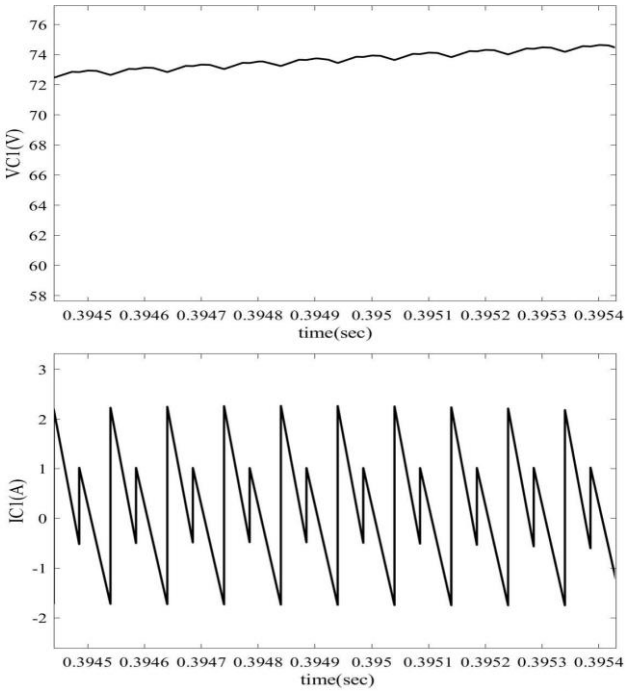

Fig. 19 Voltage across C1 and Current flowing through C1

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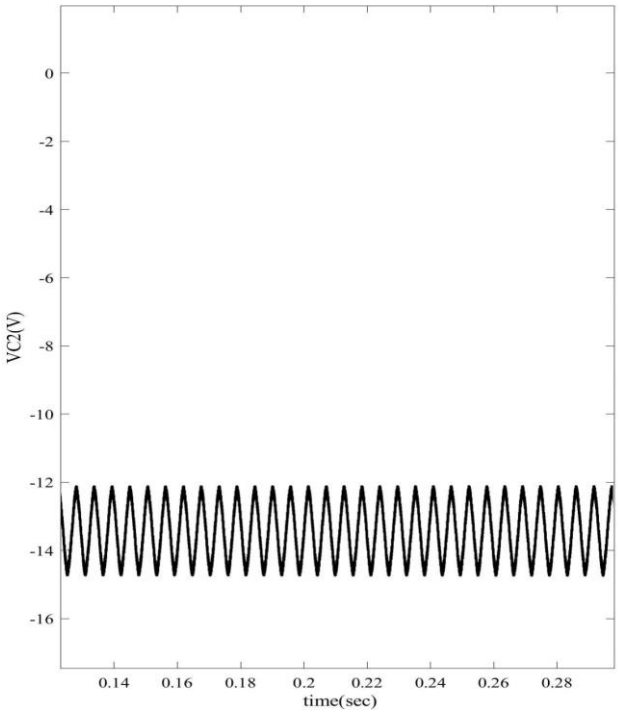

Fig. 20 Voltage across C2

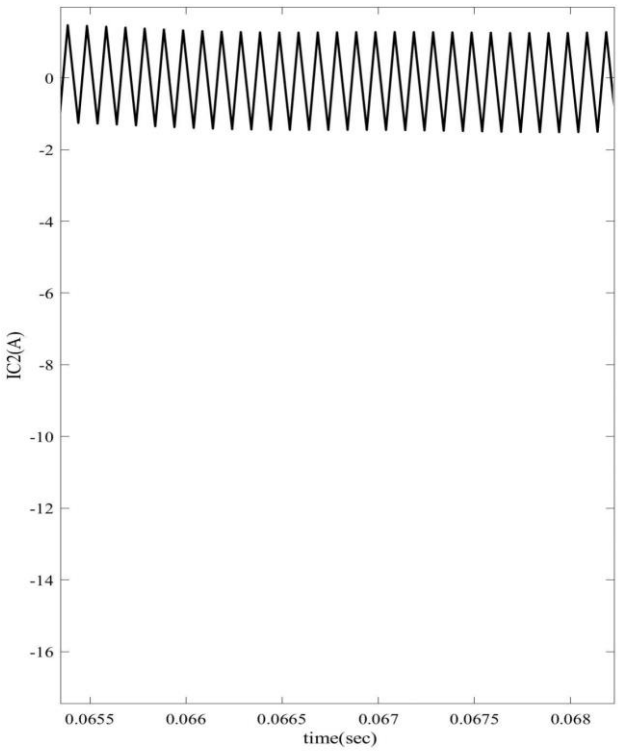

Fig. 21 Current flowing through C2

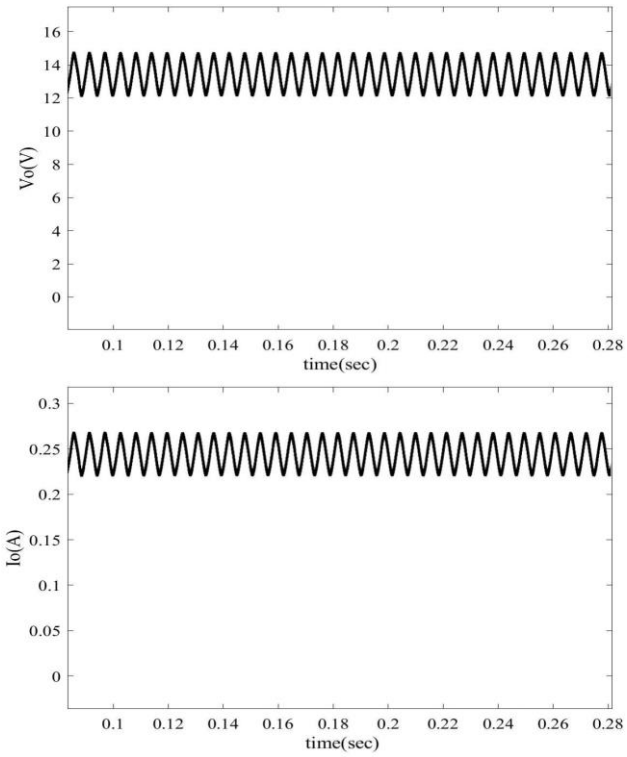

Fig. 22 Voltage across Load (Rload) and Current flowing through Load (Rload)

D) Simulation Results of ZVZCS Bidirectional Quasi-Cuk Converter:

The ZVZCS Bidirectional Quasi-Cuk Converter was simulated with the following specifications:

Vi = 60V; Rload = 55Ohms; L1 = L2 = 1.2mH; C1 = C2 = 100 micro farad; fs = 10kHz; D = 40%.

V. TOPOLOGY OF ZVS ACTIVE-CLAMPING CUK CONVERTER

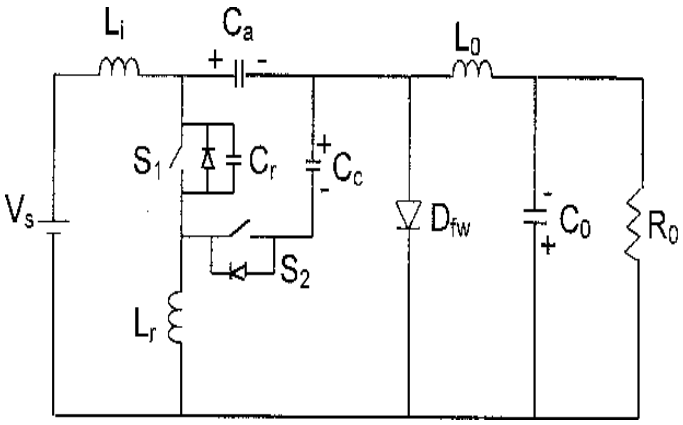

Fig. 23 ZVS Active Clamping Cuk Converter

The fig. 23 represents the equivalent circuit of ZVS Active Clamping Cuk Converter. In this converter the major parasitic reactances are absorbed, including the transistor output capacitance and track inductance, resulting in high efficiency at high frequency operation without significant increase in voltage and current stresses on switches.

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A) Modes of Operation:

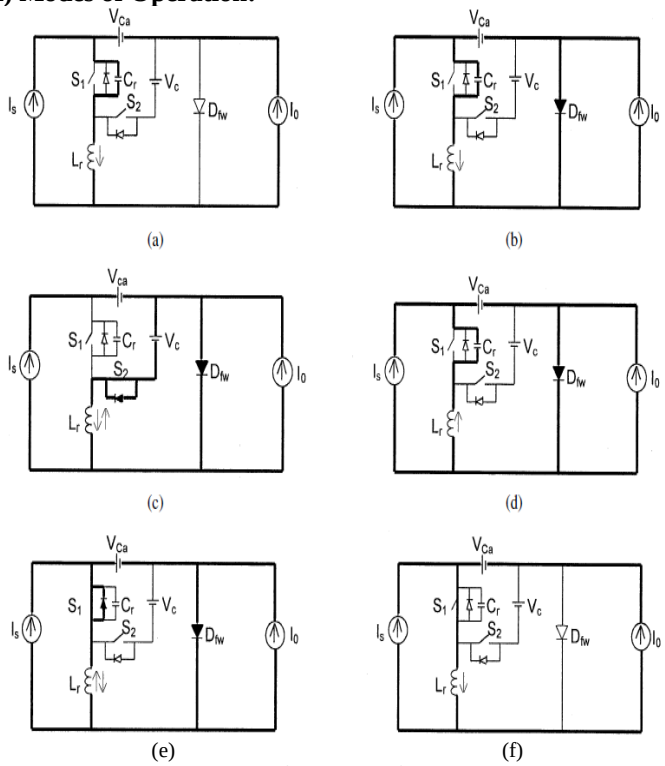

Fig. 24 Six Topological Modes of Operation of the ZVS Active Clamping Cuk Converter (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, (e) Mode 5, (f) Mode 6

The six topological modes of operation are shown in fig. 24. In this figure, it can be seen that the two switches are switched in a complementary way and soft switching is achieved for all switches.

Mode 1 (t0 <= t <= t1): Prior to t0, the main switch S1 is ON, the auxiliary switch is OFF, and the diode Dfw is OFF. When S1 is turned OFF, at t = t0, the first stage has started as shown in the fig. 24 (a). The capacitor Cr is charged under constant current. When vCr(t) reaches VCa = Vo+Vs, the output diode (Dfw) becomes forward biased and starts conducting.

Mode 2 (t1 <= t <= t2): In this mode, current through Lr and voltage across Cr rings in a resonant way. Voltage vCr(t) increases until it reaches (Vo+Vs+Vc). When vCr(t) = (Vs+Vo+Vc), the anti-parallel diode of S2 starts conducting and this stage ends.

Mode 3 (t2 <= t <= t3): At this mode, Lr current ramps down, because Cc is considered as a constant voltage source, until it reaches zero, when it changes its direction and rises again. In this stage, voltage across Cr is clamped at (Vs+Vo+Vc). When the anti-parallel diode of S2 is conducting, the auxiliary switch S2 should be switched ON to achieve a lossless turn-on. This stage ends when S2 is turned OFF t = t4.

Mode 4 (t3 <= t <= t4): At this mode the, the voltage across Cr falls, due to resonance between Lr and Cr, until reaches zero at t = t4. This stage ends when vCr(t) becomes null and the anti-parallel diode of S1 begins conducting.

Mode 5 (t4 <= t <= t5): In this mode, S1 is turned ON without switching losses, in a ZVS technique, because vCr(t) became zero. The current through Lr changes its polarity and ramps up to reach Is at t = t5. Then, the diode Dfw becomes reverse biased and turns OFF.

Mode 6 (t5 <= t <= t6): At this mode, S1 is conducting a current equal to (Is+Io) and the auxiliary switch is OFF. The diode Dfw is OFF and the stage ends when S1 is turned OFF at the end of the period.

B) Steady State Analysis and Design Considerations:

In order to obtain the low frequency behavior some simplifications are necessary, because otherwise, it could be an impossible or extremely hard task. Therefore, as the resonant time intervals are so small when compared to the duration of modes 3,5 and 6, it is possible to obtain the dc voltage gain from this simplified analysis. Therefore, to proceed with this approach the following considerations are to be made:

i) All switches are ideal and are switched in a complementary way, without dead time.

ii) The capacitances Ca and Cc are represented by the dc voltage sources.

iii) The input voltage source and Li, and the output capacitor and Lo are considered as current sources.

As Is must be equal to the average current through Lr(ILr) is given by:

$$q = Is / Io = Vo / Vs = (D-Delta) / (1-D+Delta) \quad (46)$$

where q represents the dc voltage gain of the converter. If we consider,

$$Ln = (Lr.Io) / (Vs.Ts) \quad (47)$$

It will result that,

$$Delta = 2.Ln \quad (48)$$

Substituting (48) in (46) we get,

$$q = (D-2.Ln) / (1-D+2.Ln) \quad (49)$$

The average voltage across the capacitor (Vc) is given by:

$$Vc = (Is+Io) . ((2.Lr) / ((1-D).Ts)) \quad (50)$$

(Or)

$$Beta = ((2.Ln) / (1-D)).(1+q) \quad (51)$$

Where,

$$Beta = Vc / Vs \quad (52)$$

Thus equating (49) in (51), it results that:

$$Beta = ((2.Ln) / (1-D)).(1 / (1-D+2.Ln)) \quad (53)$$

Where (Beta) is the normalized clamping voltage.

Due to the capacitance Cr, S1 and S2 are turned OFF with no losses, in a ZVS technique. However, S1 and S2 will turn ON with no losses, only if there were enough energy stored in Lr to achieve soft commutation. At t = t1, it is necessary to charge Cr from Vo+Vs to Vo+Vs+Vc. At t = t3, it is necessary to discharge Cr from Vc+Vs+Vo to zero. The latter is more difficult because it needs more energy. Thus, if enough energy is guaranteed to achieve soft commutation for S1, then S2 will

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also achieve soft commutation. Therefore, from energy relationships in Lr and Cr, at t = t3,we have:

$$Ln >= [(1-D) / ((1-D)T.wo-2)] \quad (54)$$

Where,

$$T = fs / fo \text{ and } wo = (1 / sqrt(Lr.Cr)) \quad (55)$$

And fs represents the switching frequency and fo represents the resonant frequency of Lr and Cr.

As that result was achieved on a model with imposed current, then, at t = t3, the current through Lr is equal to the average current. However in real prototype, there is an input inductor that has a maximum current greater than the average current, o there is more energy stored to commutation. Thus (54) must have a correction factor, which is represented by:

$$Ln >= [(2Ln) / (1-D)+1].[1 / ((D-2Ln).r/2+1)].(1/T.wo) \quad (56)$$

Where (r) is the percentage input current ripple,

$$r = (delta\ Is) / (Is) \quad (57)$$

From the preceding analysis, it is clear that soft commutation, when S1 turns ON, will be achieved depending on Io and Lr, and as Io on the processed power, then that commutation will occur with no losses, only in a range of load that will be established through (56). However, although commutation is not completely without losses, the converter will still operate with high efficiency I light-load situations, because there will always be enough energy stored in Lr to help the commutation process, and the lost energy will never be so high, as I a completely hard switching commutation.

As the critical commutation is when S1 turns ON, it is important to determine the time interval between the turning ON of S1 and turning OFF of S2. This time interval is necessary for existence of soft commutation. Then,

$$td >= (Vc+Vo).Cr / Is \quad (58)$$

$$td <= ((Vc+Vo).Cr / Is) + (Is.Lr) / (Vo+Vs) \quad (59)$$

The voltage and current stresses are represented below in such a way that all current and voltages are normalized, which means,

$$I\ vector = I / Io \text{ and } V\ vector = V / Vs \quad (60)$$

For switch S1,

$$V\ vector\ S1pk = 1 / (1-D) \quad (61)$$

$$I\ vector\ S1\ pk = 1 / (1-D+2Ln) \quad (62)$$

$$I\ vector\ S1\ avg = (D-2Ln) / [1-(D-2Ln)] \quad (63)$$

$$I\ vector\ S1\ rms = 1 / [Ln-(D-2Ln)].sqrt((3D-4Ln) / 3). \quad (64)$$

For switch S2,

$$V\ vector\ S2pk = 1 / (1-D) \quad (65)$$

$$I\ vector\ S2\ pk = 1 / (1-D+2Ln) \quad (66)$$

$$I\ vector\ S2\ avg = 0 \quad (67)$$

$$I\ vector\ S2\ rms = 1 / [1-(D-2Ln)].sqrt((4(1-D)+16Ln) / 3) \quad (68)$$

For Diode Dfw,

$$V\ vector\ Dfw\ pk = 1 / ((1-D)+ 2Ln) \quad (69)$$

$$I\ vector\ Dfw\ pk = 2 / ((1-D)+ 2Ln) \quad (70)$$

$$I\ vector\ Dfw\ avg = 1 \quad (71)$$

$$I\ vector\ Dfw\ rms = sqrt((4(1-D)+8Ln) / (3(1-D+2Ln)^{\wedge} 2)) \quad (72)$$

C) Simulated waveforms of ZVS Active Clamping Cuk Converter:

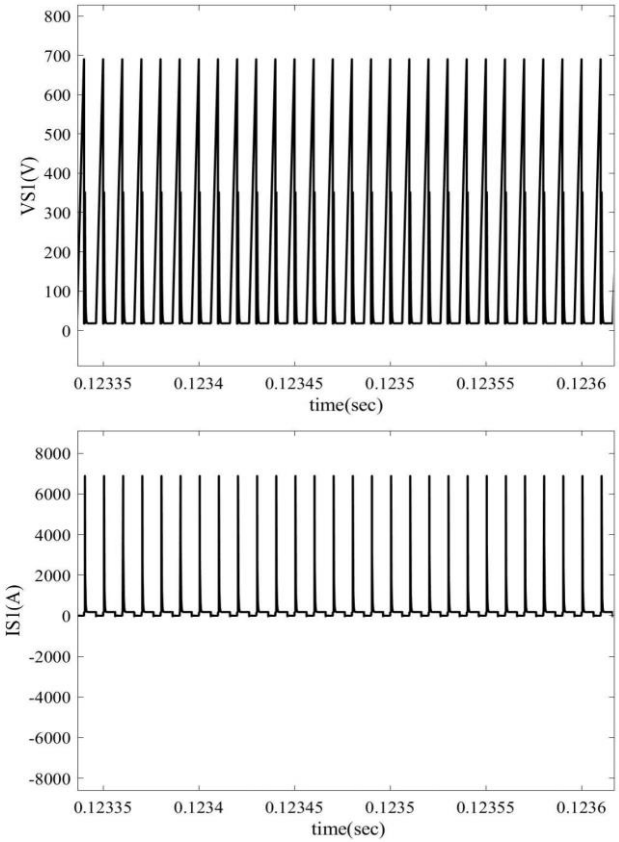

Fig. 25 Voltage across S1 and Current flowing through S1

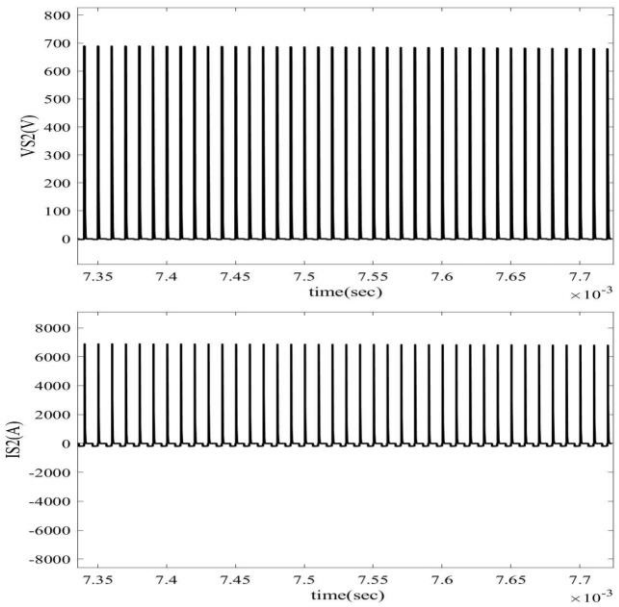

Fig. 26 Voltage across S2 and Current flowing through S2

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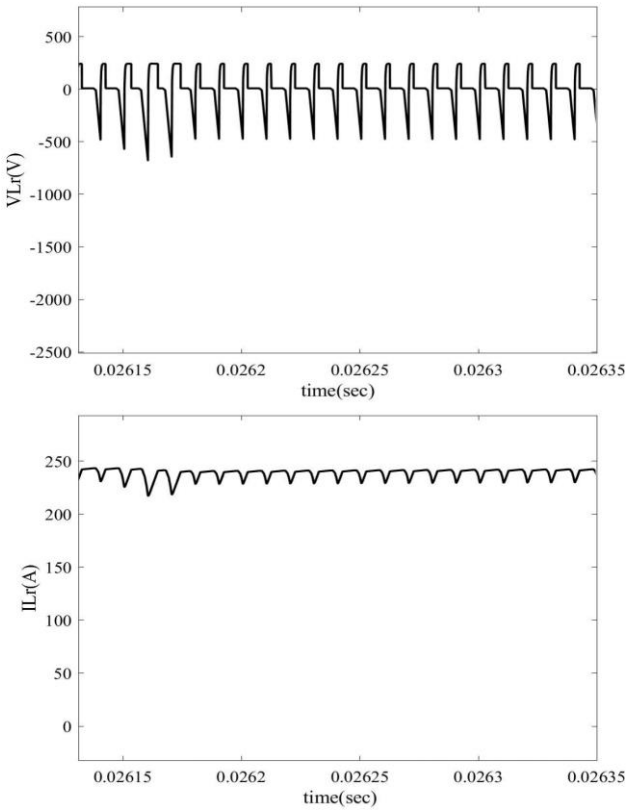

Fig. 27 Voltage across Lr and Current flowing through Lr

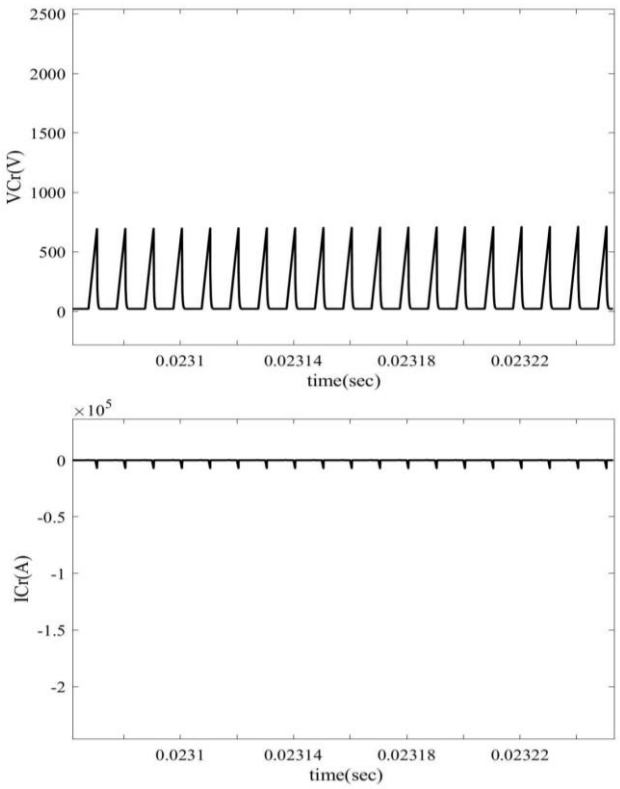

Fig. 28 Voltage across Cr and Current flowing through Cr

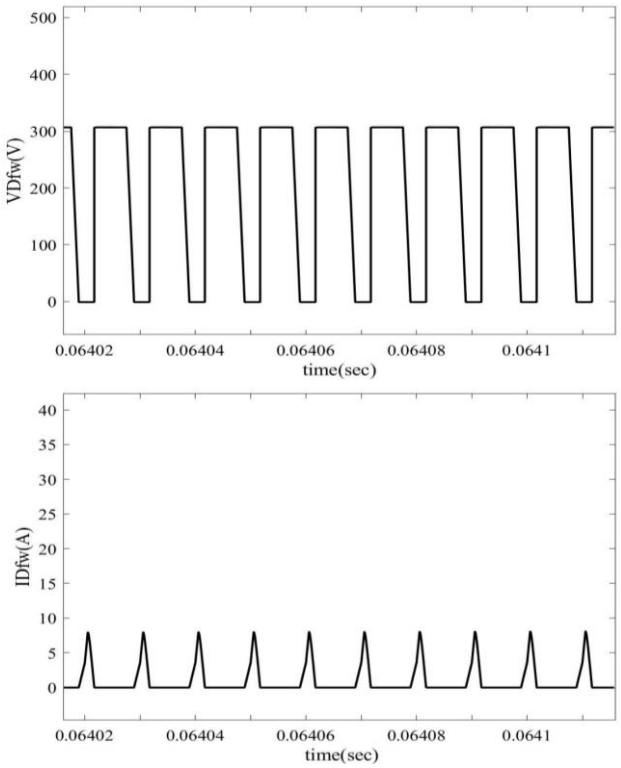

Fig.29 Voltage across Dfw and Current flowing through Dfw

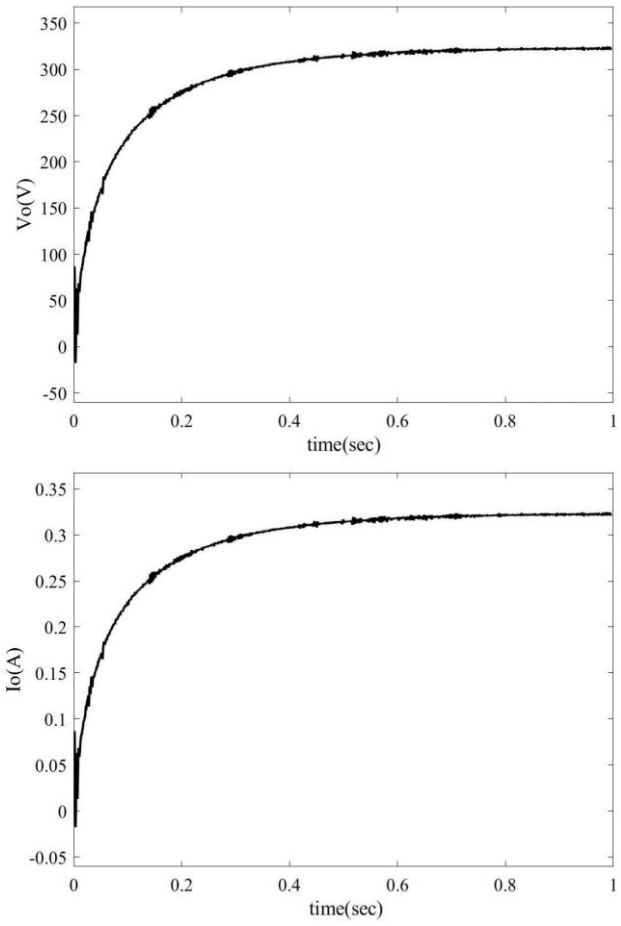

Fig. 30 Voltage across Load (Rload) and Current flowing through Load (Rload)

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Fig. 25 and 26 represents the Voltage and Current waveforms of the two anti-parallel switches S1 and S2, of which a gate pulse has been applied by pulse generator kept at 63% of duty cycle , in order to minimize the switching losses, the ZVS turn ON has to be observed with respect to the obtained voltage and current waveform of the resonant inductor Lr as shown in fig. 27, where it turns ON the switch during the Zero voltage switching period of the duty cycle. The fig. 28; 29 and 30 represents the voltage and current waveform of the resonant capacitor and the Resistive load that shows the behavior the buck-boost converter topology with minimized switching losses and dv / dt; di / dt losses.

D) Simulation Results of ZVS Active Clamping Cuk Converter:

The ZVS Active Clamping Cuk Converter was simulated with the following specifications:

Vin = 150V; Vo = 200V; fs = 100kHz; Po = 400W; Rload = 1000 Ohms; D = 0.63; Lin = Lo = 1000 micro Henry; Cr = 2.12 nF; Cc = 1 micro farad; Ca = Co = 470 micro farad; Lr = 40 micro Henry.

VI. COMPARISON OF VARIOUS BIDIRECTIONAL DC-TO-DC CUK CONVERTER TOPOLOGIES BASED ON DIFFERENT PARAMETERS

PARAMETER	CONVENTIONAL DC-TO-DC CUK CONVERTER	BIDIRECTIONAL DC-to-DC CUK CONVERTER USING LEAD-ACID BATTERY	BIDIRECTIONAL QUASI-CUK DC-TO-DC CONVERTER WITH REDUCED VOLTAGE STRESS ON CAPACITOR AND CAPABILITY OF CHANGING THE OUTPUT POLARITY	ZVS ACTIVE-CLAMPING CUK CONVERTER
EFFICIENCY	90%	93%	92%	93%

Table 1.1 Comparison based on their Efficiencies

PARAMETER	CONVENTIONAL DC-TO-DC CUK CONVERTER	BIDIRECTIONAL DC-to-DC CUK CONVERTER USING LEAD-ACID BATTERY	BIDIRECTIONAL QUASI-CUK DC-TO-DC CONVERTER WITH REDUCED VOLTAGE STRESS ON CAPACITOR AND CAPABILITY OF CHANGING THE OUTPUT POLARITY	ZVS ACTIVE-CLAMPING CUK CONVERTER
DUTY RATIO	0.5454	0.44	0.40	0.63

Table 1. 2 Comparison based on their Duty Ratio

PARAMETER	CONVENTIONAL DC-TO-DC CUK CONVERTER	BIDIRECTIONAL DC-to-DC CUK CONVERTER USING LEAD-ACID BATTERY	BIDIRECTIONAL QUASI-CUK DC-TO-DC CONVERTER WITH REDUCED VOLTAGE STRESS ON CAPACITOR AND CAPABILITY OF CHANGING THE OUTPUT POLARITY	ZVS ACTIVE-CLAMPING CUK CONVERTER
LOAD	Rload = 15Ohms	Lead-Acid Battery (7, 2 Ah)	Rload = 55 Ohms	Rload = 1000 Ohms

Table 1. 3 Comparison based on their Load

VII. CONCLUSION

The various Bidirectional DC-to-DC Cuk Converter Topologies were proposed to overcome the limitations of Conventional DC-to-DC Cuk Converter. As the resonant circuits absorb almost all parasitic reactances, including transistor output capacitance and diode junction capacitance, the new converter operates with favorable switching conditions in all switching devices. Theoretical studies and simulated results allows us to draw the conclusion that the Bidirectional DC-to-DC Cuk Converter with Soft Switching Active Clamping Technique is suitable for high-frequency operation with high efficiency.

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