Published by :
https://www.ijert.org/
An International Peer-Reviewed Journal

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 15 Issue 11 , November - 2026

A Replica-Bitline Self-Timed 1-Kb 6T SRAM in SKY130: Compact Layout and Post-Layout PVT Validation using Open-Source Tools

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Abstract **- In a static random-access memory (SRAM), the sense amplifier must be enabled only after the selected cell has developed enough bit-line signal, yet without wasting time. A fixed sense-enable (SAE) delay cannot satisfy both conditions once layout parasitics and process, voltage and temperature (PVT) variation are considered. This paper presents a 1-Kb SRAM of 128 words by 8 bits, designed in the open-source SkyWater SKY130 process with Xschem, ngspice, Magic and netgen, and shows through layout and parasitic extraction that the safe fixed SAE delay shifts from 190 ps to 350 ps and that a fixed delay leaves only 0.4 mV of signal at the slow-slow corner, causing read failure. Two remedies are proposed: a compact mirrored bit cell with bit lines on metal 2, which reduces cell area by 73.3 percent and bit-line capacitance by about 55 percent, and a replica bit-line SAE generator laid out from the same cells. In full-chip simulations with extracted resistance and capacitance, the replica-timed SRAM reads correctly at the TT, SS and FF corners with a sensing margin of 86.7 to 113.7 mV, at least 4.4 times the 19.9 mV offset standard deviation of the sense amplifier obtained by Monte Carlo analysis, and reads 19.0 percent faster than the fixed-delay design at the FF corner.**

Keywords *- Monte Carlo analysis; open-source EDA; post-layout simulation; PVT variation; replica bit line; sense-amplifier timing; SKY130; SRAM*

I. INTRODUCTION

On-chip SRAM occupies a large share of the area of modern digital systems, and its read path often limits their speed [1]. During a read, a small cell discharges a heavily loaded bit line, and a latch-type sense amplifier converts the resulting small differential voltage into full logic levels. The instant at which the sense amplifier is enabled therefore controls both correctness and speed: an early enable resolves a signal smaller than the amplifier offset, while a late enable wastes time and bit-line energy [2], [3].

The required enable instant depends on the word-line rise time, the cell read current and the bit-line capacitance. These quantities change with the physical layout and with PVT conditions, whereas a delay chain built from logic gates follows the speed of logic, not of the memory cell. Designs verified only at schematic level, such as the 90 nm 1-Kb SRAM reported in [4], cannot reveal this problem, because the dominant loads are wire parasitics that appear only after layout.

This work uses the organisation of [4] as a baseline and carries it through a complete open-source flow in the SkyWater SKY130 process [5], from schematic to layout, design-rule check (DRC), layout-versus-schematic (LVS) check and resistance-capacitance (R+C) extraction. Open-source SKY130 SRAM macros have been generated with the OpenRAM compiler [6] and demonstrated in silicon [7]; the present work instead studies the sense-timing problem at the design level for a small array. The contributions are:

- quantification, through layout and extraction, of how the safe fixed SAE delay moves and how a fixed delay fails at the slow corner;
- a compact mirrored 6T cell with metal-2 bit lines and a word-line driver resized for the resulting array;
- a replica bit-line SAE generator built from the same cells, laid out and verified by DRC and LVS;
- full-chip post-layout validation at three process corners, with the sensing margin justified by a Monte Carlo analysis of the sense-amplifier offset.

II. RELATED WORK

Cell stability is usually expressed by the static noise margin (SNM), the side of the largest square that fits between the two transfer curves of the cross-coupled inverters [8]. Grossar *et al.* extended this analysis with current-based read and write metrics [9], and several studies showed that random threshold-voltage fluctuations reduce SNM and must be treated statistically [10], [11]. Pelgrom *et al.* showed that the standard deviation of transistor mismatch falls with the square root of gate area [12]; the same mismatch sets the input offset of latch-type sense amplifiers, whose sizing trades offset against speed [13], [14].

Amrutur and Horowitz introduced replica bit lines, built from dummy cells, to generate sense and word-line timing that tracks the real bit lines across operating conditions [15]. Later work reduced the local variation of the replica path itself by configurable driver cells [16], by digitising the replica delay [17] and by multi-stage parallel replica bit lines [18]. These techniques were demonstrated in commercial processes. For open processes, OpenRAM uses a replica bit line in its control logic [6], [7], but a step-by-step comparison of fixed and replica timing through layout, extraction and corners is not reported. The reference design [4] reports schematic-level results only.

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III. BASELINE DESIGN

The memory stores 128 words of 8 bits in a 32 × 32 array of 6T cells (Fig. 1). Address bits A6–A2 drive a 5:32 row decoder built from 2:4 and 3:8 predecoders, NAND3 gates with a word-line enable (EN) and inverting word-line drivers. Address bits A1–A0 drive a 2:4 column decoder that selects one of four columns per data bit through transmission-gate multiplexers. Each bit has a three-transistor PMOS precharge and equaliser, a write driver and a latch-type sense amplifier [13], [19]. The complete design contains 6,974 transistors.

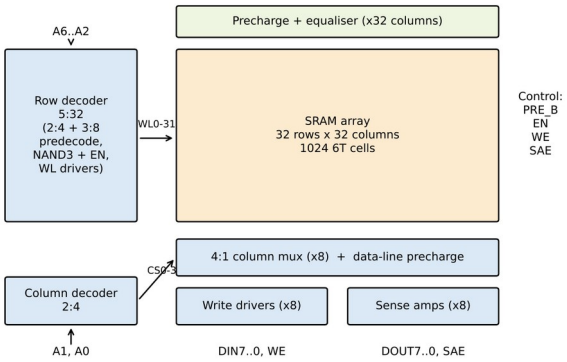

Fig. 1. Organisation of the 1-Kb SRAM (organisation adapted from [4]).

All devices use L = 0.15 µm. The cell uses pull-up, pull-down and access widths of 0.42, 1.0 and 0.5 µm, giving

$$CR = W_{PD} / W_{AX} = 2, \quad PR = W_{PU} / W_{AX} = 0.84 \qquad (1)$$

The cell ratio CR protects read stability and the pull-up ratio PR keeps the cell writable [19], [20]. The SNM was extracted with the 45-degree rotation method of [8]. Table I summarises the baseline results at the TT corner, 1.8 V and 27 °C.

TABLE I. BASELINE RESULTS (SCHEMATIC LEVEL)

Parameter	Value
Hold / read / write SNM	703.9 / 406.8 / 695.8 mV
Row decoder delay, EN to word line	≈170 ps
Sense-amplifier delay, SAE to output	62.4 ps
Full-chip functional test	4 / 4 reads correct
Read access, SAE 190 ps after EN	277 ps (113 mV at SAE)
Energy per read / write (8-bit word)	≈2.7 / 3.1–3.3 pJ

IV. FRAGILITY OF A FIXED SAE DELAY

The array was laid out in Magic [21] with a first, tileable cell of 3.92 × 5.40 µm (21.2 µm²) whose bit lines run on the local-interconnect layer, and extracted with parasitic capacitance. The extracted bit lines carry 23–28 fF of wire capacitance. Fig. 2 compares the bit-line signal available at the SAE instant before and after layout. The delay of 190 ps that leaves 113 mV before layout leaves only 7.1 mV after layout, and at 170 ps the read fails; a 300 ps delay is now needed. When a more compact layout later increased the word-line load, the safe delay moved again, to 350 ps. A fixed delay therefore has to be re-tuned after every layout change, and it still cannot follow the process corners, as Section VII shows.

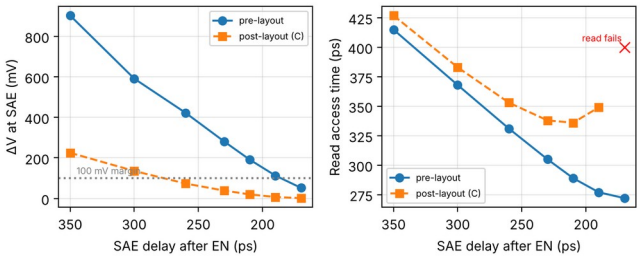

Fig. 2. Bit-line signal at SAE and read access time versus SAE delay, before and after layout.

V. PROPOSED DESIGN

A. Compact Mirrored Cell

The compact cell (Fig. 3) uses vertical diffusion strips and horizontal gates. Its right half is rotated by 180°, so that each storage node reaches the opposite inverter gate on local interconnect without crossing. Adjacent rows are mirrored and share their boundary contacts. Bit lines and supply lines run vertically on metal 2, and the word line is a poly line strapped with metal 1. Well and substrate taps are collected in tap rows at the top and bottom of the array. The cell measures 6.01 × 0.94 µm (5.65 µm²), and the 32 × 32 array core measures 192.32 × 30.08 µm. The 2 × 2, 4 × 4 and 32 × 32 arrays are free of DRC errors and match their schematics in LVS.

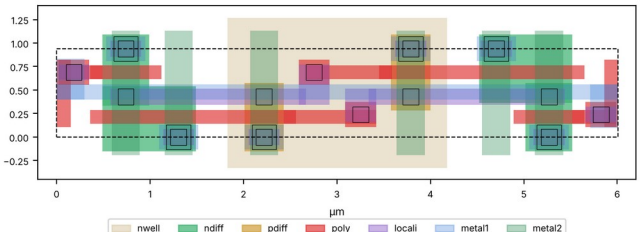

Fig. 3. Layout of the compact 6T cell (dashed line: cell boundary).

The wider array lengthens the word lines to about 55 fF. With the original 3.0/1.5 µm word-line driver, the word line became the bottleneck (safe SAE 350 ps, access 428 ps); doubling the driver to 6.0/3.0 µm restored a safe SAE delay of 260 ps and an access time of 346 ps.

B. Replica Bit-Line SAE Generator

The replica column (Fig. 4) is built from two variants of the compact cell. In a replica cell, node QB is strapped to VDD so that the cell always stores 0; in a dummy cell, the word line is tied to ground. The replica word line (RWL) is driven by the same NAND3 and driver as a real row, is loaded like a real word line and is enabled only during reads. Then k replica cells discharge the replica bit line (RBL) together, so that the RBL falls about k times faster than a real bit line. A skewed inverter (6.0/1.0 µm) with a high switching threshold V_M detects the falling RBL and drives SAE directly. Since the RBL and the real bit lines have the same geometry, the signal on a real bit line when SAE fires is approximately

$$\Delta V_{BL} \approx (V_{DD} - V_M) \cdot C_{RBL} / (k \cdot C_{BL}) \qquad (2)$$

which, to first order, does not depend on the cell current, and hence on the process corner or temperature: a slow cell delays SAE in proportion. Parameter k sets the margin. A column-level design study fixed the detector topology; on the full chip k was

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International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 15 Issue 11 , November - 2026

tuned from 12 to 10 after the laid-out replica was extracted (Section VII). The final column contains 10 replica and 22 dummy cells (6.01 × 30.08 µm), is DRC clean and matches its schematic in LVS. Its extracted RBL capacitance of 9.17 fF equals that of a real bit line, which is the physical basis of the tracking. The RWL driver and the detector are at schematic level.

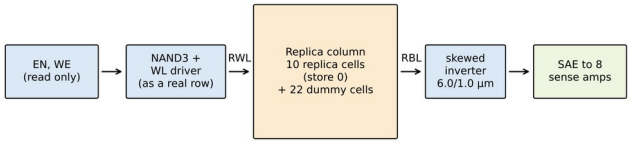

Fig. 4. Replica bit-line SAE generator (final design).

VI. EXPERIMENTAL SETUP

All circuits use the SKY130A process design kit built with open_pdks [5], with schematics in Xschem 3.4.8, simulation in ngspice-36, layout and extraction in Magic 8.3 [21] and LVS in netgen. The supply is 1.8 V. Every schematic was netlisted and checked before simulation, and every layout was checked by DRC and LVS. The compact array and the replica column were extracted with resistance and capacitance; the array netlist contains about 10,800 resistors and 35,400 capacitors. To keep simulation tractable, resistors below 50 Ω were merged and capacitors below 1 aF removed. A sanity check found three implausible lumped capacitors produced by the extractor (212.9 fF on one bit line and two supply-to-ground well capacitances), which were removed; the well capacitances do not affect timing with an ideal supply. In the full-chip tests the extracted array and replica column are combined with the schematic-level periphery. Each run reads 0xA5 from address 127 and 0x5A from address 0 twice, so every data bit is read as both 0 and 1. Sense-amplifier offset was obtained from 300 Monte Carlo samples per corner with the SKY130 mismatch models, using a bisection on the input difference for each sample.

VII. RESULTS AND DISCUSSION

A. Full-Chip Post-Layout Validation

Table II and Fig. 5 compare the replica SAE (k = 10, laid out and extracted) with the fixed delay of 260 ps, which is the best safe fixed value at the TT corner. At TT both schemes read correctly with almost the same access time. At SS the fixed delay fires with only 0.4 mV of signal and the read fails, whereas the replica postpones SAE to 366 ps and reads correctly with 106.0 mV. At FF the fixed delay waits for 424.9 mV that is not needed, whereas the replica fires at 185 ps and completes the read in 255 ps.

TABLE II. FULL-CHIP POST-LAYOUT RESULTS (COMPACT ARRAY, R+C)

Corner / SAE source	SAE delay	ΔV at SAE	Access
TT, fixed	260 ps	111.6 mV	346 ps
TT, replica	253 ps	86.7 mV	347 ps
SS, fixed	260 ps	0.4 mV	fails
SS, replica	366 ps	106.0 mV	499 ps
FF, fixed	260 ps	424.9 mV	315 ps
FF, replica	185 ps	113.7 mV	255 ps

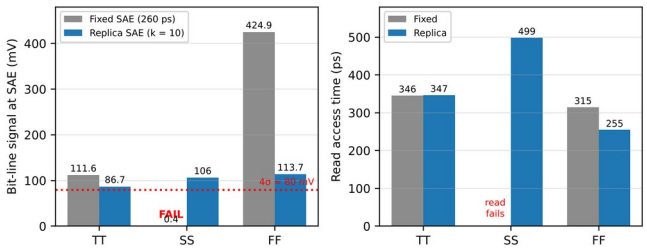

Fig. 5. Signal at SAE and read access time across process corners.

The replica keeps the signal within 86.7–113.7 mV at all three corners, a spread of 27.0 mV, compared with 0.4–424.9 mV for the fixed delay. The tracking is not perfect: the TT margin is the smallest because the replica and real paths are not loaded identically, but the residual spread is about sixteen times smaller than with the fixed delay. With the earlier 12-cell replica, the laid-out column fired 6–11 ps earlier than its schematic version and left 77.9 mV at FF; reducing k to 10 restored the margin at the cost of 2–3 ps in access time.

B. Sense-Amplifier Offset

Table III lists the Monte Carlo offset statistics. The mean is close to zero, as expected for a symmetric latch, and the standard deviation σ is about 20 mV at every corner. Since the memory contains eight sense amplifiers, a 4σ target of about 80 mV is appropriate. The replica margin of at least 86.7 mV corresponds to 4.4σ, whereas the fixed delay at SS (0.4 mV) is far below even 1σ. The analysis covers sense-amplifier mismatch only; the replica-cell mismatch is reduced by averaging over ten cells [16], [17].

TABLE III. SENSE-AMPLIFIER OFFSET, 300 SAMPLES PER CORNER

Corner	Mean	σ	4σ	Worst
TT	−0.47 mV	19.87 mV	79.9 mV	59.8 mV
SS	+0.38 mV	19.20 mV	77.2 mV	57.2 mV
FF	−0.45 mV	20.15 mV	81.1 mV	61.3 mV

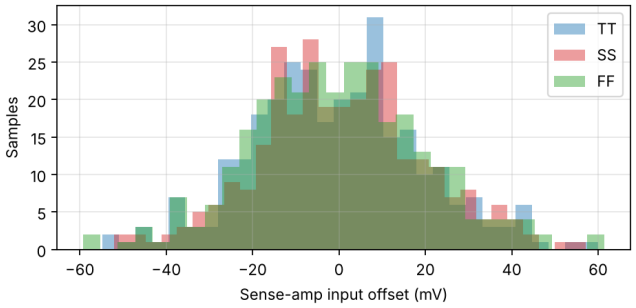

Fig. 6. Distribution of the sense-amplifier input offset.

C. Existing versus Proposed Design

Table IV compares the existing approach (first layout, fixed SAE) with the proposed design. The relative improvement η in a quantity X is

$$\eta = (X_e - X_p) / X_e \times 100\ \% \qquad (3)$$

where X_e and X_p are the existing and proposed values. The FF access time thus improves by (315 − 255)/315 = 19.0 %, the cell area by (21.2 − 5.65)/21.2 = 73.3 %, and the bit-line capacitance, taking the mid-points of the extracted ranges, by

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International Journal of Engineering Research & Technology (IJERT)
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(25.5 − 11.5)/25.5 = 54.9 %. At TT the replica is 1 ps (0.3 %) slower than the fixed delay, the price of robustness at the slow corner.

TABLE IV. EXISTING VERSUS PROPOSED DESIGN

Parameter	Existing	Proposed	Change
Cell area	21.2 µm²	5.65 µm²	−73.3 %
Bit-line layer / C	li1 / 23–28 fF	metal 2 / 10–13 fF	−54.9 %
Read at SS	fails (0.4 mV)	correct (106.0 mV)	failure removed
Access at FF	315 ps	255 ps	−19.0 %
Access at TT	346 ps	347 ps	+0.3 %
ΔV spread, TT/SS/FF	424.5 mV	27.0 mV	tracks PVT

Compared with [4], which reports a 90 nm, 1 V design at schematic level, the present results are obtained under different conditions and definitions and are therefore not directly comparable; the additions of this work are the layout, the extraction, the corner analysis and the PVT-tracking sense enable.

VIII. CONCLUSION

A 1-Kb 6T SRAM was designed and taken through layout and R+C extraction in the open-source SKY130 process. The study shows that a fixed sense-enable delay chosen at schematic level becomes unsafe after layout and fails at the slow corner. A compact mirrored cell with metal-2 bit lines reduces cell area by 73.3 % and bit-line capacitance by about 55 %, and a replica bit-line SAE generator built from the same cells keeps the sensing margin within 86.7–113.7 mV (at least 4.4σ of the sense-amplifier offset) at the TT, SS and FF corners, while reading 19.0 % faster than the fixed delay at FF. The periphery, the RWL driver and the detector are still at schematic level, full-chip temperature and supply corners and cell mismatch are not yet included, and the cell is larger than production SKY130 cells [7]. Layout of the periphery, full PVT and mismatch coverage and a lower-offset sense amplifier are left for future work.

ACKNOWLEDGMENT

The authors thank the Department of ECE, S.K.U. College of Engineering & Technology, Anantapuramu, and the developers of the open-source SKY130 PDK and of the Xschem, ngspice, Magic and netgen tools. An AI assistant was used to help prepare simulation and layout scripts and to edit the manuscript; all designs, simulations and reported results were produced and verified by the authors.

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