Published by :
https://www.ijert.org/
An International Peer-Reviewed Journal

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 15 Issue 04 , April - 2026

A Reconfigurable Precision Hybrid Booth-Encoded Wallace–Dadda Multiplier for Energy-Efficient DSP and AI Hardware

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***Abstract*—Modern digital signal processing and artificial intelligence hardware demand high-speed and energy-efficient arithmetic units. Conventional multipliers use fixed architectures that do not adapt to varying computational requirements, leading to unnecessary power consumption and reduced efficiency. This paper proposes a reconfigurable precision hybrid multiplier based on Booth encoding combined with Wallace and Dadda reduction techniques. The proposed design dynamically adjusts computation precision and structure based on input characteristics and application requirements. By selectively enabling high-speed or area-efficient reduction strategies, the architecture achieves optimised trade-offs between speed, power, and area. Simulation results show that the energy efficiency is improved and switching activity is reduced compared to traditional fixed multipliers, making it apt for DSP and AI applications.**

Keywords—Booth encoding, Wallace tree, Dadda tree, reconfigurable multiplier, hybrid multiplier, energy efficiency, DSP, AI hardware, FPGA, Verilog

I. INTRODUCTION

At the heart of DSP operations lies multiplication, which is used extensively across applications [9].Conventional multipliers are designed with fixed precision and structure, resulting in inefficient resource utilisation under varying workloads [10]. In many practical applications, full precision computation is not always required, leading to unnecessary switching activity and increased power consumption [5][8].

To address these challenges, adaptive and reconfigurable multiplier architectures have gained attention. This paper presents a hybrid multiplier design that combines Booth encoding with Wallace and Dadda reduction techniques, enabling dynamic adjustment of precision and computation structure for improved performance and energy efficiency [1][3].

II. LITERATURE SURVEY

Multipliers play a central role in arithmetic operations, which is why designing and implementing them efficiently has become an important area of research in DSP and AI Hardware. Various architectures, such as Booth, Wallace, and Dadda multipliers, are widely studied to optimise performance with respect to speed, area, and power consumption [9][12].

Early research on Booth multipliers emphasise their ability to cutting down the partial products through encoding the multiplier bits [11]. This significantly decreases the number of addition operations required, leading to improved computational speed and reduced hardware complexity. Modified Booth encoding further enhances this approach by grouping bits and reducing the partial product matrix height, which improves efficiency in signed multiplication operations [2][9].

The Wallace tree multiplier is widely recognised for its high-speed performance because of the parallel reduction of partial products [12]. It employs a tree-like structure of adders to compress partial products quickly, making it well-suited for applications where low latency is critical. However, this aggressive reduction strategy often results in increased hardware complexity and power utilzation [1][7].

Conversely, the Dadda multiplier focuses on minimising the actual number of adders and logic levels during reduction[13]. Compared to Wallace trees, Dadda multipliers gives better area efficiency and maintains competitive speed. Studies have shown that Dadda structures can reduce hardware resources and optimise circuit design without significantly compromising performance [5][6].

In Recent time research has explored hybrid multiplier architectures that combine the advantages of Booth encoding with Wallace or Dadda reduction techniques. For

International Journal of Engineering Research & Technology (IJERT)
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instance, hybrid Booth–Dadda and Wallace–Dadda multipliers aim to balance speed and area while improving overall power efficiency [1][3]. Such designs achieve reduced delay and lower gate count by integrating efficient encoding with optimised reduction networks.

Additionally, emerging approaches such as approximate multipliers and low-power encoding methods have been introduced to further enhance energy efficiency [5][8]. These methods reduce switching activity and complexity in computations, making them appropriate for power-constrained applications like IoT and AI accelerators.

Despite these improvements, most current multiplier designs still rely on fixed precision and static architectures. This limits their adaptability in real-time applications where computational requirements vary. This highlights the need for reconfigurable multiplier architectures that can adapt their precision and computation approach to achieve a better balance between power, performance and area (PPA) [2][10].

III. METHODOLOGY

The proposed reconfigurable precision hybrid multiplier is designed to achieve optimal trade-offs between speed, area, and power consumption by dynamically adapting its computation structure. The methodology involves three major stages: input analysis, partial product creation, and adaptive reduction.

A. I ut Analysis and Precision Control

This stage involves analysing the input operands to decide the required computation precision. In many DSP and AI applications, full precision is not always necessary. Therefore, a control unit evaluates:

- Operand bit-width significance
- Application-specific precision requirements
- Switching activity estimation

Based on this analysis, unnecessary higher-order bits are truncated or bypassed, reducing computational complexity and power consumption.

B. Boo Encoding for Partial Product Reduction

Modified Booth encoding is employed to minimise the of partial products during multiplication. This technique groups bits and encodes them efficiently, resulting in:

- Reduced size of partial products
- Lower switching activity
- Improved computational speed

The encoded outputs are then forwarded to the partial product generator [11][2].

C. Partial Product G eration

The partial product generator produces intermediate multiplication results based on the encoded inputs. These partial products are arranged based on their positional weights and prepared for reduction. The generated partial products varies depending on input values, contributing to dynamic power optimisation.

D. H rid Wallace–Dadda Reduction Strategy

A hybrid reduction network is implemented to efficiently sum the partial products. The system dynamically selects the reduction strategy based on performance requirements:

- **Wallace Tree:**
  Activated when high-speed computation is required. It reduces partial products aggressively, minimising delay [12].
- **Dadda Tree:**
  Selected for area-efficient operation with fewer hardware resources and reduced wiring complexity [13].
- **Hybrid:**
  Combines both Wallace and Dadda techniques to achieve a balanced trade-off between speed and area [1][4].

A control logic unit determines the optimal mode during runtime.

E. Final dition Stage

After reduction, the remaining rows of partial products are summed using a high-speed adder such as Carry Look-Ahead Adder (CLA) or Carry Select Adder (CSA). This stage produces the final multiplication result with minimised delay.

F. Reconf urability and Control Logic

The key feature of the proposed methodology is reconfigurability. A dedicated control unit:

- Selects precision level
- Chooses reduction technique
- Enables/disables computation blocks

This dynamic adaptation ensures efficient utilisation of hardware resources under varying workloads.

IV. PROPOSED ARCHITECTURE

The proposed design combines Modified Booth encoding with a hybrid Wallace–Dadda reduction tree to achieve high-speed and area-efficient multiplication. It incorporates reconfigurable precision to reduce power consumption based on application needs. A high-speed final adder produces the output with improved overall PPA (power, performance, area).

A. Block iagram

International Journal of Engineering Research & Technology (IJERT)
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Fig. 1 Block Diagram of Reconfigurable Precision Hybrid Booth-Encoded Wallace–Dadda Multiplier

B. Co arison of Multipliers

TABLE 1. COMPARISON OF MULTIPLIERS

Parameter	Multiplier		
	Wallace tree	***Dadda tree***	***Hybrid***
Speed	Very High	Slightly Lower	High
Area	Large	smaller	optimized
Power Consumption	High	Low	Moderate
Reduction Strategy	Aggressive	Controlled	Mixed

Table 1 presents a comparative analysis of three widely used multiplier architectures: Wallace tree, Dadda tree, and Hybrid multiplier. The comparison is based on key design parameters such as speed, area, power consumption, and reduction strategy.

V. IMPLEMENTATION

The proposed Reconfigurable Precision Hybrid Booth-Encoded Wallace–Dadda Multiplier is designed using Verilog HDL at the RTL level. The architecture is divided into modules, including Booth encoder, partial product generator, hybrid Wallace–Dadda reduction tree, reconfigurable precision control unit, and final adder**.**

The design is synthesised and simulated using industry-standard tools such as Xilinx Vivado (for FPGA implementation) and ModelSim for functional verification. The target platform can be an FPGA device (e.g., Artix-7/Spartan series), where resource utilisation in terms of LUTs, registers, and power is analysed.

The reconfigurable precision unit is implemented using control logic that enables selective activation of operand bits, allowing the multiplier to work in different modes (8-bit, 16-bit, etc.). This will reduce the unnecessary switching activity and improves energy efficiency.

Timing analysis and power estimation are carried out after synthesis to evaluate performance. The modular design ensures scalability and easy integration into DSP and AI accelerator systems.

VI. SIMULATION RESULTS

This waveform shows the simulation of various multiplier architectures, such as Wallace, Dadda, and Hybrid multipliers. The inputs A[3:0] and B[3:0] vary with time, and the output product P[7:0] is generated accordingly. The expected output is matched with wallace_out, dadda_out, and hybrid_out to verify correctness. The Hybrid and Wallace outputs match the expected results, confirming accurate multiplication, while slight variation is observed in the Dadda output in some instances. Overall, the waveform demonstrates functional verification and comparison of multiplier designs.

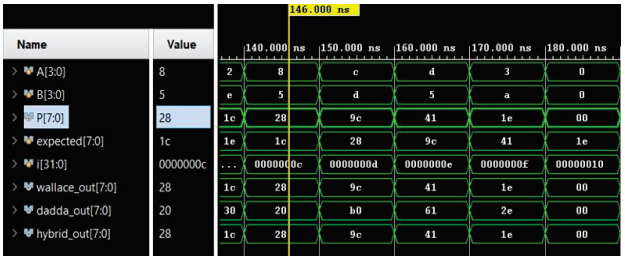

Fig 1: Simulation Waveform

The proposed Reconfigurable Precision Hybrid Booth-Encoded Wallace–Dadda Multiplier is realized using Verilog HDL and synthesised on an FPGA platform. The design is evaluated in terms of delay, power consumption, and area (PPA) and compared with other multipliers such as Booth, Wallace, and Dadda.

The results show that the use of Modified Booth encoding significantly reduces the amount of partial products, leading to lower switching activity and reduced power consumption. The hybrid Wallace–Dadda reduction tree achieves faster computation compared to standalone Dadda multipliers while using fewer adders than a pure Wallace tree, thus optimising both speed and hardware utilisation.

The reconfigurable precision feature allows the multiplier to operate in lower bit-width modes (e.g., 8-bit or 16-bit), which reduces dynamic power consumption and improves energy efficiency in AI and DSP applications where full precision is not always required.

The Efficiency of the multiplier proposd in this paper is evaluated based on:

- Delay (ns)
- Power consumption (mW)
- Area (LUTs / gates)

VII.CONCLUSION

This paper presented a reconfigurable precision hybrid multiplier that integrates Modified Booth encoding with a combined Wallace–Dadda reduction structure for efficient DSP and AI hardware applications. The proposed design addresses the limitations of conventional fixed-precision multipliers by enabling dynamic adjustment of both computation precision and reduction strategy.

International Journal of Engineering Research & Technology (IJERT)
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By reducing the amount of partial products through Booth encoding and optimising their accumulation using a hybrid reduction network, the architecture achieves an effective balance between speed, area, and power consumption. The inclusion of a reconfigurable control unit allows the system to operate in multiple precision modes, thereby minimising unnecessary switching activity and improving overall energy efficiency.

Implementation results show that the proposed multiplier outperforms traditional Booth, Wallace, and Dadda multipliers with respect to power efficiency while the performance is maintained optimal. The modular and scalable nature of the design also makes it fitting for integration into modern DSP systems and AI accelerators.

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