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A PV-Fed Reduced-Switch Nine-Level Inverter for Home Grid Interfacing and Electric Vehicle Charging

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Abstract - **The rapid penetration of photovoltaic (PV) based distributed generation and the growing demand for residential electric vehicle (EV) charging systems necessitate compact, efficient, and high-power-quality inverter topologies. Conventional multilevel inverters suffer from increased component count, higher switching losses, and complex control requirements, which limit their suitability for home-grid and EV charging applications. This paper presents a PV-fed reduced-switch nine-level switched-capacitor inverter designed to support both grid-connected and islanded operation while supplying residential loads and EV chargers. The proposed topology generates nine distinct voltage levels (±4Vdc, ±3Vdc, ±2Vdc, ±Vdc, and zero) using only eight power switches, four capacitors, and three diodes, thereby significantly reducing hardware complexity and switching losses compared to conventional multilevel inverter structures. A boost converter integrated with a Perturb and Observe (P&O) based Maximum Power Point Tracking (MPPT) algorithm ensures optimal power extraction from the PV array under varying irradiation conditions. Furthermore, a fuzzy logic-based control strategy is employed for grid synchronization, voltage regulation, and smooth transition between grid-connected and islanded modes. The proposed system is validated through detailed MATLAB/Simulink simulations. Simulation results demonstrate stable operation under irradiation variation, load changes, and grid disconnection scenarios. The inverter achieves a high-quality output with a load current total harmonic distortion (THD) of approximately 0.22%, satisfying grid power quality standards. The results confirm that the proposed reduced-switch nine-level inverter is a compact, efficient, and cost-effective solution for PV-based home-grid integration and EV charging applications.**

Keywords - Nine-level inverter, reduced switches, photovoltaic system, EV charging, grid-connected inverter

I. INTRODUCTION

The increasing penetration of renewable energy sources, particularly photovoltaic (PV) systems, has significantly transformed modern power generation and distribution networks. Residential microgrids integrating PV generation, home loads, and electric vehicle (EV) charging stations demand power electronic interfaces that are compact, efficient, and capable of delivering high-quality power to both local loads and the utility grid. In this context, DC–AC inverters play a critical role in enabling reliable power conversion, grid synchronization, and bidirectional energy flow. However, conventional inverter topologies often struggle to meet stringent power quality and efficiency requirements when operated under varying irradiation and load conditions.

Multilevel inverters (MLIs) have emerged as an effective solution for medium- and high-power applications due to their ability to generate high-quality output voltage with reduced harmonic distortion and lower voltage stress on power devices. Classical MLI configurations such as diode-clamped (NPC), flying-capacitor (FC), and cascaded H-bridge (CHB) inverters have been widely reported in the literature [1]–[3]. Despite their advantages, these topologies suffer from inherent drawbacks including a large number of semiconductor switches, multiple isolated DC sources, complex voltage balancing mechanisms, and increased switching losses. These limitations lead to higher system cost, reduced reliability, and increased control complexity, making them less attractive for residential PV and EV charging applications.

To overcome these challenges, recent research has focused on reduced-switch-count and switched-capacitor-based multilevel inverter topologies [4]–[7]. Switched-capacitor (SC) inverters offer intrinsic voltage boosting capability without the need for bulky transformers or additional DC–DC converters, while simultaneously reducing component count. Several SC-based MLIs have been proposed to enhance voltage gain, self-balance capacitor voltages, and minimize total standing voltage across switches [8], [9]. However, many existing SC-MLI configurations still require a relatively high number of power devices or suffer from increased conduction losses and limited scalability.

In parallel, the rapid growth of electric vehicles has introduced additional technical requirements for residential power conversion systems, including dynamic load handling, fast transient response, and seamless transition between grid-connected and islanded operation. In EV charging scenarios, maintaining low total harmonic distortion (THD), high efficiency, and stable voltage regulation is essential to ensure battery safety and grid compliance. Therefore, there is a growing demand for inverter topologies that combine reduced hardware complexity with advanced control strategies capable of supporting both home-grid operation and EV charging infrastructure.

Motivated by these challenges, this paper proposes a PV-fed reduced-switch nine-level switched-capacitor inverter suitable for home-grid integration and EV charging applications. The proposed topology generates nine voltage levels using only eight power switches, thereby significantly reducing component count

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and switching losses compared to conventional MLIs. A boost converter with Perturb and Observe (P&O) based maximum power point tracking (MPPT) ensures optimal PV power extraction under varying irradiation conditions. Furthermore, a fuzzy logic-based control strategy is employed to achieve effective grid synchronization, voltage regulation, and smooth transition between grid-connected and islanded modes. The effectiveness of the proposed system is validated through detailed MATLAB/Simulink simulations, demonstrating excellent power quality with very low current THD and robust performance under dynamic operating conditions.

II. THE FRAMEWORK OF PROPOSED SYSTEM

A. Description of the Proposed 9-Level MLI With PV Source

The photovoltaic (PV) source generates DC power, which is monitored through PV voltage and current signals. A P&O-based maximum power point tracking (MPPT) algorithm controls the boost converter to extract maximum available power under varying irradiation conditions and regulate the DC-link voltage. The boosted DC output is supplied to the multilevel inverter, which converts it into high-quality AC power. Grid voltage, current, and load voltage are continuously sensed and processed by a fuzzy logic–based grid synchronization controller as shown in Figure 1. Based on the reference voltage generated, the switching circuit produces appropriate gating signals, ensuring proper synchronization, low harmonic distortion, stable power injection, and seamless operation in both grid-connected and islanded modes.

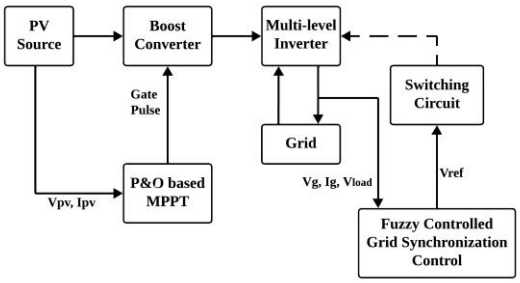

Figure 1: Proposed system Block diagram

The proposed circuit as shown in Figure 2 represents a nine-level switched-capacitor multilevel inverter with a reduced switch count, designed to produce multiple voltage levels from a single DC source for photovoltaic applications. The topology comprises eight controlled power switches (S1–S8), four capacitors (C1–C4), and three diodes (D1–D3). Capacitors C1–C4 are charged from the input DC source and are selectively reconfigured in series or parallel combinations through switches S1–S4 and diodes D1–D3, forming a switched-capacitor network that provides inherent voltage boosting without the need for a transformer or additional DC–DC conversion stages.

By selecting appropriate switching states, the inverter generates nine distinct output voltage levels, namely ±Vdc, ±2Vdc, ±3Vdc, ±4Vdc, and zero. Switches S5–S8 form the output stage and enable polarity reversal, allowing symmetrical positive and negative voltage generation across the load. This configuration significantly reduces the number of power devices, gate driver requirements, and switching losses compared to conventional multilevel inverter topologies, while achieving improved output waveform quality, lower voltage stress on switches, and reduced total harmonic distortion.

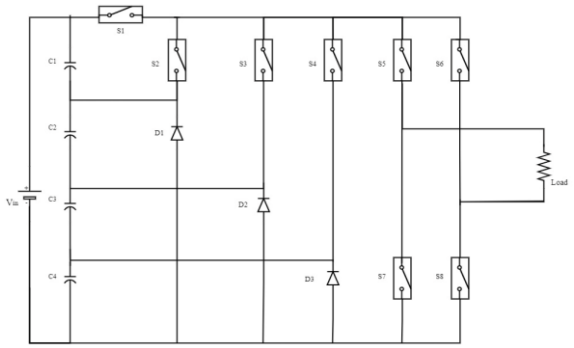

Figure 2: Proposed Circuit Diagram of Nine Level Inverter

B. Operation of the Proposed 9-Level MLI

In all the modes of operation Vin values is always represents the Vdc, in which Vdc is the source voltage fed from the photo voltaic block which is monitored by the P & O based MPPT controller. The inverter receives the 230V of voltage from PV array, which provide source to operate the proposed inverter.

In mode 1, capacitors C1, C2, and C3 are charged simultaneously from the input DC source. Once charged, these capacitors are connected in series with the input voltage Vin through the appropriate switching configuration. As a result, the individual capacitor voltages add to the source voltage, producing the maximum output voltage level across the load as shown in Figure 3. This operating state enables the inverter to achieve the highest positive voltage step while maintaining proper capacitor voltage balance.

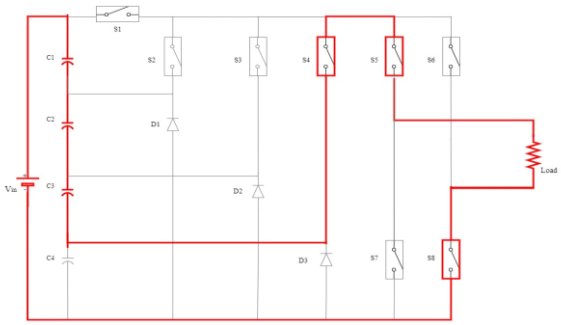

Figure 3: Conduction Path of Proposed Topology in Mode 1

In Mode 2, capacitors C1 and C2 are charged from the input DC source Vin, while capacitor C3 is bypassed through the switching network. During this operating state, the charged capacitors C1 and C2 are reconfigured in series with the input source. Consequently, their voltages combine with Vin to generate a stepped output voltage across the load equal to Vin −VC1−VC2, as established by the corresponding conduction path illustrated in Figure 4.

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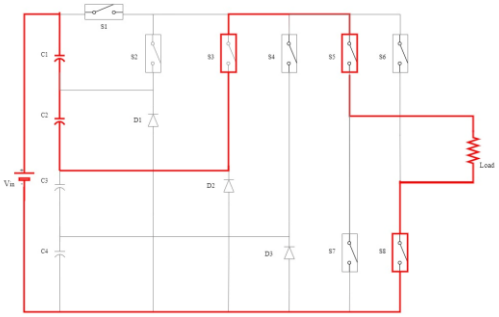

Figure 4: Conduction Path of Proposed Topology in Mode 2

In mode 3, only capacitor C1 is charged from the input DC source while the remaining capacitors are bypassed. The charged capacitor C1 is then connected in series with the input voltage Vin as illustrated in Figure 5. As a result, the voltage applied across the load is equal to Vin−Vc1, producing a reduced output voltage level.

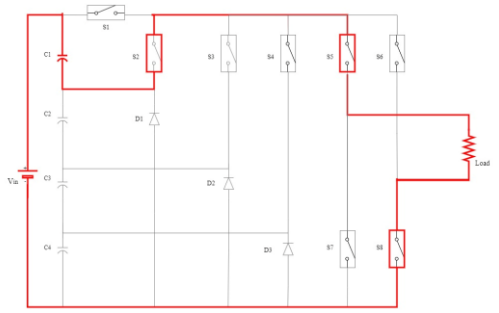

Figure 5: Conduction Path of Proposed Topology in Mode 3

In Mode 4, the input DC source Vin is directly connected to the load, and all capacitors are isolated from the conduction path. Switches S1, S5, and S8 are turned ON to establish a direct current path between the source and the load. As a result, the inverter applies the fundamental or base voltage level equal to Vin across the load, providing a stable reference voltage level for multilevel waveform generation, as illustrated in Figure 6.

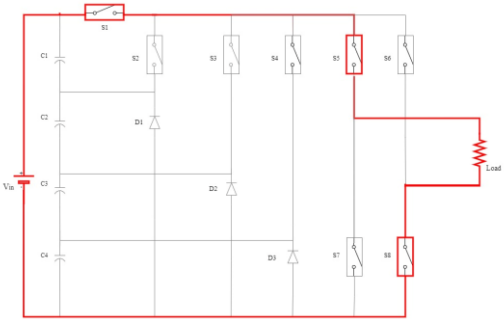

Figure 6: Conduction Path of Proposed Topology in Mode 4

In Mode 5, all capacitors remain in their charged condition while the switching configuration completely isolates the input DC source from the load. During this state, none of the power switches establish a conduction path between the source and the load, preventing any energy transfer. As a result, the inverter output is clamped to zero, and no voltage is applied across the load. This operating mode generates the zero-voltage level required for multilevel waveform synthesis, as illustrated in Figure 7.

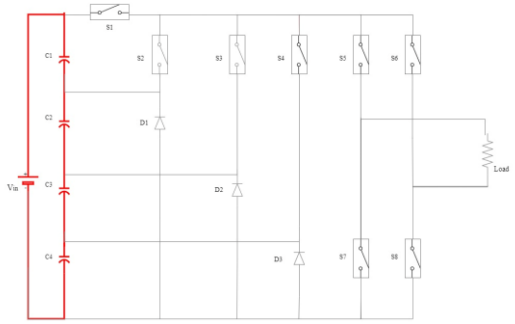

Figure 7: Conduction Path of Proposed Topology in Mode 5

In Mode 6, capacitors C1, C2, and C3 are charged and subsequently connected in series in opposition to the input DC source Vin, as shown in Figure 8. In this configuration, the series-combined capacitor voltages subtract from the input source voltage, resulting in a negative output voltage across the load equal to VC3−VC2−VC1−Vin.

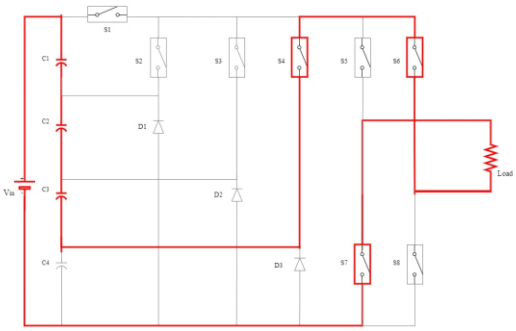

Figure 8: Conduction Path of Proposed Topology in Mode 6

In Mode 7, capacitors C1 and C2 are charged from the input source while capacitor C3 is bypassed, as illustrated in Figure 9. During this operating state, the charged capacitors are connected in series in opposition to the input voltage Vin. As a result, the inverter generates a negative output voltage across the load equal to VC2−VC1−Vin.

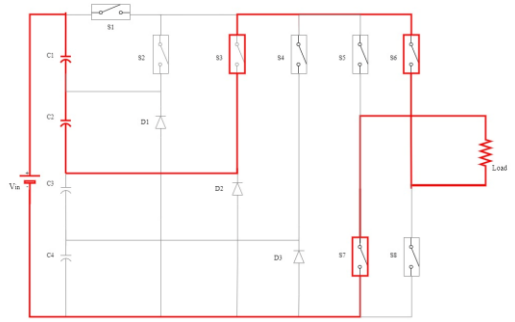

Figure 9: Conduction Path of Proposed Topology in Mode 7

In Mode 8, only capacitor C1 is charged from the input DC source, while the remaining capacitors are bypassed through the switching network, as illustrated in Figure 10. During this operating state, the charged capacitor C1 is connected in series in opposition to the input voltage Vin. This series opposition causes the capacitor voltage to subtract from the input source, resulting in a reduced negative output voltage level across the load equal to VC1−Vin. This mode contributes to the stepped negative voltage generation required for multilevel operation.

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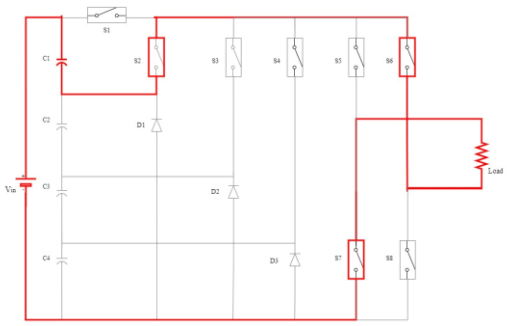

Figure 10: Conduction Path of Proposed Topology in Mode 8

In mode 9, the input voltage Vin is directly connected to the load, as shown in Figure 11. Switches S1, S6, and S7 are turned ON to establish the conduction path. This switching configuration produces the fundamental output voltage level equal to Vin across the load.

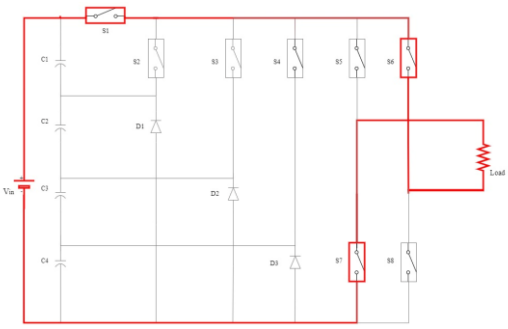

Figure 11: Conduction Path of Proposed Topology in Mode 9

The switching states of the proposed 9 level inverter along with the corresponding output voltage levels is shown in below Table I. The inverter operates in nine distinct states during one fundamental cycle, enabling the generation of positive, negative, and zero voltage levels. Each state is defined by a specific combination of ON switches, which determines both the output voltage magnitude of the nine-level inverter.

TABLE I: Switching table of the proposed inverter

S1	S2	S3	S4	S5	S6	S7	S8	Vo
OFF	OFF	OFF	ON	ON	OFF	OFF	ON	**Vdc**
OFF	OFF	ON	OFF	ON	OFF	OFF	ON	**2Vdc**
OFF	ON	OFF	OFF	ON	OFF	OFF	ON	**3Vdc**
ON	OFF	OFF	OFF	ON	OFF	OFF	ON	**4Vdc**
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	**zero**
OFF	OFF	OFF	ON	OFF	ON	ON	OFF	**-Vdc**
OFF	OFF	ON	OFF	OFF	ON	ON	OFF	**-2Vdc**
OFF	ON	OFF	OFF	OFF	ON	ON	OFF	**-3Vdc**
ON	OFF	OFF	OFF	OFF	ON	ON	OFF	**-4Vdc**

C. Modeling of PV Array

A preliminary comprehension of a solar cell's performance can be achieved by conceptualizing it as a diode. In this model, light energy, manifested as photons possessing the requisite energy level, strikes the cell and produces electron-hole pairs. The electric field created at the diode's junction separates the electrons and holes, subsequently propelling them through an external circuit due to this junction potential. However, there are losses linked to the series and shunt resistance of the cell, in addition to some current leaking back across the p-n junction. This results in the equivalent circuit depicted in Figure 12 below:

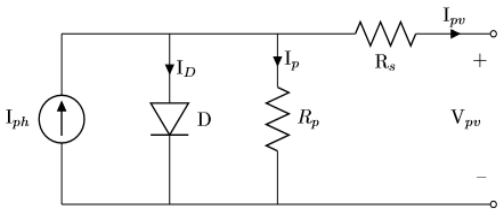

Figure 12*:* Equivalent Circuit of PV cell

The photovoltaic cell can be modeled as a diode in parallel with a constant current source and a shunt resistor. These three components are arranged in series with the series resistor. The output terminal current, I, is equivalent to the light-generated current, Iph, reduced by the diode current, ID, and the shunt-leakage current, Ip. The series resistance, Rs, represents the internal resistance to current flow and is affected by the depth of the p-n junction, the presence of impurities, and the contact resistance. In contrast, the shunt resistance, Rsh, is inversely related to the leakage current to the ground. In an ideal photovoltaic cell, Rs is equal to 0 (indicating no series loss), and Rp is equal to 1 (indicating no leakage to the ground). The conversion efficiency of the photovoltaic cell is highly sensitive to small changes in Rs, while it remains largely unaffected by variations in Rp. A minor increase in Rs can result in a substantial decrease in the photovoltaic output. In the equivalent circuit, the current delivered to the external load is equal to the current Iph generated by illumination, diminished by the diode current ID and the ground-shunt current Ish. The fundamental equation governing the photovoltaic cell can be derived from the principles of the Shockley diode equation and semiconductor theory.

The essential equations required for the design of a photovoltaic (PV) cell are presented below:

Utilizing Kirchhoff's Current Law (KCL), we get

$$I_{pv} = I_{ph} - I_D - I_p \tag{1}$$

As per the Shockley diode equation, we have

$$I_D = I_0 - \exp\left(\frac{e(V_p + R_s I)}{nK_b T}\right) - 1 \tag{2}$$

Substituting this value into equation (1) yields

$$I_{pv} = I_{ph} - I_0\left[\exp\left(\frac{e(V_p + R_s I)}{nK_b T}\right)\right] - I_p \tag{3}$$

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Finally, by incorporating the value of Ip into equation (3), we obtain

$$I_{pv} = I_{ph} - I_0 \left[\exp\left(\frac{e(V_p + R_s I)}{nK_b T}\right)\right] - \frac{V_p + R_s I}{R_p} \quad (4)$$

The output current under standard test conditions (STC) is expressed as:

$$I_{pv} = I_{ph,ref} - I_{0,ref} \left[\exp\left(\frac{V_p}{a_{ref}}\right) - 1\right] \quad (5)$$

Considering the short circuit condition where V=0, we find

$$I_{pv} = I_{ph,ref} - I_{0,ref} \left[\exp\left(\frac{0}{a_{ref}}\right) - 1\right] = I_{ph,ref} \quad (6)$$

However, the photocurrent is influenced by light intensity and temperature. Thus, the equation for photocurrent can be articulated as

$$I_{ph} = \frac{G}{G_{ref}}\left(I_{ph,ref} + \mu_{sc}.\Delta T\right) \quad (7)$$

Where G signifies Irradiance, Gref indicates the Irradiance at Standard Test Conditions (STC), and ΔT =Tc -Tref, with Tref being the cell temperature at STC calculated as 25 + 273 = 298. The temperature coefficient for short circuit current, μsc (A/K), is provided by the manufacturer, while I*ph,ref* denotes the Photocurrent (A) at STC.

Ultimately, through simplification, we derive the reverse current saturation as

$$I_0 = I_{0,ref}\left(\frac{T_c}{T_{ref}}\right)^3 \exp\left[\frac{-q\sum_g}{AK}\right] \left(\frac{1}{T_c} - \frac{1}{T_{ref}}\right) \quad (8)$$

Table II summarizes the electrical specifications of the single photovoltaic module employed in the proposed system. These parameters define the voltage, current, and power characteristics of the PV module and are used for accurate modeling and performance evaluation of the PV-fed inverter system.

TABLE II: Single PV Module Details

Parameters	Values
Open circuit voltage (Voc)	36.86V
Short-circuit current (Isc)	8.3A
Maximum power point voltage (Vm)	29.81V
Maximum power point current (Im)	7.72A
Maximum Power (Pm)	230.13W

D. MAXIMUM POWER POINT TRACKING

The P&O algorithm is employed to analyse and extract the maximum power from the photovoltaic (PV) system. In this algorithm, the operating voltage of the PV array is adjusted by a small increment, and the resulting change in power (ΔP) is recorded. If ΔP is positive, it indicates that the perturbation of the operating voltage has shifted the PV array's operating point closer to the maximum power point (MPP). Consequently, additional voltage perturbations in the same direction (i.e., with the same algebraic sign) should further advance the operating point toward the MPP. Conversely, if ΔP is negative, it signifies that the system's operating point has deviated from the MPP, necessitating a reversal of the algebraic sign of the perturbation to return to the MPP. The P&O algorithm is advantageous due to its simplicity and ease of implementation. The P&O maximum power point tracking (MPPT) algorithm, illustrated in Figure 13, has been executed in MATLAB to optimize the power extraction from the solar PV module.

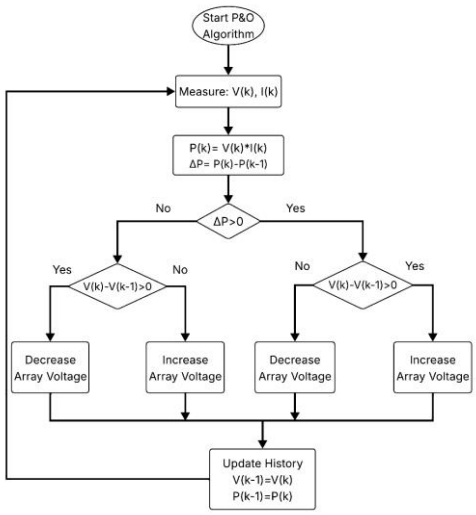

Figure 13: Flowchart for P&O algorithm of MPPT

If ΔP/ΔV > 0, ΔD is +ve (9)

If ΔP/ΔV < 0, ΔD is –ve (10)

E. Implementation of Fuzzy Controller

Fuzzy logic control is an effective technique for regulating complex and nonlinear systems in which accurate mathematical models are difficult to obtain. In power electronic applications, fuzzy controllers efficiently handle system uncertainties and parameter variations using linguistic rules rather than precise numerical equations. A fuzzy logic controller (FLC) is based on fuzzy set theory, where variables are represented by degrees of membership instead of binary values. The basic structure of the FLC consists of three main stages: fuzzification, fuzzy rule inference, and defuzzification.

In the fuzzification stage, numerical input variables such as error and rate of change of error are converted into linguistic variables using predefined membership functions. Triangular and trapezoidal membership functions are commonly adopted due to their simplicity and computational efficiency. In this work, seven membership functions are used for both input variables, while four membership functions are assigned to the output. The fuzzy inference mechanism employs the Mamdani method, which uses a set of expert-defined IF–THEN rules to determine the control action. Finally, the defuzzification stage converts the fuzzy output into a crisp control signal using the

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centroid method, ensuring smooth and accurate control of the PV-fed multilevel inverter system.

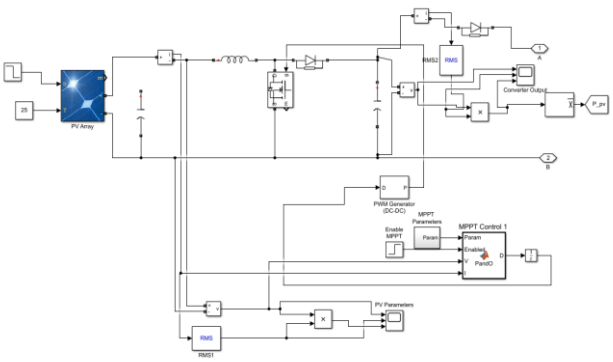
Table III presents the fuzzy rule base used to determine the duty ratio for PV control based on the voltage error. The rules are designed to maintain stable operation by assigning zero duty variation for negative and zero errors, while progressively increasing the duty ratio for positive voltage errors to ensure effective MPPT and voltage regulation.

TABLE III: Rules table for the fuzzy control for PV

VE/CE	DUTY RATIO
NEGATIVE VERY LARGE	ZERO
NEGATIVE LARGE	ZERO
NEGATIVE MEDIUM	ZERO
NEGATIVE SMALL	ZERO
ZERO	ZERO
POSITIVE SMALL	POSITIVE MEDIUM
POSITIVE MEDIUM	POSITIVE LARGE
POSITIVE LARGE	POSITIVE LARGE
POSITIVE VERY LARGE	POSITIVE LARGE

III. SIMULATION RESULTS

The simulation model under consideration is executed in MATLAB/Simulink, utilizing the Simscape Electrical toolbox. As shown in Figure 14, solar photovoltaic (PV) block is designed to function as the DC source and is linked to the power conversion stage. The simulation operates in discrete mode, facilitated by the powergui block, with a sampling interval of 1e-6 seconds. Voltage and current measurement blocks are incorporated at the output of the PV, while RMS blocks are employed to calculate effective values for performance evaluation. These signals undergo processing through mathematical and control blocks to produce reference signals. The multilevel inverter (MLI) subsystem is constructed using controlled switches and is connected to the load via measurement ports. Appropriate gating pulses are applied to the inverter switches to achieve the desired multilevel output waveform, and scopes are utilized to monitor voltage and current responses.



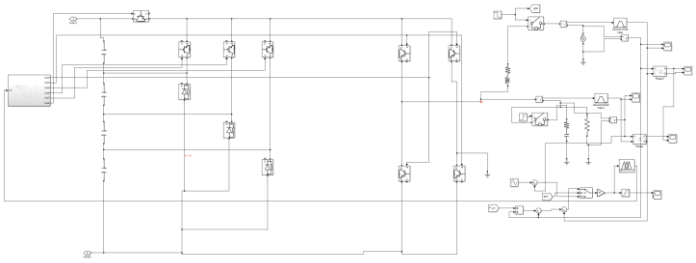


Figure 14. Simulation Circuit for the Proposed Inverter

The photovoltaic (PV) source generates power in accordance with the irradiation level, which is initially 1000W/m2 and decreases to 600W/m2 at t=0.5s. The boost converter increases the voltage based on the maximum power point tracking (MPPT) control. The output from the boost converter is fed into the multilevel inverter, which comprises eight power electronic switches, four capacitors, and a load of 20Ω. The grid is disconnected at t=1s, and an additional load of 20Ω is connected at t=1.5s.

At a solar irradiation level of 1000 W/m², the photovoltaic (PV) array produces a current of roughly 50 A and a voltage of approximately 230 V, leading to an output power of nearly 11.52 kW. When the solar irradiation diminishes to 600 W/m², the available power from the PV system decreases considerably due to the reduced solar energy incident on the array, resulting in an output power of about 6.3 kW. This decline clearly illustrates the direct relationship between PV output power and solar irradiation, as the operating voltage remains nearly stable while the current decreases with the reduction in irradiation.

The PV voltage, current and power is provided below in Figure 15:

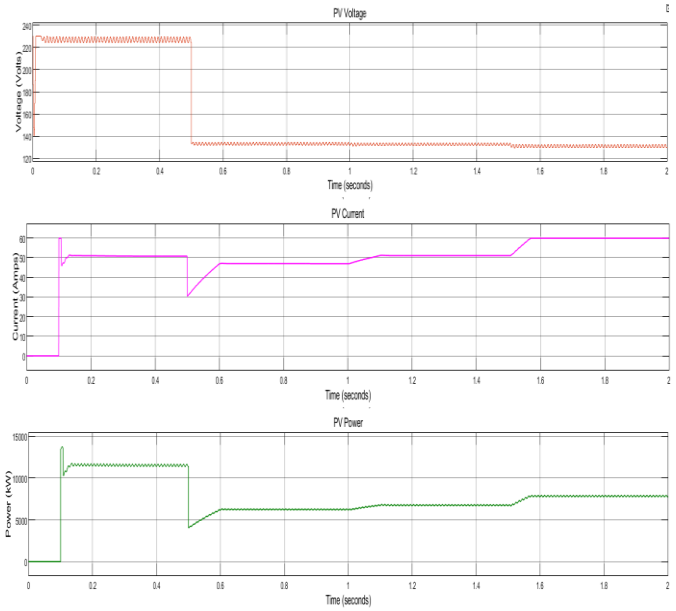


Figure 15: PV Voltage, Current, and Power Response under Irradiance Variation

The voltage waveform of the load fluctuates between +230V and −230V, demonstrating symmetrical functioning during both the positive and negative half cycles. Each voltage

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increment has an approximate magnitude of 60 V, facilitating the creation of several discrete voltage levels. During the positive half cycle, four unique positive voltage levels are generated, whereas in the negative half cycle, four corresponding negative voltage levels are produced as illustrated in Figure 16. Moreover, a zero-voltage state is incorporated at the midpoint of the waveform.

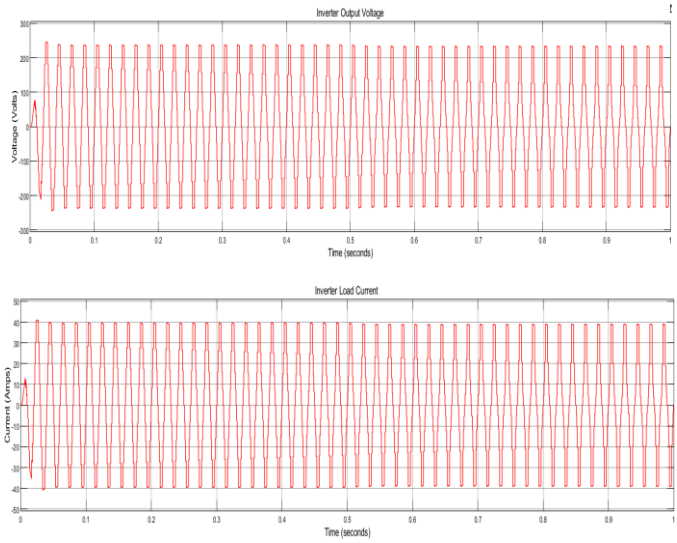

Figure 16: Inverter Output Voltage and Load Current Waveform

The inverter provides an output power of roughly 11.5 kW when operating in a standard grid-connected mode. Under these circumstances, the grid contributes approximately 2.4 kW of power until t = 1s, which signifies a collaborative power distribution between the inverter and the utility grid. At t = 1 s, the grid is severed, prompting the system to shift into islanded mode, wherein the inverter independently caters to the load. Throughout this phase, the inverter's power stabilizes at about 5 kW to satisfy the local load requirements. When the load demand escalates at t = 1.5s, the inverter swiftly adjusts by raising its output power to around 6 kW as shown in Figure 17, thereby showcasing its proficient load tracking ability and maintaining stable performance amidst fluctuating load conditions.

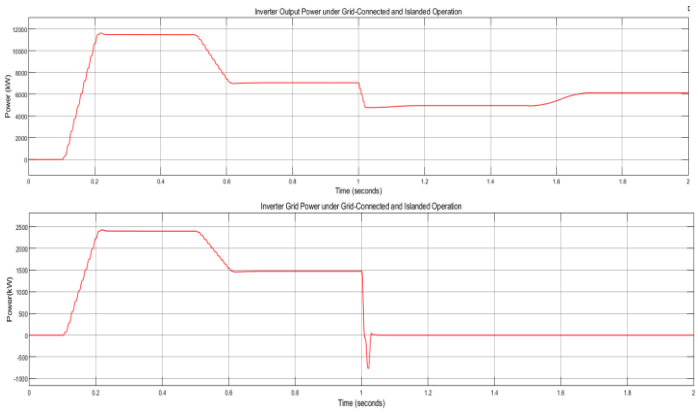

Figure 17: Inverter Output Power and Grid Power under Grid-Connected and Islanded Operation

The grid current typically measures around 10 A during standard functioning under conditions of elevated solar irradiation. As the level of solar irradiation diminishes, the power generated by the photovoltaic (PV) system decreases, resulting in a reduction of the grid current to approximately 6 A as shown in Figure 18. At the moment the grid is disconnected, the grid current reduces to zero, signifying a successful shift to islanded operation and the total separation of the inverter from the utility grid.

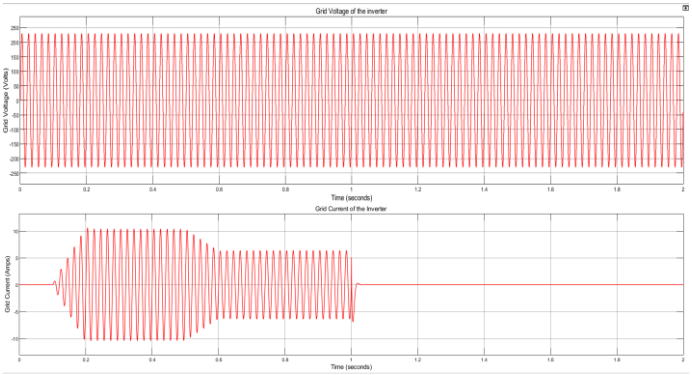

Figure 18: Grid Voltage and Grid Current Waveforms of the Proposed Inverter

The total harmonic distortion (THD) of the load current is around 0.22% as shown in Figure 19, signifying a high-quality sinusoidal current waveform. Such a low THD value validates the efficient multilevel functioning of the inverter and an appropriate control strategy, thereby ensuring adherence to power quality standards and minimal harmonic injection into both the load and the grid.

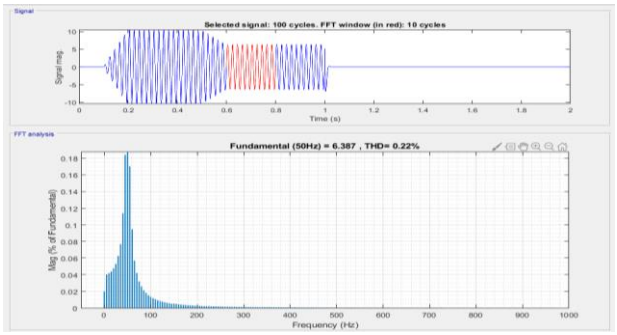

Figure 19: FFT Analysis of Load Current Showing Harmonic Spectrum and THD

IV. CONCLUSION

This paper presented a photovoltaic-fed nine-level switched-capacitor multilevel inverter with a reduced switch count for home-grid integration and electric vehicle charging applications. The proposed topology generates nine voltage levels using only eight power switches, four capacitors, and three diodes, leading to reduced hardware complexity, lower switching losses, and decreased voltage stress compared to conventional multilevel inverters. The inverter was operated with a rated power of approximately 11.5 kW in grid-connected mode, while the grid supplied about 2.4 kW before disconnection, demonstrating effective power sharing. Upon

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grid isolation, the inverter independently supplied around 5 kW to the load, confirming reliable islanded operation.

A boost converter with P&O-based MPPT ensured maximum power extraction from the PV array under varying irradiation, and a fuzzy logic–based control scheme provided smooth grid synchronization and stable voltage regulation. MATLAB/Simulink results show that the proposed inverter achieves excellent output power quality with a load current total harmonic distortion of approximately 0.22%, well within IEEE standards. These results validate the suitability of the proposed inverter for efficient, high-quality residential PV and EV charging systems.

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