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A Proficient Design of Adaptive Modulation Scheme Supportive Address Generator for WiMAX Deinterleaver Precinct

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***Abstract*— Transmission errors gets induced into the information when communication takes place between transmitter and receiver through wireless channel. These errors can be corrected and its effects can be reduced by using the interleaving technique along with the forward error correction method. Deinterleaver has to be used for retrieving the error induced information correctly at the receiver. Address generator plays a vital role in deciding the overall performance of the deinterleaver. This work proposes a new novel algorithm for the address generating circuitry for WiMAX deinterleaver supporting adaptive modulation schemes. The FPGA implementation for the deinterleaver block is being hindered due to the presence of floor function in the deinterleaving permutations. In this paper the deinterleaver addresses are produced based on a new algorithm which can logically generate the deinterleaver addresses without using the floor functions. The FPGA parameter analysis is carried in Xilinx 14.6 ISE for Spartan 3e device for having a device utilization comparison of the proposed new algorithm with a recent existing design.**

Keywords*— Address Generator, Deinterleaver, Forward error correction, VHDL, WiMAX

I. INTRODUCTION

WiMAX (Worldwide Interoperability for Microwave Access) is a latest technology which can revolutionize the existing last mile or wired technology. WiMAX can be broadly classified into two namely fixed WiMAX (IEEE 802.16-2004) and mobile WiMAX (IEEE 802.16e-2005) respectively. In this work, address generator of deinterleaver for mobile WiMAX has been considered. Presently WiMAX is used as a broadband wireless access technology [1]. When communication is being established between base station (BS) and the subscriber station (SS) via the wireless channel different kinds of transmission errors gets induced into the transmitted information due to channel characteristics.

Channel can induce transmission errors such as random errors and burst errors due the fading, interference, scattering etc. Errors can be detected and corrected by using error correcting codes. Amongst random and burst errors, burst errors are difficult to detect and combat due to their bursty nature. The most simplest and effective method for combating transmission error is by using interleaving method in conjunction with FEC. If we are using interleaving technique at the transmitter side we have to use deinterleaving technique at the receiver side to recreate the original transmitted information.

WiMAX uses different modulation schemes as per the IEEE standards. It uses QPSK, 16-QAM and 64-QAM modulation schemes, the deinterleaver has to produce the deinterleaver addresses in an adaptive nature. Deinterleaver addresses are produced by the address generator based upon two level permutation, which consists of floor function thus making its FPGA implementation difficult. In order to optimize the performance of deinterleaver we have to optimize the address generator which can support adaptive modulation scheme and coding schemes [4].

The mobile WiMAX can support more than thousand mobile users and can replace the existing wired system. It can offer a data rate of 54-70 Mbps within a range of 30-50 km with the help of varying modulation schemes and OFDMA (Orthogonal Frequency Division Multiple Access) technique [5], [8].

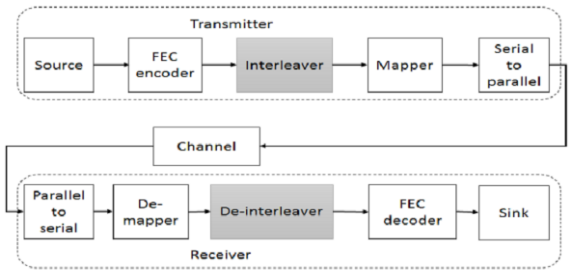

Fig.1. Block diagram of WiMAX transceiver

When transmitter transmits information via wireless channel to the receiver (Figure 1) source produces the information which is then encoded using FEC and interleaved for obtaining the time diversity and immunity to slow flat fading effects. The interleaved information is then mapped into different modulation schemes as per mobile WiMAX specifications and the mapped information is transmitted using OFDMA. At the receiver side the inverse operation takes place in the reverse order. The received error induced information is down converted, de-mapped based on different modulation schemes and is deinterleaved. The address generator in deinterleaver has to produce the deinterleaver addresses as per the different modulation schemes in an adaptive manner [3], [7]. In this paper a novel deinterleaver address generating algorithm is being proposed.

This paper is divided into four sections, first section provides a brief introduction of mobile WiMAX and explains the technical background of deinterleaver and the address generator; second section explains the proposed new algorithm of address generator; third section highlights the results and comparison of new algorithm with a recent work. Section four concludes the paper by making remarks on the contributions and results achieved by the new algorithm

II. THE PROPOSED PRECINCT

The motivation for creating new algorithm was due to the drawbacks of a recent work. The recent work used correlation based approach [1] rather than the conventional look up table (LUTs) approach [2]. The correlation based method computed the addresses instead of storing all the addresses like the look up table approach. Amongst two methods correlation based method was efficient in terms of FPGA device utilization. But, the correlation based method used complex mathematical computations thus making it less resource efficient which made us devise a new algorithm.

$$m_k = \left(\frac{N_{cbps}}{d}\right) * (k\%d) + \left\lfloor \frac{k}{d} \right\rfloor \quad (1)$$

$$j_k = s * \left\lfloor \frac{m_k}{s} \right\rfloor + \left(m_k + N_{cbps} - \left\lfloor \frac{d * m_k}{N_{cbps}} \right\rfloor \right) \% s \quad (2)$$

Using Equations (1) and (2) the interleaving computations of WiMAX system is carried out. ⌊ ⌋ denotes the floor function which hinders the FPGA implementation and optimization. ‘s’ can take the values 1, 2 or 3 for selecting different modulation schemes, ‘j’ denotes the number of column, ‘d’ denotes the number of rows, N_{cbps} denotes the number of coded bits per symbol and N_{cpc} denotes the number of coded bits per subcarrier [8], [9].

$$m_j = s * \left\lfloor \frac{j}{s} \right\rfloor + \left(j + \left\lfloor \frac{d * j}{N_{cbps}} \right\rfloor \right) \% s \quad (3)$$

$$k_j = d * m_j - (N_{cbps} - 1) * \left\lfloor \frac{d * m_j}{N_{cbps}} \right\rfloor \quad (4)$$

‘s’ is the parameter which is defined by $N_{cpc}/2$ and it takes the value 1, 2 or 3 for QPSK, 16-QAM and 64-QAM respectively. Equations (3) and (4) does the inverse operation of interleaving and it takes place at the receiver side [1].

Table 1: Permitted interleaver/deinterleaver depths as per IEEE standard

Interleaver depth (N_{cbps})	Modulation Schemes with allowed code rates						
	QPSK		16-QAM		64-QAM		
	1/2	3/4	1/2	3/4	1/2	2/3	3/4
	96	144	192	288	288	384	432
	192	288	384	576	576	-	-
	288	432	576	-	-	-	-
	384	576					
	480	-	-	-	-	-	-
	576	-	-	-	-	-	-

The floor function is an approximation function so we have to store all the values in memory modules or look up tables (LUTs) to perform the operation of deinterleaver address generator thus, the FPGA device utilization is high and the design is not optimized. We have to create a new method to optimize the address generator unit which can produce deinterleaver address without using complex floor fuction. This work only concentrates on address generator of deinterleaver thus equations (3) and (4) are of interest. By constraining equations (3) and (4) using MATLAB the deinterleaver addresses are obtained based upon table 1.

Table 1 shows the different code rates and interleaver depths for the different modulation schemes as per IEEE standard [6]. The value of j is varied from 0 to (N_{cbps}/d)-1 and i is varied from 0 to d-1. The value of d can be 16 or 12. N_{cbps} takes value from table 1 [1], [6]. The new algorithm produces deinterleaver addresses based on simple mathematical computation rather than storing the deinterleaver addresses like in the conventional methods.

Table 2: Deinterleaver addresses obtained for different modulation schemes

Modulation type	Deinterleaver address					
QPSK scheme	0	16	32	48	64	80
	1	17	33	49	65	81
	2	18	34	50	66	82
	3	19	35	51	67	83
16-QAM scheme	0	16	32	48	64	80
	17	1	49	33	81	65
	2	18	34	50	66	82
	19	3	51	35	83	67
64-QAM scheme	0	16	32	48	64	80
	17	33	1	65	81	49
	34	2	18	82	50	66
	3	19	35	51	67	83

Table 2 shows the deinterleaver addresses obtained based upon equations (3) and (4) using MATLAB. From close observation the deinterleaver addresses can be obtained by using simple arithmetic operations. The design proposed in this paper produces deinterleaver addresses for IEEE 802.16e (mobile WiMAX) using incrementing and decrementing operations for each modulation schemes and its respective code rates. Thus making the deinterleaver address generator adaptive.

The algorithm is applicable for all the modulation schemes and it doesn’t store the addresses but computes deinterleaver addresses based upon the present deinterleaver addresses. The values which are used to compute the new deinterleaver addresses are known as master mode as per the new proposed algorithm. Table 2 is tabulated for d=16 using MATLAB.

When base station establishes connection with a close subscriber station initially it produces the deinterleaver addresses for QPSK and as the distance increases the 16-QAM deinterleaver addresses are produced and then finally 64-QAM deinterleaver addresses are produced. When the subscriber station comes closer to the base station the

deinterleaver addresses for 64-QAM, 16-QAM and QPSK are produced respectively. The deinterleaver addresses are to be produced in the same manner as depicted in table 2. The new proposed algorithm works based on the flow chart (Figure 2) which briefs the different steps involved in producing the deinterleaver addresses. The row and column values are initialized and then master mode values are computed which is used to obtain the next deinterleaver address from present deinterleaver address.

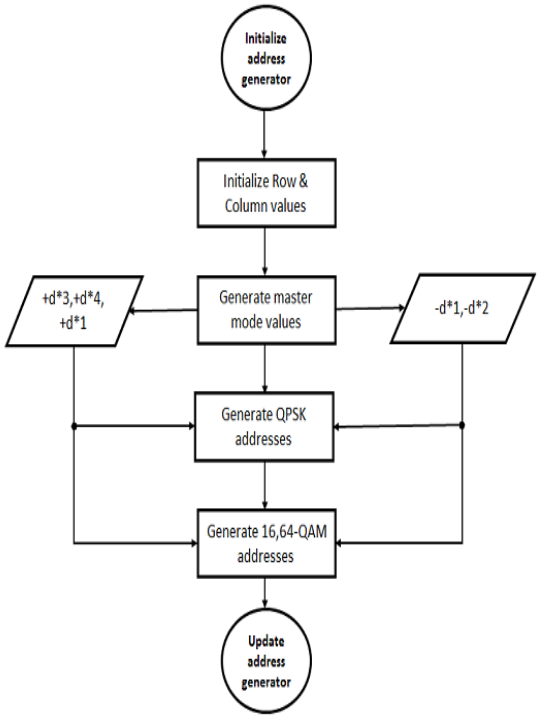

Fig.2. Flowchart for the proposed new algorithm

The master mode values are generated based upon the new proposed algorithm. Work by B K Upadhyaya [1] used correlation method for obtaining QPSK and 16-QAM deinterleaver addresses but 64-QAM addresses were stored in look up tables like the conventional method making it less resource efficient. In this work, all the deinterleaver addresses for all the modulation schemes are generated rather than storing and retrieving them making the design more resource efficient than prevailing designs. Hardware models for all the modulations schemes were developed which is depicted in Figure 3 and Figure 4 and Figure 5 shows the top-level model of the new algorithm.

The hardware model for the 64-QAM scheme (Figure 4) shows the various arithmetic units which are used to generate deinterleaver address on the signal kn. Master mode has got the functionality of the algorithm. Using the signal code rate different column values are selected. The column value 'i' varies from 0 to (N_{cbps}/d)-1 and row value 'j' varies from 0 to d-1. The value of d is selected as 16 for IEEE 802.16e.

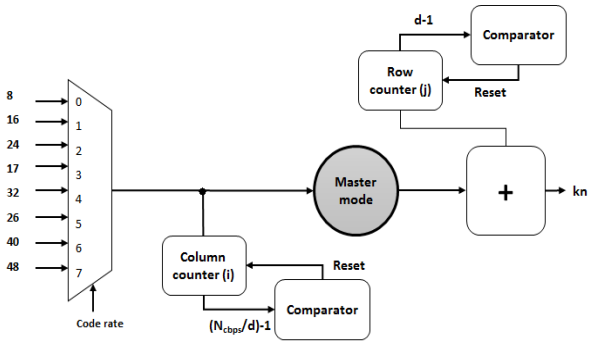

Fig.3. Hardware model for the QPSK scheme

Figure 3 shows the hardware model for the QPSK scheme. The deinterleaver addresses are produced on the signal kn. The master mode embedded with the new proposed algorithm which controls the generation of deinterleaver addresses as per adaptive modulation and coding schemes.

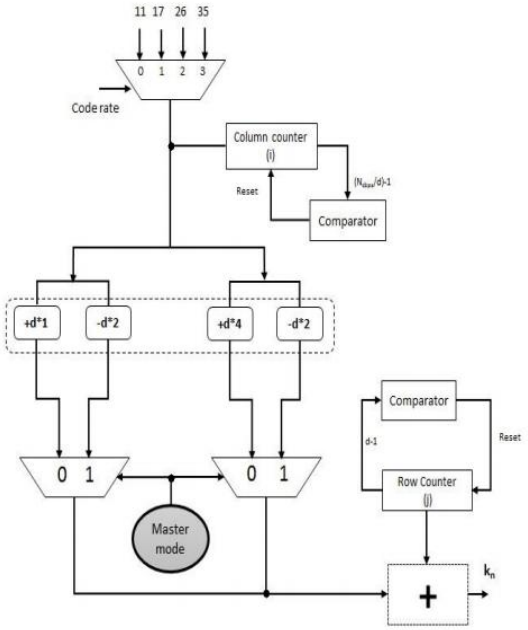

Fig.4. Hardware model for the 64-QAM scheme

The mathematical computation of master mode is given in [10],[11]. Using the mathematical computation on the variable 'd' the deinterleaver addresses can be generated unlike the conventional method of storing and retrieving the addresses in LUTs. The addresses generation was possible due to the new algorithms ability to eliminate the use of floor function.

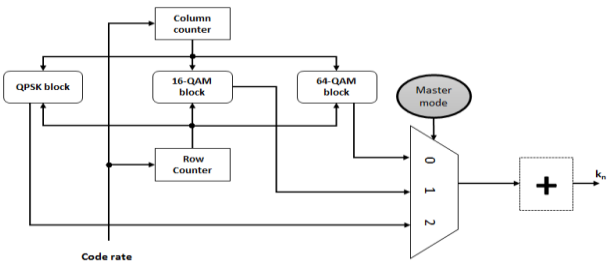

Fig.5. Hardware replica of top-level mode

In the top level model (Figure 5) master mode is used to select different modulation schemes and code rate is used to initialize the row and column values respectively. The signal kn produces the different updated deinterleaver addresses as per the selected modulation scheme. Using the present deinterleaver address the next deinterleaver address are generated using incrementing and decrementing values.

III. RESULTS AND DISCUSSIONS

The mobile WiMAX can be deployed in disaster hit areas to establish communication links with ease. The deinterleaver is used to overcome and reduce different kinds of transmission errors which occurs when transmission of information takes place through wireless channel [7], [12].

Simulation of the proposed new algorithm is done using ModelSim 6.2b to check the values on signal kn, as expected the values on signal kn was same as that produced by MATLAB using equations (3) and (4). The hardware was modelled using HDL and FPGA device utilization was compared with the prevailing designs.

The new proposed precinct showed significant reduction in FPGA device utilization. The deinterleaver address generator for 64-QAM modulation scheme showed significant reduction than the existing designs since the new algorithm used the methodology of logical generation of the addresses rather than storing and retrieving it.

The proposed new algorithm and existing design was synthesized in Xilinx 14.6 ISE in Spartan 3e device.

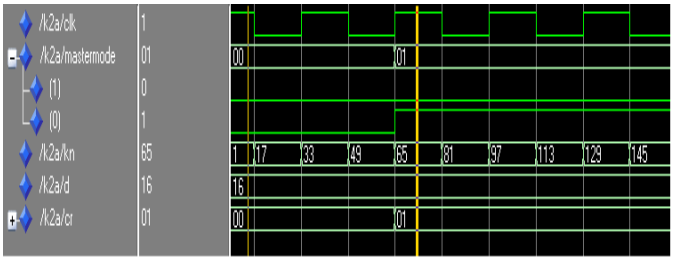

Fig.6. Simulated Waveform of the proposed design

Figure 6 shows the simulated waveform of the top level hardware model. The values on kn are generated based on the cr and mastermode inputs.

The cr provides the different code rates and mastermode selects different modulation schemes. Cursor in Figure 6 shows the transitions of different modulation schemes namely from QPSK to 16-QAM. Table 3 shows the FPGA device utilization summary of the proposed new algorithm with the existing design. The new algorithm generates the mobile WiMAX deinterleaver addresses in a proficient and adaptive manner. The new deinterleaver can be used in mobile WiMAX system to speed up the overall performance of the transceiver.

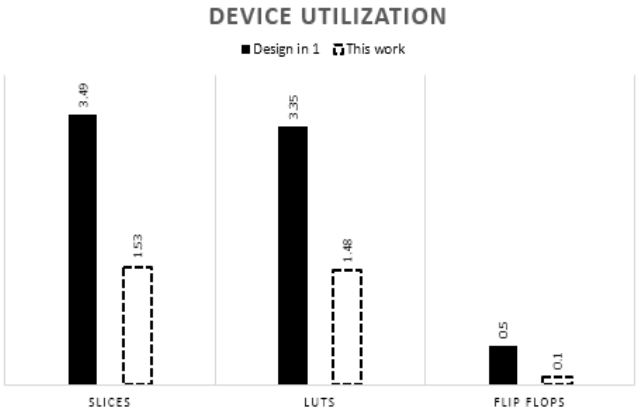

Fig.7. FPGA Device parameter Comparison

Figure 7 shows the FPGA device parameter comparison between the existing design and proposed designs respectively.

Table 3: FPGA Device utilization comparison of proposed and existing design

FPGA Parameters	Correlation Based design [1]	New Algorithm [this work]
Slices	3.49 %	1.53 %
Flip Flops	0.50 %	0.10 %
4 input LUT	3.35 %	1.48 %
Operating frequency	121. 82 MHz	148. 68 MHz

IV. CONCLUSION

The address generator plays a decisive role in deciding the overall performance of the WiMAX deinterleaver. Complexity of address generator is due to the presence of floor function in the computation of deinterleaver addresses which hinders the FPGA performance.

This work concentrated on optimizing the deinterleaver address generator for WiMAX. The new algorithm was found to be outperforming the recent existing design in terms of FPGA device parameters. The deinterleaver addresses were computed using MATLAB for authenticity with the help of two permutations as specified by the standards. The new algorithm was modelled using VHDL and simulated in Mentor Graphics ModelSim 6.2b. The existing design and the proposed new algorithm was synthesised in Spartan 3e device in Xilinx 14.6 ISE, as expected the new algorithm was found to be more efficient than the existing design. It showed a significant reduction in terms of FPGA device utilization and a significant improvement in terms operating frequency in contrast to the existing design. The new algorithm clocked a maximum operating frequency of 148.68 MHz in Spartan 3e device.

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