A Power Factor Correction based on Canonical Switching Cell Converter for VSI Fed BLDC Motor by using Voltage Follower Technique

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Abstract— This paper describes about a power factor correction based canonical switching cell converter for VSI fed BLDC motor by using voltage follower technique .In this paper (BLCSC) Bridge Less Canonical Switching Cell Converter runs in a discontinuous inductor current mode . Due to this near unity power factor is obtained .The DC link voltage at the front end of VSI fed BLDC motor is changed to control the speed of the motor with the help of PFC converter. From the above action, VSI which works in a fundamental frequency switching when it is electronically commutated , minimizes the switching losses. Conduction losses are also reduced by eliminating the DBR circuit in CSC configuration in existing system. The proposed configuration shows a considerable increase in the performance as compared with the conventional scheme. The execution of a proposed drive is certified through the observed results from the modified model simulated using PROTEUS . The power quality is improved at the AC mains for a substantial range of speed and supply voltage in concern.

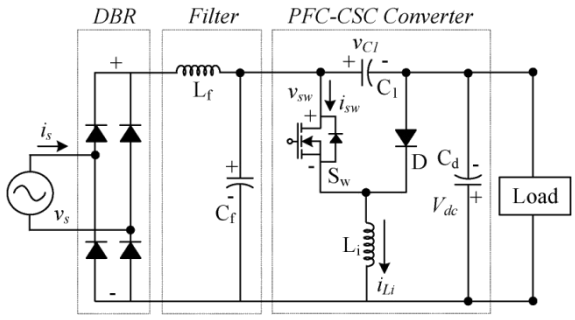
Keyword- VSI – Voltage source Inverter, BLDC – Brush Less DC motor, BLCSC –Bridge Less Canonical Switching Cell converter, PFC-Power Factor Correction, DBR-Diode Bridge Rectifier, power quality.

I INTRODUCTION

Brushless DC motor drives have acquired importance in the recent ten years due to development in power quality that have resulted in unmatched performance compared with existing drives(1). Some of the reasons made this motor more famous in industries. That reasons are as follows: high reliability, high performance, high ruggedness, reduced electromagnetic interference problems, and exceptional performance over a extensive range of speed control (2,3).This machine is more applicable for many low power and medium power applications such as position actuators , ventilation, household appliances, air conditioning and heating, medical equipment , motion control and transportation(4-7). It is a synchronous motor having permanent magnet mounted on the rotor and three phase winding on the stator. Hall sensors are used to remove the tribulations related with the existing DC motors. The problems removed by the sensor are EMI, sparking noise, maintenance problem etc.,(8). The higher value of DC link capacitor fed VSI based BLDC motor follows the diode bridge rectifier to drag high current from a supply and insert a large amount of harmonics in the supply system(9). As a effect of this operation the power factor value is poor(even lower than 0.7) and large total distortion (THD) of supply current (even as more as 65%) at the AC mains. This type of power quality standard is not permissible by Inter National power quality standard IEC 61000-3-2. For this reason power quality at the AC mains were improved by using power factor correction converters. In the collection many forms of single –stage power conversion techniques with or without isolation have been sighted. These converter circuits have smaller amount of devices and thus have low losses linked with them . The expenditure of these converter design become an imperative parameter which is first based on the quantity of sensing requirement and the type of operation of the PFC converter. The choice of working mode is a transaction between the price and tolerable stress on the switch because a current multiplier approach is used for the PFC converter working in continuous conduction operating mode(CCM) which results in little stress on the switch but it required more than a sensor whereas one potential sensor is required for the PFC converter`s switch. So that the option of interchange working mode is a exchange between the cost and the allowable stress on the switch. A CSC converter based BLDC motor drive with PFC configurations have been reported in the literature. Ozturk et al. [13] and Wu and Tzou [14] have proposed a conventional boost PFC converter for feeding BLDC motor drive**.** The constant dc link voltage and PWM based control of BLDC motor is used. It is affected from high switching losses in six solid state switches of the VSI due to the higher switching frequency of PWM pulses.(15) Cheng has proposed a three phase VSI fed BLDC motor drive, with active rectifier required a difficult control and it is suitable for higher power applications. During the speed control of BLDC motor switching losses are reduced by using a perception of variable DC link voltage. In general BLDC motor electronic commutation requires low frequency switching VSI ,the circuit uses the same principle to decrease the

switching losses. A variable voltage control is fed by the(SEPIC) single-ended primary-inductor converter in the front end of the BLDC motor. These are proposed in (18).This paper explains about the improvement of a reduced sensor based BLDC motor drive for low power applications. In the last ten years, Due to the low conduction losses it has more profit at the front end(20-30).The bridge less buck and boost converter is used for limited voltage conversion so it cannot be used for wide range of voltage control. To avoid this problem a bridge less buck and boost converters has been proposed in (23 and 24) but 23 has some more switching losses corresponding to 3 switches compared with (24).Likewise many components are used with high order PFC bridge. The advantage of using canonical switching cell converter are good performance, pre regulator power factor, good light load condition and small component count(31-34). Fig.1. Shows Conventional PFC based CSC converter. Canonical switching cell converter circuit contains the combinations of switch (S_w), diode (D), capacitor(C_1). This cell combines with the inductor (L_i) and DC link capacitor (C_d). This is known as Canonical switching cell converter. By making the circuit in a proper way that is with selected parameters PFC correction will be achieved when it is fed by a single phase supply through DBR and DC filter .The aim of this paper is to offer a reduced conduction loss by removing the DBR and also used to develop a low cost solution to low power application.

Fig.1. Conventional PFC based CSC converter



II. PFC BASED BRIDGE LESS -CSC CONVERTER- FED BLDC MOTOR DRIVE:

Fig. 2 explains about BL-CSC converter for VSI fed brush less DC motor drive. In this converter diode bridge rectifier is neglected .So that conduction losses gets reduced .This converter works in a discontinuous inductor current operating mode(DICM). Inductor currents (L_{i1}, L_{i2}) are broken. Although voltage across intermediary capacitors (C_1, C_2) are continuous in a switching period. A changeable DC link voltage is used to control the speed of the BLDC motor are shown below. Switching losses are decreased in VSI ,when it is electronically commutated .The execution of projected drive is compared with the test results received from a planned model with improved power quality for the ac mains for a vast range of speed and supply voltages. The comparison of projected configuration and conventional configurations of converter is summarized and tabulated as table I. It displays the not only the total number of components but also the conducting components at every half cycle of supply voltage. The boost and buck converter schemes are not applicable for necessary application .Due to this high voltage exchange ratio, it is used for speed control of the BLDC motor over a wide range. When compared to other BL configurations of SEPIC, CUK AND ZETA converters, and BLCSC converters has less components and less number of power electronic devices at every half cycle. When supply voltage is given. The proposed model shows fewer amounts of conduction losses owing to the usage of conducting devices at half line cycle.

A. Working Principle Of The PFC Based Bridge Less - CSC Converter

The working of the BL-CSC converter is divided into two key categories.

A Working in Positive and Negative Half Cycles of Input AC Supply:

When supply voltage is applied to the bridge less converter, for each positive and negative half cycles one switch will conduct. Fig. 3a–f explains about the working of the projected model for each positive and negative half cycles. Input current flows through diode D_p, inductor L_i, and switch S_{w1} during the positive half cycle as shown in 3a-c.Equivalently switch S_{w2}, diode D_n and inductor L_{i2} are operate for a negative half cycle as shown in the figure 3d-f.Fig. 4a explains about the waveforms of input AC voltage with inductor current (i_{Li1} and i_{Li2}) and midway capacitor voltages (V_{C1} and V_{C2}). The projected model is working in discontinuous inductor current mode. Due to this inductor currents are discontinuous and voltage across the capacitor is continuous during switching period.

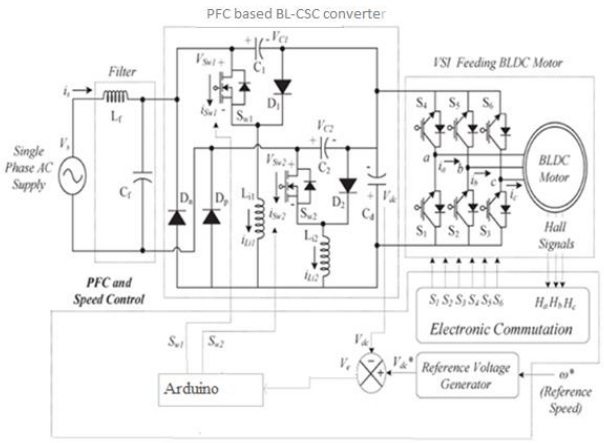


TABLE-I COMPARISION OF PROPOSED BRIDGE LESS CSC CONVERVERTER WITH OTHER RELEVANT CONFIGURATIONS.

Configuration	No. of Devices					½ Period Cond.
	S_w	D	L	C	Total	
BL-Buck [20]	2	4	2	2	10	5
BL-Boost [21]	2	2	1	1	6	4
BL-Boost [22]	2	2	1	2	7	7
BL-Buck-Boost [23]	3	4	1	3	11	8
BL-Buck-Boost [24]	2	4	2	1	9	5
BL-Cuk T-1 [25]	2	3	3	3	11	7
BL-Cuk T-2 [25]	2	2	3	4	11	11
BL-Cuk T-3 [25, 26]	2	4	4	3	13	7
BL-Cuk [27]	2	3	3	2	10	8
BL-SEPIC [28]	2	3	1	3	9	7
BL-SEPIC [29]	2	3	2	2	9	7
BL-Zeta [30]	2	4	4	3	13	7
Proposed BL-CSC	2	4	2	3	11	6

B. Operation during Complete Switching Period:

The proposed brush less canonical switching cell converter is constructed to work in DICM.Fig. 3(a-f) tells about the working of different modes of operation for every half cycles of the input AC voltage , Fig 4b shows the linked waveforms during all the three modes of working .

MODE 1 (A): During first mode(A) switch S_{w1} is in ON condition ,inductor L_{i1} begins charging in the input side through diode D_p and current i_{L1} increases , whereas intermediate capacitor C_1 begins discharging through switch S_{w1} to charge C_d. From this operation V_{c1} decrease and V_{dc} increase. Fig 3a.

MODE I-B:

During mode B switch S_{w1} is in OFF condition .If S_{w1} is OFF then inductor L_{i1} discharges to DC link capacitor through diode D_1 (Fig 3b). Owing to this the current i_{L1} decreased. The voltage across the DC link increases continuously during this mode of operation .The capacitor C_1 starts charging which increases the voltage V_{c1} (Fig 4b).

MODE I-C:

During discontinuous mode of operation the current which flows all the way through the inductor L_{i1}, becomes zero (Fig 3c). The capacitor C_d delivers the necessary demand of the load. At the same time capacitor C_1 holding the energy continuously to retain its energy . The equivalent operation of converter is observed for other negative half cycle of the input, whereas inductor(L_{i2}) ,capacitor(C_2) and diodes(D_1 and D_2) conducts in the same way. Fig 3d-f.

III. DESIGN OF THE PFC BASED BRIDGE LESS-CSC CONVERTER:

The projected PFC converter is modeled to work in Discontinuous ICM . So that, the inductorcurrent iL_{i1} and $iL_{i2}$are discontinuous and the capacitor C_1 and C_2 voltage are continuous during switching operation. For experimental studies 424-W BLDC motor is used the input side converter of 500W (P_{max}) is considered to supply a BLDC motor drive .The speed can be varied widely from low value corresponding to 70V ($V_{dc\ min}$) to the the maximum voltage of 310 V($V_{dc\ max}$) by using DC link voltage control.

The input voltage can be given by ,

$V_s(t)=V_m Sin(\omega t)=220(\sqrt{2})$ x Sin (314t) (1)

Where $V_m \rightarrow$ maximum input voltage, (ie.,$\sqrt{2}\ V_s$)

The value of voltage which appears across the inductor combination and any of the switches are given as

$V_{in}(t) = |V_m \sin(2\pi ft)| = |220(\sqrt{2}) x \sin(314t)|$ (2)

The voltage output V_{dc} of the CSC converter is given as (9)

$$V_{DC} = \frac{\alpha}{1-\alpha} V_{in} \quad (3)$$

$\alpha \rightarrow$Duty ratio

The value of $\alpha(t)$ based onvoltage input $V_{in}(t)$ and the desired voltage of DC link V_{DC}. The instantaneous duty cycle$\alpha(t)$ is acquired by substituting equations 2 and 3 as follows,

$$\alpha(t) = \frac{V_{dc}}{V(t)+V_{dc}} = \frac{V_{dc}}{|V_m \sin(\omega t)|+V_{dc}} \quad (4)$$

If the voltage across the DC link is changed then the speed of the drive will be varied, therefore the P_i is noted as linear function of V_{dc} as

$$P_i = \frac{P_{max}}{V_{dcmax}}(V_{dc}) \quad (5)$$

Where V_{dc} is the dc link voltage .

$P_{max} \rightarrow$rated power for the PFC converter

With the help of equation (5) the minimum power is calculated as 113V (P_{min}) corresponding to minimum DC link voltage of 70V ($V_{dc\ min}$).

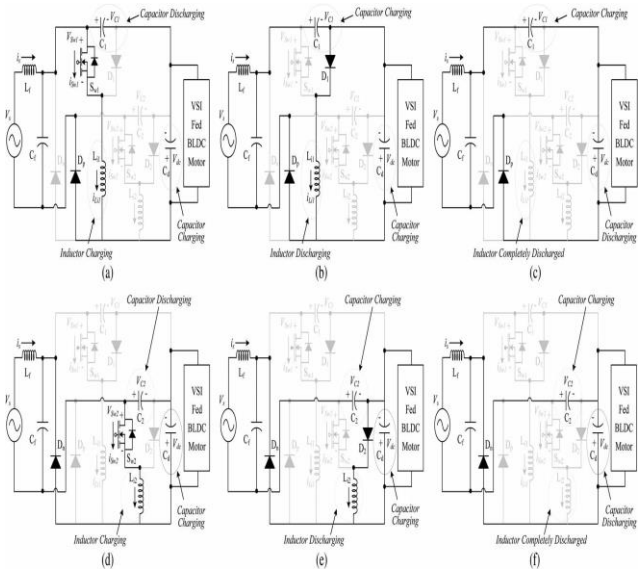


Fig. 3.Various modes of working of the projected Bridge Less-CSC converter. a: Mode I(A), b: Mode I(B), c: Mode I(C), d: Mode II(A), e: Mode II(B), f: Mode II(C)

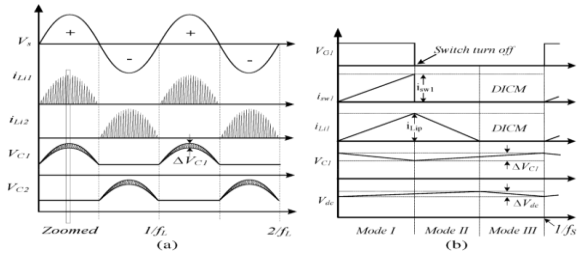


Fig. 4. Wave forms for various modes of working of the projected converter.

A. Design of input inductors (L_{i1} and L_{i2}) in discontinuous current conduction:

The critical value of input inductor L_{ic} is as follows

$$L_{ic} = \frac{Vin(t)\,D(t)}{2I_{in}(t)f_s} = \frac{Rin\,D(t)}{2f_s} = \left(\frac{V_s^2}{2f_s}\right) \quad (6)$$

$R_{in} \rightarrow$ input resistance

$f_s \rightarrow$ switching frequency and

$P_i \rightarrow$ instantaneous power .

The selection of switching frequency is a tradeoff between the permitted losses in the PFC converter switches and the size of the input inductor .A high switching frequency reduces the size and value of input side inductor but increase the switching losses of the solid state devices and it requires a large size of heat sink. The current stress on

the PFC converter switch in DICM operation gets increases when the low value of inductance is increases. For this reason the switching frequency is selected as 20KHZ such that the losses and current stress of PFC converter switches are low and it also meets the desired performance.

The lowest critical value of input inductance (L_{ic}) is calculated at the lowest possible value of supply voltage ie.,85V for its operation at universal ac mains (85-270V).

The value of $L_{ic\ min}$ is calculated as

$$L_{ic\ min}=\frac{V_{smin}^2}{P_{max}} * \frac{D(t)}{2f_s}$$

$$=\frac{85^2}{500}$$

$$=\frac{0.7206}{2*20000}$$

≈260 µH (7)

where D(t) is the duty ratio calculated at Dc link voltage of 310 V and peak value of supply voltage of $85\sqrt{2}$V.

To achieve the discontinuous current transmission by picking the minimum value of input inductors (L_{i1} and L_{i2}) which should be less than $L_{ic\ min}$ (35).Therefore the values of $L_{i1}=L_{i2}=70$ µH to accomplish intermittent current transmission .`

The manifestation for C_1 and C_2 are

$$C1=C2=\frac{V_{dc}D_t}{\Delta V_c(t)f_sR_L}$$

$$=\frac{V_{dc}D_t}{\eta(V_{in}(t)+V_{dc})f_sR_L} \quad (8)$$

V_{cd}=legalized ripple voltage athwart in-between capacitors C1 and C2

Vc=middle capacitor voltage

RL=rivaled load resistance

$$RL=\frac{V_{dc}^2}{P_i}$$

The rate of intermediate capacitor is considered at the extreme value of intermediate capacitor ripple which arises at rated dc link voltage of 310V and extreme source voltage of 270 V .

$$C1=C2=\frac{V_{dcmax}D(t)}{\eta\{\sqrt{2}V_{smax}(t)+V_{dc}\}f_sR_L}$$

$$=\frac{310*0.4481}{0.1\{270\sqrt{2}+310\}20000*192.2}$$

=0.522 µF

Where the quantity of allowable voltage across the intermediate capacitors desired for this claim should have low ohmic losses. Therefore the film capacitors are used for this application .

C.STRATEGY OF DC LINK CAPACITORS(C_d):

The value of Cd is as follows

$$Cd=\frac{I_{dc}}{2\omega\Delta V_{dc}}=\left(\frac{P_i}{V_{dc}}\right)\frac{1}{2\omega\kappa V_{dc}} \quad (10)$$

If the value of DC link voltage is minimum then the design will in worst case. It is expressed as Cd,

$$Cd=\left(\frac{P_{min}}{V_{dcmin}^*}\right)\frac{1}{2\omega\Delta V_{dcmin}}=\left(\frac{113}{70}\right)\frac{1}{2*314*0.02*70}$$

≈ = 1836µF (11)

Therefore the DC link capacitor with a adjacent potential rate of 2200 µF is nominated for this presentation.

For this presentation the electrolytic capacitors are top suitable because it must have a large capacitance per unit volume due to the high rate of capacitance and its process at comparatively high current and low frequency switching.

D.STRATEGY OF FILTER PARAMETERS(Lf AND Cf):

The higher order harmonics in the supply system are ducked with the help of low pass LC filter. The extreme rate of filter capacitance is given as (36)

$$Cmax=\left(\frac{I_m}{\omega_L V_m}\right)\tan(\theta)$$

$$=\left(\frac{P_o\sqrt{2}V_s}{\omega_L V_m}\right)\tan(\theta)$$

$$=\frac{\left(\frac{500\sqrt{2}}{220}\right)}{314*220\sqrt{2}V}\tan(1^\circ)$$

=574.27 nF. (12)

Therefore Cf of 330 nF is selected .

The rate of filter inductor is planned by seeing the source impedance(Ls) of 4%-5% of the base impedance .Hence the auxiliary value of inductance obligatory is given as

$$Lf=Lreq+Ls=\frac{1}{4\pi^2 f_c^2 C_f}=Lreq+0.05\left(\frac{1}{\omega_L}\right)\left(\frac{V_s^2}{P_o}\right)$$

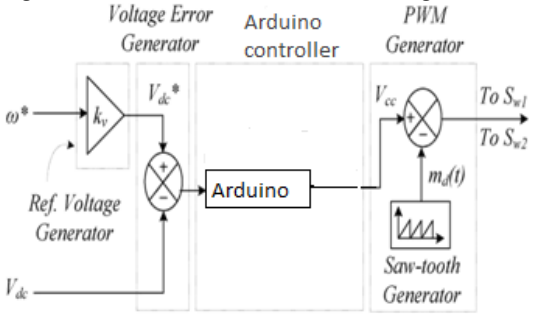
$$Lreq=\frac{1}{4\pi^2*(2000^2)*330*10^{-9}}-0.05\left(\frac{1}{314}\right)\left(\frac{220^2}{500}\right)$$

=3.77mH (13)

Where fc is the cut off frequency which is designated such that fl<fc<fs

Therefore fc is reserved as fs /10

Fig 5. Control of PFC BL-CSC converter feeding BLDC motor drive.



This LC filter taking inductance Lf (3.77mH) and capacitance Cf (330 nF). We can choose film capacitor with polypropylene dielectric for nourishing the high frequency current ripples reduction in the existing converter.

IV CONTROL OF THE PFC BL-CSC CONVERTER – FED BLDC MOTOR DRIVE :

In our motor drive voltage supporter system is used .A single voltage sensor is desirable for monitoring the DC link voltage .So that speed of the motor is meticulous . Fig 5 shows the block diagram of DC link voltage control.

It contains reference voltage generator ,voltage error generator , a voltage controller and a PWM generator, product of reference speed 'ω' and motor voltage 'k_v' (constant) produces the reference voltage generator .

$$V_{dc}^*=\kappa_v\omega^* \quad (14)$$

Reference dc link voltage is related with the detected dc link voltage (V_{dc}) ,to yield an error voltage (V_c) by using voltage error generator.

The error voltage is specified as

$V_e(\kappa) = V_{dc}(\kappa)^* - V_{dc}(\kappa)$ (15)

Finally ,we can find the PWM signals by computing the output of PI controller (V_{cc}) .With saw tooth high frequency signal(m_d) is assumed as

for $V_s > 0$; { if $m_d < V_{cc}$,then S_{w1}='ON' ; if $m_d \geq V_{cc}$,then S_{w1}='OFF' } (16)

for $V_s < 0$; { if $m_d < V_{cc}$,then S_{w2}='ON' ; if $m_d \geq V_{cc}$,then S_{w2}='OFF' }

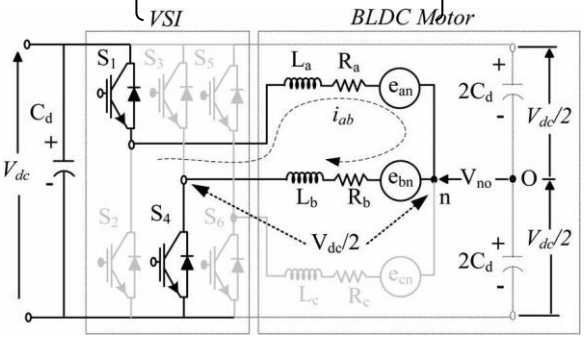


Fig 6. Three phase VSI feeding a BLDC motor

TABLEII
SWITCHING STATES FOR ELECTRONIC COMMUTATION OF BLDC MOTOR BUILT ON HALL-EFFECT POSITION SIGNALS

θ(°)	Hall Signals			Switching States					
	H_a	H_b	H_c	S_1	S_2	S_3	S_4	S_5	S_6
NA	0	0	0	0	0	0	0	0	0
0-60	0	0	1	1	0	0	0	0	1
60-120	0	1	0	0	1	1	0	0	0
120-180	0	1	1	0	0	1	0	0	1
180-240	1	0	0	0	0	0	1	1	0
240-300	1	0	1	1	0	0	1	0	0
300-360	1	1	0	0	1	0	0	1	0
NA	1	1	1	0	0	0	0	0	0

B.CONTROL OF BLDC MOTOR:

The electronic commutation of BLDC motor is found by identifying the rotor position with the help of hall effect position sensor.

In trapezoidal back emf BLDC motor ,2 stator phases conduct at any given instant of time by via standard commutation procedure .Rotor position material is used to turn ON and OFF the switches in VSI to follow the current flow in separate windings.

Rotor position can be detected on a span of 60˚ by spending hall effect position sensor (H_a , H_b , H_c).

Fig 6 shows conduction states of 2 switches S_1 and S_4. The line current (I_{ab}) is obtained from Dc link ,whose magnitude based on the functional dc link voltage V_{dc} ,the back emf e_{an} and e_{bn} , resistance(R_a & R_b),mutual inductance and self inductance (M,L_a,L_b) of the stator windings. The altered switching states of the VSI feeding a BLDC motor based on the hall effect position signal (H_a-H_c) which is exposed in table II.

VI OUTCOMES AND DISCUSSION :

The performance of the projected energy was established as a hardware prototype which was experimentally confirmed. In our scheme DSP TI-TMS320F2812 is used to grow our drive . In between the digital signal processing and the gate driven of the VSI the opto separation is decided .6N136 opto couplers are used in PFC switches .To make our circuit more compactable with A/D converter of the DSP some of the security and ascending circuits are established to extent the output voltage sensor to 0-3 V whereas , for the hall effect position sensors hall signal filtering and power circuitries are established. The acceptable procedure of BLDC motor is done by educating the detecting of rotor position with the help of DSP based average filter (37).Now we are going to see about the test results of our paper .They are as follows

A.STEADY STATE PERFOMANCE :

The following diagrams signify the test results of our motor drive at a rated load with a supply voltage of 220V and Dc link voltages of 310V and 70V respectively. The dc link voltage is kept at desired value with various magnitude and frequency of the stator current starting in the BLDC motor working at different speeds. A sinusoidal supply voltage is achieving which exhibits a unity power factor at both the values of DC link voltages .

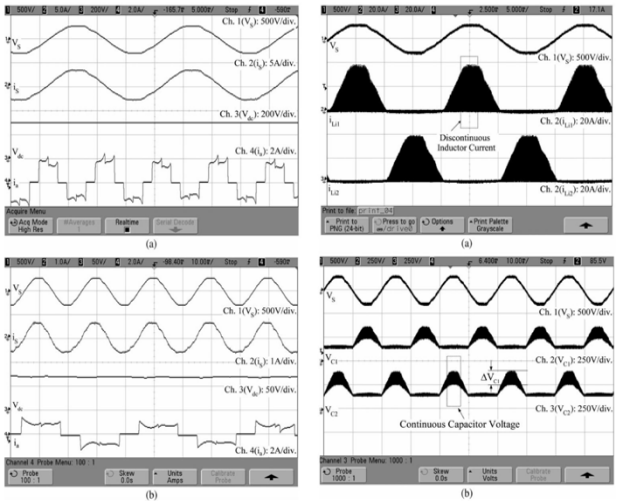


Fig. 7. Performance of the proposed drive at rated condition withsupply voltage as 220 V and dc link voltage as (a) 310 V and (b) 70 V.

Fig. 8. Waveforms of (a) inductors' currents and (b) intermediate capacitor voltage with supply voltage at rated load on the BLDC motor with dc link voltage as 310 V and supply voltage as 220 V.

switch(Fig 9-a and 9-b) . A constant voltage is obtained in the intermediate capacitor(Fig 8-b).

RMS value of current in PFC converter switches is half of the input RMS current .For that purpose conduction losses are reduced and RMS current is low . So that small size of heat sink is mandatory for this application.

C.DYNAMIC PERFOMANCE OF THE PROPOSED BLDC MOTOR DRIVE :

The Figure 10 represents the dynamic routine of our drive during various values of supply voltage and DC link voltages. The figure 10-a represents the initial of our motor during step change in the DC link voltage from 0-5V at a supply voltage of 220V.The frequency of stator current rises then the speed of our motor is also gets amplified and also narrow inrush current and supply current are observed in this motor drive.

The step change in dc link voltage from 100 to 170 V during speed control which is characterized in diagram (fig 10b) as dynamic performance of our drive. During the step change in dc link voltage from 250 to 180 V the dc link voltage is kept constant which fulfil the closed loop performance of our drive . It is represented as dynamic performance of motor drive in figure 10-c.

D.PFC AND IMPROVED POWER QUALITY AT AC MAINS :

This content compacts with practical power quality guides at the ac mains to operate our BLDC motor drive at different values of DC link voltages and supply voltages .The size of excellence guides are done by using the casual mode power analyzer.

Three different types of waveforms are found during power quality guides. They are as follows :i)In this wave form 4 different cases are exhibited about i)RMS value ii) frequency iii)crest factor (CF) of supply voltage and supply current. These are showed in the figure (11 a, d, g, j)

ii)In this set of waveform active ,reactive and apparent power ,power factor (PF);and the displacement power factor at ac mains. These are showed in the figure (11 b,e,h &k)

iii)In this third set harmonic spectra and the obtained THD of supply current at AC mains are showed in the figure(11 c,f,i,1)

The performance of our drive is showed in figure (11 a-f) with rated supply voltage and rated dc link voltage of 310 V and 70V respectively. whereas in figure (11 g-i) shows the performance of our drive with rated load on the motor with supply voltages of 259V and 170V respectively.

In both the cases the power factor is attained to unity power factor and low THD of supply current at the ac mains in the limits of IEC 61000-3-2 [10].

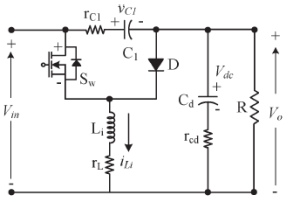


Fig. 12. Circuit configuration of the CSC converter with parasitic resistances.

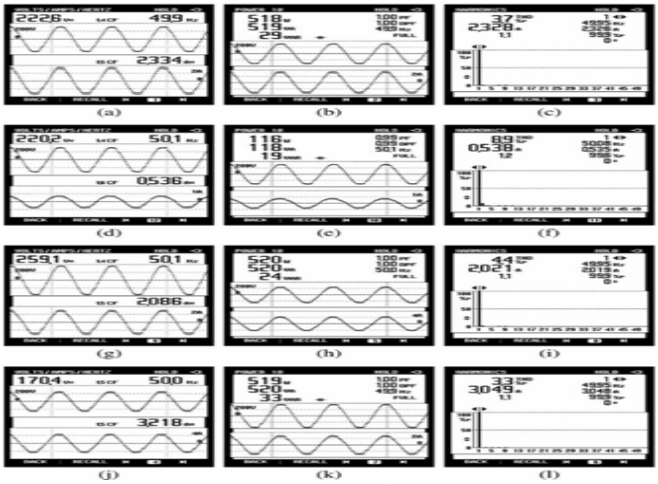


Fig. 14. Recorded power quality indices of the proposed drive at ratedload on the BLDC motor for (a)–(c) V_{dc}=**300** V, V_S= **220** V; (d)–(f) V_{dc}=**70** V,V_S = **220** V; (g)–(i)V_{dc} = **300** V,V_S = **259** V; and (j)–(l)V_{dc} = **300** V,V_S= **170**V.

E.EVALUATION OF EFFICIENCY OF PROPOSED DRIVE WITH CONVENTIONAL SCHEME :

In BLDC motor drive the losses are present in BLDC motor, VSI, PFC converter. The losses are independently measured in three different parts of our drive.The two types of losses are fixed and variable .The fixed. Losses are core and windage losses. The copper loss depends on current flow in the stator winding .It can be sedate by using standard technique(ie.,) No load test by it with a DC machine. PFC converter losses are considered by calculating the input power and output power sensing ,DC link voltage ,current,supply voltage and supply current.VSI losses sedate by the widespread drive system.

TABLE III : COMPARISON OF EXISTING AND PROPOSED SYSTEM

DBR FED BLDC MOTOR	**BL-CSC MOTOR**
BLDC has very high losses.	Losses are low compared to BL-CSC fed motor DBR
It causes more switching losses soin this motor switching frequency are high.	Switching losses in VSI are significantly reduced ,because DBR at the front end converter is eliminated.
It has less efficiency. Fig 12 a&b	It has more efficiency. The efficiency is increased in the order of 4% to 5%

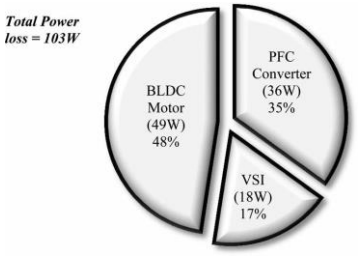


Fig. 11. Percentage of losses in different parts of the proposed BLDC motor drive

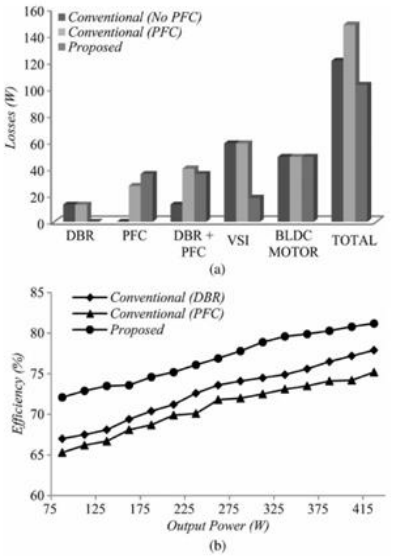


Fig. 13. Comparative analysis of (a) losses and (b) efficiency of the proposed drive with the conventional scheme.

VIII CONCLUSION:

A power factor correction based canonical switching cell converter for VSI fed BLDC motor by using voltage follower technique is used to increase the power quality at the AC mains The DC link voltage at the front end of VSI fed BLDC motor is changed to control the speed of the motor with the help of PFC converter. From the above action, VSI which works in a fundamental frequency switching when it is electronically commutated , minimizes the switching losses. Conduction losses are also reduced by eliminating the DBR circuit in CSC configuration in existing system. The power quality is improved at the AC mains for a substantial range of speed and supply voltage in concern. Finally the desired output was obtained for the proposed drive. This is mainly recommended for low power applications.

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