International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 3 Issue 2, February - 2014

A Novel Z-source Based Multilevel Inverter with Reduced Components

V. Manivannan [1]
D. DanPrakash [2]
R. D'souza Praveen Kumar [3]
[2] (Asst.Prof, Department of EEE)
[1] [3](PG Students of Power Electronics and Drives)

Abstract: **In this paper a novel Z-source based multilevel inverter with reduced components is proposed. The suggested circuit consists of two DC sources, single phase transformers and semiconductor switches in each basic unit of the inverter. This inverter, which operates as symmetric and asymmetric, here the output more number of voltage levels in the same number of the switching devices. Besides, the number of gate driving circuits is reduced so the circuit size and cost can be reduced and it is more reliable against short circuit. In this paper the output voltage is easily controlled and reduced total harmonic distortion (THD) is proposed. The simulation is done by MATLAB/SIMULINK software for up to thirteen levels.**

Keywords: Z-source, Cascaded multilevel inverter, Reduction of components, voltage boosting.

I. INTRODUCTION

Nowadays multilevel inverters are having more and more attention and perfect choice because of their high voltage operations, high efficiency and multilevel inverters have been widely applied in several industries such as large induction motor drives, energy conversion systems, compensation device and etc.

The three common topologies for multilevel inverters are as: (1) diode clamped, (2) flying capacitors and (3) cascaded H-bridge inverters [5, 6, 7].In this cascaded H-bridge inverters have been focused in these topologies because of the modularity and the simplicity [8]. Cascaded H-bridge inverters can also increase the number of output voltage levels easily by increasing the number of H-bridges. However, if the number of output voltage levels is increased, the number of switching Devices is also increased, which makes a multilevel inverter more Complicated. However, the cascaded

H-bridge type multilevel inverter has a disadvantage that the independent DC-link voltage needs to be provided by each H-bridge separately. To reduce the number of independent DC sources, methods were introduced in recent years [9].

In this paper, a multilevel inverter using two Z-sources and two DC voltage sources, single phase transformers and semiconductor switches is proposed. The number of switching devices and DC voltage sources of the proposed inverter is reduced. Capacitors, batteries, and other DC voltage sources can be used as the voltage sources of the proposed inverter. Proposed inverter can operates as symmetric or asymmetric converter. Here the Single phase transformers are used in this topology therefore it can be used for high or medium voltage distribution level system, so the inverter output voltage can be increased by using the cascaded. Occurring of short circuit can destroy the cascaded transformer based multilevel inverters to avoid this problem, cascaded Transformers based cascaded H-bridge inverters using Z-source is proposed. In this proposed topology the Z-Source inverter which employs LC network and it's connected with the two DC voltage sources.

In section II, the circuit topology of the proposed inverter is introduced. In section III, the operation and application of the inverter is described. In section IV, Simulation results are shown. In section finally in section V draws the conclusions.

II. PROPOSED MULTILEVEL INVERTER

The cascaded H-bridge type multilevel inverter has a Disadvantage of that the independent DC-link voltage needs to be provided by each H-bridge separately to reduce the number of independent DC sources the cascaded transformer inverter with two DC sources and Z-sources is proposed.

In multilevel inverter topologies, the required number of power devices depends on the output voltage levels. However, increasing the number of voltage levels increases number of components and increasing the number of components is increases the inverter circuit size, cost, Installation area and control complexity of the circuit. In this proposed circuit model, a number of switches and DC sources can be reduced. The number of output voltage levels in the suggested topology is 2n+ 1 where n is the number of H-bridge cells. Prototype is simulated based on the proposed topology. This topology having more significance for higher rated converters used for high or medium voltage distribution system, as they require transformers to increase the inverter output voltage at the desired or required level.

Fig. 1 shows the circuit topology of the proposed Z-source based multi level inverter. This structure is made of two DC voltage sources, two Z-source impedance network and several single phase inverters. In this circuit several single phase inverter can be cascaded as shown in Fig. 1. Two DC voltage sources are connected with Z-source which is feed all basic or separate units and are the same.

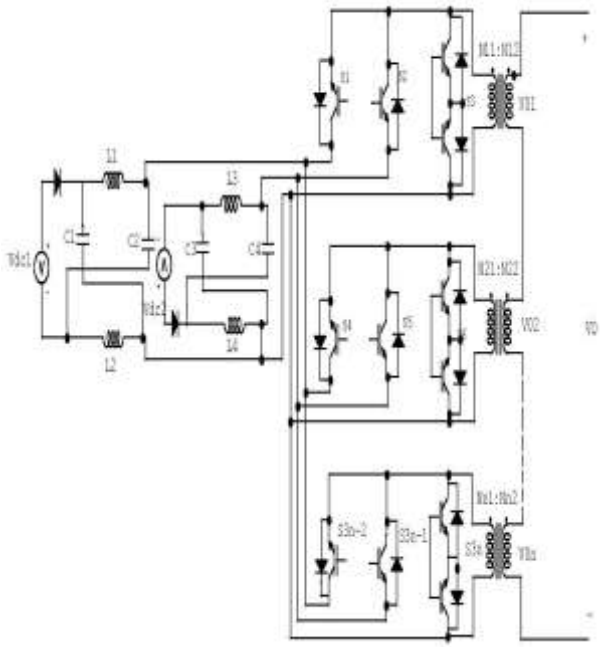


Fig.1. Proposed Z-source based cascaded topology.

For example one basic or separate unit consists of a one single phase transformer and three switches. The proposed multilevel converter requires unidirectional and bi-directional switches. The bidirectional switches with capability of blocking voltage and conducting current in both directions are needed in this multi level inverter. There are several arrangement can be used to create such a bi-directional switch. The common emitter anti-parallel IGBT with diode pair arrangement has been used in this paper. This bi-directional switch Arrangement consists of two diodes and two IGBT. Similarly this arrangement is given to the thirteen level proposed topology.

The output voltage of proposed multi level inverter is achieved by summing (or) adding the output voltages of separate units. Output phase voltage is obtained by:

$$V_O = V_{O1} + V_{O2} + ... + V_{On} \quad (1)$$

Operation of proposed topology is the same as cascaded H-bridge multilevel inverters. In cascaded multilevel inverters, selection of DC sources magnitude is main part of inverter design but in this topology, two DC voltage sources exist and selection of turn's ratio of transformers is more important while designing of circuit. By selecting proper switching functions, positive, negative, and zero voltages can be synthesized. The output voltages of basic units are cascaded through the secondary of the transformers. The input voltage to transformers is defined by switching functions of the separate units. Output voltage is sum of the transformers (secondary) output voltages. The amplitude of the output voltage is determined by the input DC voltage source and turn ratio of the transformers. This proposed topology can operate in asymmetric or symmetric state to obtain uniform step voltage. To provide a large number of output steps without increasing the number of components, asymmetric multilevel converters can be used. In this proposed topology to obtain asymmetric multilevel converters turn ratio of transformers are selected in different value.

The basic problems are mostly occurred in the components, voltage and current rating of semiconductor switches, efficiency, control and cost of multilevel inverter. Voltage and current ratings of the switches in a multilevel inverter affect on the cost and realization of the multilevel inverter. Although volume and the number of components reduce in asymmetric cascaded H-bridge multilevel inverters but switches PIV is the one of the important problems for asymmetric multilevel inverters. In the cascaded H-bridge multilevel inverters the voltage standing on switches.

PIV for switches is given by the following equation:

$$PIV_{sw,i} = V_{dc} \quad (2)$$

$PIV_{aw.i}$ -switch PIV that put on in i_{th} H-bridge cell.
V_i - voltage sources of i_{th} H-bridge cell.

DC voltage sources of all H-bridge cells are the same in symmetric cascaded H-bridge multilevel inverters so ($V_i = V_{dc}$):

$$PIV_{sw} = V_{dc} \quad (3)$$

A switch PIV in asymmetric state and symmetric state is same in this topology.

A. Transformers Turn Ratio for Z-Source Based MLI (proposed topology):

If all turn ratios of transformers are the same, the inverter is known as symmetric multilevel inverter, Here

$$N_{i1} = p \, , \, N_{i2} = q \, , \, i = 1,2,3,....,n \quad (4)$$

The maximum number of phase voltage levels is given by:

$$m = 2n+1 \quad (5)$$

n- Number of transformer.
m- Maximum number of levels of phase voltage.

The maximum output voltage (V_{Omax}) is:

$$V_{O\,max} = n\,(q/p)V_{dc} \quad (6)$$

III. OPERATION OF PROPOSED TOPOLOGY

Fig.2. Shows proposed topology with six separate units. The magnitude of each voltage source (V_{dc}) is considered 50 V. Here, turn ratio of transformers are selected according to given method ref (2.1) in this method all turn ratio of transformers are the same. Operation of multilevel inverters

depends on the modulation methods. There are several modulation strategies for multilevel inverters. Modulation techniques for cascaded multilevel inverters are usually an extension of the two level modulations [10-12].

According to its switching frequency they can be classified as: fundamental switching and high switching frequency. According to high switching frequency different algorithm are introduced in recent years [13].

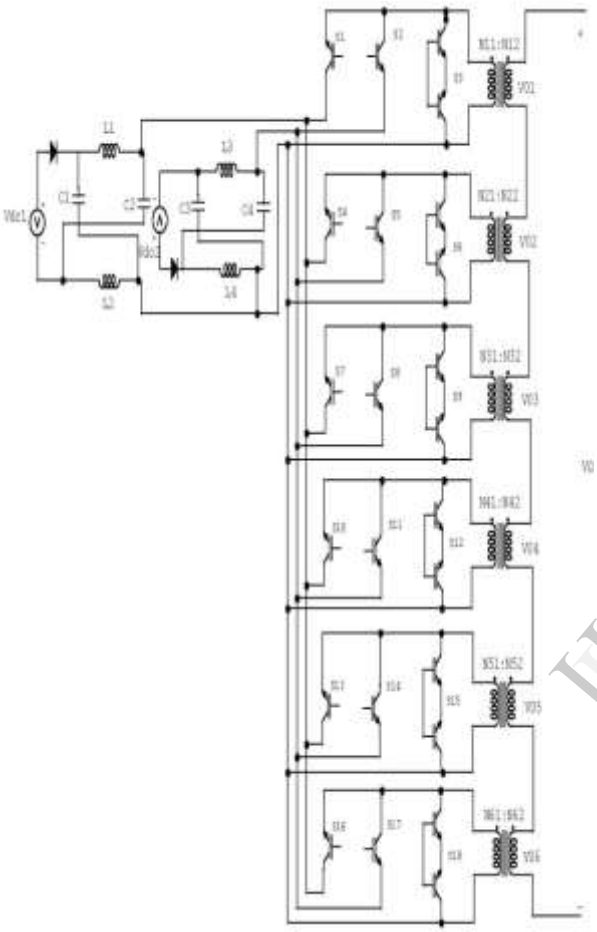


Fig.2. proposed topology Z-source based multilevel inverter

In this, Multi-carrier sub-harmonic pulse width modulation (MCSHPWM) technique is mostly used. The principle of the MCSHPWM method is based on a comparison of a sinusoidal reference waveform, with shifted carrier triangular or DC waveforms shown in fig .3.

Operation of 13-level proposed topology has shown in simulation result. In the other hand, Fig.6&7 shows signals of switches gate (switching) and output waveform of voltage. From comparison among sine wave and DC waves thirteen pulses are created. These pulses are used to switching with notice to lookup table of multilevel switching. Lookup table of 13-level proposed topology is shown in table1. For example if sine wave greater than second carrier and lower than third carrier then P2 is created and this pulse for production of second level is given to S1, S4 and S9. In Fig.4, Z indicates to zero level, P1, P2,P3,P4,P5and P6 indicate to positive levels and N1, N2,N3,N4,N5and N6 indicate to negative levels. Fig. 5.shows gate signals of switches. Output voltage is shown in Fig.7.

TABLE I. LOOK UP TABLE FOR SWITCHING FROM S_1 TO S_9:

1=on, 0=off

O/P Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
$+6V_{dc}$	1	0	0	1	0	0	1	0	0
$+5V_{dc}$	1	0	0	1	0	0	1	0	0
$+4V_{dc}$	1	0	0	1	0	0	1	0	0
$+3V_{dc}$	1	0	0	1	0	0	1	0	0
$+2V_{dc}$	1	0	0	1	0	1	0	0	1
$+1V_{dc}$	1	0	0	0	0	1	0	0	1
0	0	0	1	0	0	1	0	0	1
$-1V_{dc}$	0	1	0	0	0	0	0	0	1
$-2V_{dc}$	0	1	0	0	1	0	0	0	1
$-3V_{dc}$	0	1	0	0	1	0	0	1	0
$-4V_{dc}$	0	1	0	0	1	0	0	1	0
$-5V_{dc}$	0	1	0	0	1	0	0	1	0
$-6V_{dc}$	0	1	0	0	1	0	0	1	0

TABLE IA. LOOK UP TABLE FOR SWITCHING FROM S10 TO S18:

1=on, 2=off

O/P Voltage	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{16}	S_{17}	S_{18}
$+6V_{dc}$	1	0	0	1	0	0	1	0	0
$+5V_{dc}$	1	0	0	1	0	0	0	0	1
$+4V_{dc}$	1	0	0	0	0	1	0	0	1
$+3V_{dc}$	0	0	1	0	0	1	0	0	1
$+2V_{dc}$	0	0	1	0	0	1	0	0	1
$+1V_{dc}$	0	0	1	0	0	1	0	0	1
0	0	0	1	0	0	1	0	0	1
$-1V_{dc}$	0	0	1	0	0	1	0	0	1
$-2V_{dc}$	0	0	1	0	0	1	0	0	1
$-3V_{dc}$	0	0	1	0	0	1	0	0	1
$-4V_{dc}$	0	1	0	0	0	1	0	0	1
$-5V_{dc}$	0	1	0	0	1	0	0	0	1
$-6V_{dc}$	0	1	0	0	1	0	0	1	0

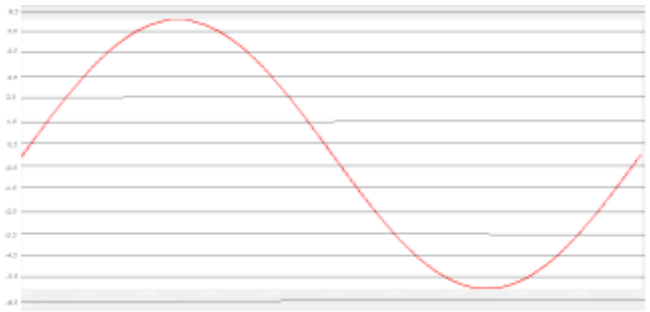


Fig.3. Modulation waveform.

IV. SIMULATION CIRCUIT AND RESULTS

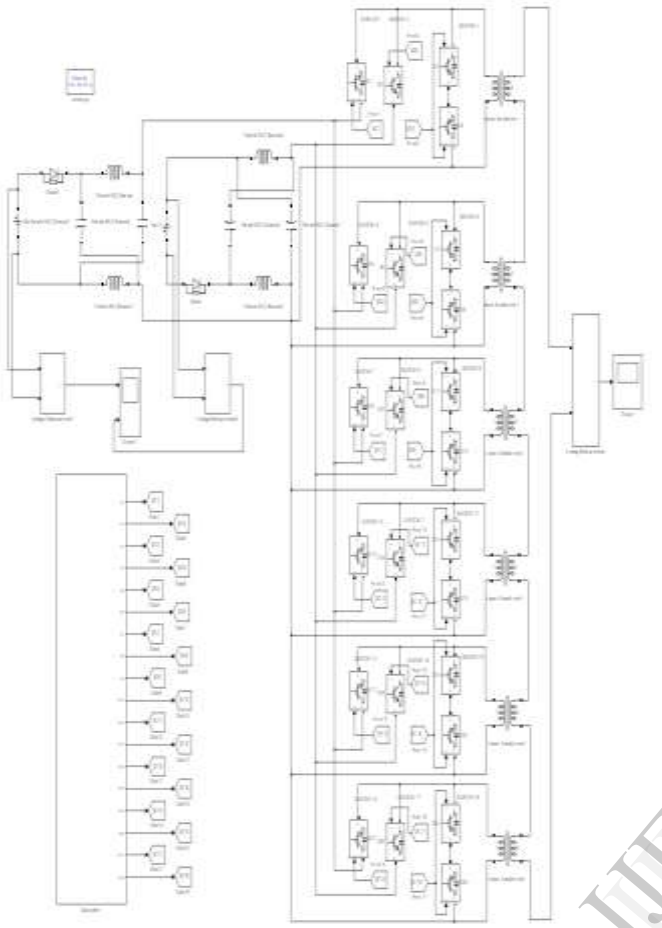


Fig.4. Simulation circuit for proposed topology.

In the previous section operation of symmetric proposed topology has been shown. To evaluate the expected performance for proposed topology in the generation of a desired output voltage waveform, a prototype is simulated based on the proposed topology according to that one shown in Fig.4.The simulation results carried out by MATLAB/SIMULINK.

In this simulation, V_{dc}=1 $_{pu}$ and output frequency is 50Hz.The generated switch pulse is shown in Fig.5, and g gate signals are shown in fig.6, The output voltage for the Z-source based multilevel inverter is shown in Fig.7, Output phase voltage of the proposed inverter is achieved by summing the output voltages of separate units .

The harmonic spectrum of output voltage is shown in Fig.8, respectively. The proposed multilevel inverter has 13-level voltages per phase with the fewest components. Total harmonic distortion (THD) of output voltage is as low as 7%. It can be observed from the harmonic spectrum of voltages that, presented topology is effective to meet low harmonic level.

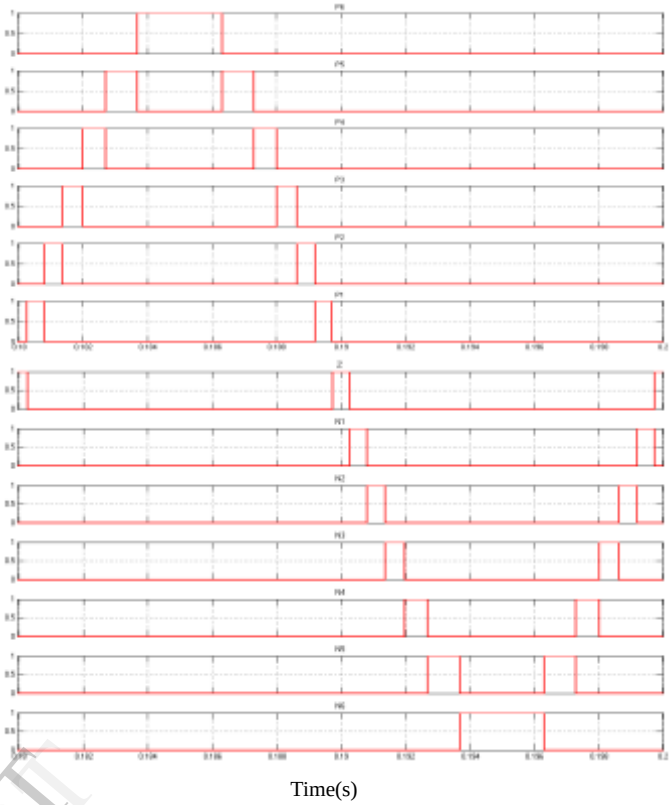


Fig.5. Switching pulses for proposed topology.

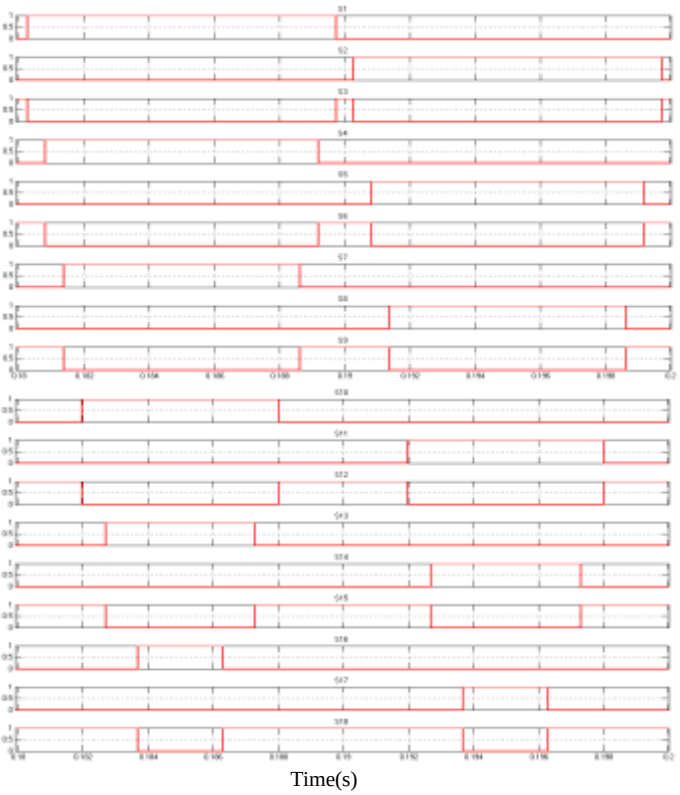
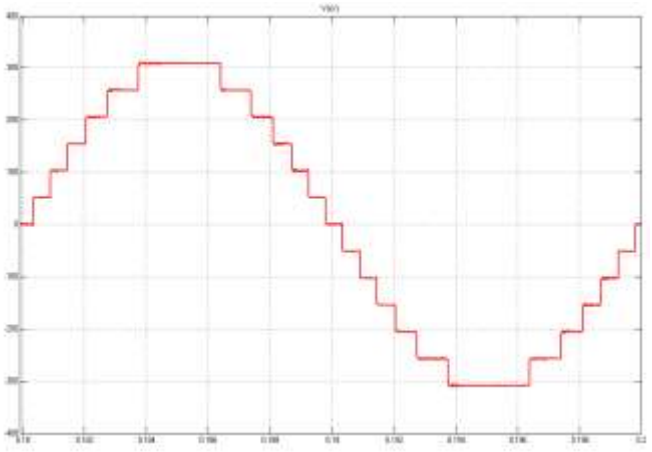


Fig.6, Gates signals for proposed topology.



Time(s)

Fig.7. Output voltage.

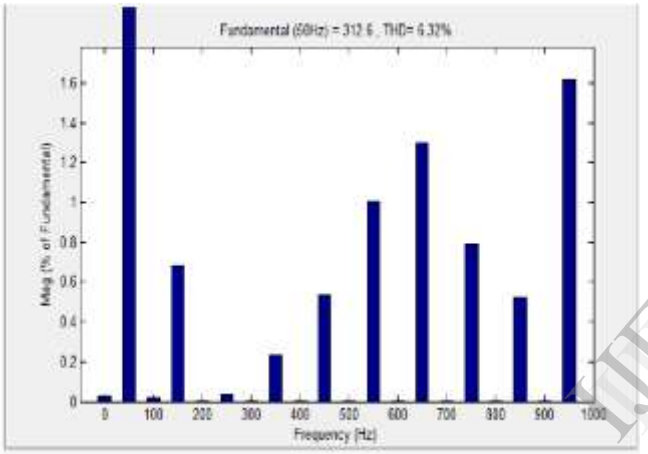


Fig.8.Harmonic spectrum of output voltage.

V. CONCLUSIONS

This paper proposed a Z-source based multilevel inverter employing low-frequency single-phase transformers and two DC input power source and Z-source networks and boosting of input DC voltage is also possible by employing Z-source. The proposed circuit configuration can reduce a number of switches and DC sources compared with conventional cascaded H-bridge multilevel inverters. The performance of the proposed multilevel inverter has been verified by simulation results.

REFERENCES

1. AK. AI-Othman, Tamer H. Abdelhamid, "Elimination of harmonics in multilevel inverters with non-equal de sources using PSO", Elsevier Energy Conversion and Management, Vol. 50, pp. 756-764,2009.
2. O. Said Barkati, Lotfi Baghli, EL Majid Berkouk, Mohmed-Seghir Boucherit, "Harmonic elimination in diode-clamped multilevel inverter using evolutionary algorithms", Elsevier Electric Power System Research, Vol. 78, pp. 1736-1746,2008.
3. Keith A Corzine, Mike W. Wielebski, Fang Z. Peng, Jin Wang, "Control of Cascaded Multilevel Inverters", IEEE Trans. on Power Electronics, Vol. 19, No. 3, pp. 732-738,2004.
4. Ebrahim Babaei, Seyed Hossein Hosseini, "New cascaded multilevel inverter topology with minimum number of switches", Elsevier Energy Conversion and Management, 50 (2009) 2761-2767.
5. J. Rodriguez, 1. Lai, F. Z. Peng, "Multilevel Inverters: a Survey ofTopologies, Controls, and Applications", IEEE Trans. on Ind. Appl. , Vol. 49, No. 4, pp. 724-738,2002.
6. Jeyraj Selvaraj, Nasrudin A Rahim, "Multilevel Inverter for Gird - Connected PV System Employing Digital PI Controller", IEEE Trans. on Industrial Electronics, Vol. 56, No. 1, pp. 149-158,2009.
7. P. Zhiguo, F. Z. Peng, "Harmonics Optimization of the Voltage Balancing Control for Multilevel Converterl Inverter Systems", in: Proceedings of the IEEE 39th Annual Industry Applications Conference, Vol. 4, pp. 2194-2201, 2004
8. J. I. Leon, S. Vazquez, A. J. Watson, L. G. Franquelo,P. W. Wheeler, J. M. Carrasco, "Feed-forward space vector modulation for single-phase multilevel cascaded converters with any DC voltage ratio," IEEE Trans. Industrial Electronics, Vol. 56, No. 2, pp. 315-325, Feb. 2009.
9. E. Barcenas, S. Ramirez, V. Cardenas, R. Echavarria, "Cascaded multilevel inverter with only one dc source ", in Proceeding of VIII IEEE Inter. Tech. Proc. CIEP, pp. 171-176, 2002.
10. M. R. Banaei, E. Salary, "Verification of New Family for Cascade Multilevel Inverters with Reduction of Components ",Journal of Electrical Engineering & Technology,Vol. 6, No. 2, pp. 245-254, 2011.
11. E. Babaei, S.H. Hosseini, G.B. Gharehpetian, M.TarafdarHaque, M. Sabahi, "Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology", Electric Power Systems Research, pp. 1073–1085, 2007.
12. M. R. Banaei, E. Salary, " Analysis of a Generalized Symmetrical Multilevel Inverter", Journal of Circuits, Systems, and Computers, Vol. 20, No. 2, pp. 1-13, 2011.
13. J. I. Leon, S. Vazquez, S. Kouro, L. G. Franquelo, J. M. Carrasco, J. Rodriguez, "Unidimensional modulation technique for cascaded multilevel converters", IEEE Transactions on Industrial Electronics, Vol. 56, No. 8,pp. 2981–2986, Aug. 2009.

V. Manivannan He received his B.E degree in Electrical and Electronics Engineering in 2011 from Easwari Engineering College, Affiliated to Anna University Chennai, Tamilnadu, India and he is currently doing his M.E degree in Power Electronics and Drives in CSI College of Engineering, The Nilgiris, affiliated to Anna University -Chennai. Tamilnadu, India. His main research interests are power electronics and renewable energy.

D. Danprakash He is working as an Asst. Prof in CSI College of Engineering, Department of EEE, The Nilgiris, India. He obtained his B.E degree in Electrical Engineering from Odaiyappa College of Engineering and Technology, Theni, India in the year of 2010, and M.E degree in 2013 from Jayam College of Engineering and Technology, Dharmapuri, India. He has 1 year teaching experience and his area of research is in Power electronics and renewable energy.

R. D'souza Praveen Kumar He received his B.Tech degree in Electrical and Electronics Engineering in 2008 from Manakula Vinayagar Engineering College, Pudhucherry, India and he is currently doing his M.E degree in Power Electronics and Drives in CSI College of Engineering, The Nilgiris, Affiliated to Anna University -Chennai. Tamilnadu, India. . He has around 4 years of industrial experience. His main research interests are power electronics, and Power systems.